

Features

- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)
- HBM ESD protection level pass 8KV

Note : The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Applications

- Power Management in LCD TV Inverter.

Product Summary

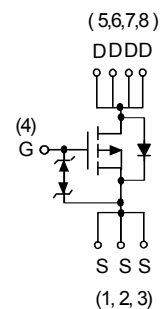
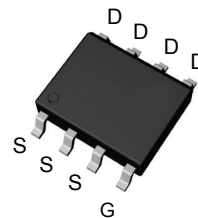
-40V/-16.7A,

$R_{DS(ON)} = 8.5m\Omega$ (max.) @ $V_{GS} = -20V$

$R_{DS(ON)} = 10m\Omega$ (max.) @ $V_{GS} = -10V$

$R_{DS(ON)} = 16m\Omega$ (max.) @ $V_{GS} = -4.5V$

SOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	
V_{DSS}	Drain-Source Voltage	-40	V	
V_{GSS}	Gate-Source Voltage	± 25		
I_D^a	Continuous Drain Current ($V_{GS} = -10V$)	$T_A = 25^\circ C$	-16.7	A
		$T_A = 70^\circ C$	-13.3	
I_{DM}^a	Pulsed Drain Current ($V_{GS} = -10V$)	-66		
I_S^a	Diode Continuous Forward Current	-4		
I_{AS}^b	Avalanche Current, Single pulse	L=0.1mH	-43	mJ
		L=0.5mH	-24	
E_{AS}^b	Avalanche Energy, Single pulse	L=0.1mH	92	
		L=0.5mH	144	
T_J	Maximum Junction Temperature	150	$^\circ C$	
T_{STG}	Storage Temperature Range	-55 to 150		
P_D^a	Maximum Power Dissipation	$T_A = 25^\circ C$	4.2	W
		$T_A = 70^\circ C$	2.7	
$R_{\theta JA}^a$	Thermal Resistance-Junction to Ambient	$t \leq 10s$	30	$^\circ C/W$
		Steady State	75	
$R_{\theta JL}^c$	Thermal Resistance-Junction to Lead	Steady State	24	

Note a : Surface Mounted on $1in^2$ pad area, $t \leq 10sec$.

Note b : UIS tested and pulse width limited by maximum junction temperature $150^\circ C$ (initial temperature $T_J = 25^\circ C$).

Note c : The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ C$, and it is useful for reducing junction-to-case thermal resistance ($R_{\theta JC}$) when additional heat sink is used.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

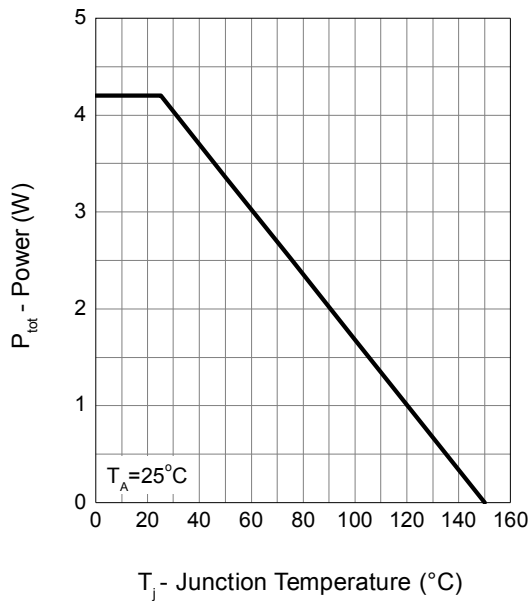
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-32V, V_{GS}=0V$	-	-	-1	μA
		$T_J=85^\circ C$	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1.5	-2	-2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
$R_{DS(ON)}^d$	Drain-Source On-state Resistance	$V_{GS}=-20V, I_{DS}=-16A$	-	7	8.5	m Ω
		$V_{GS}=-10V, I_{DS}=-16A$	-	7.9	10	
		$V_{GS}=-4.5V, I_{DS}=-10A$	-	11.5	16	
Diode Characteristics						
V_{SD}^d	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.75	-1	V
t_{rr}	Reverse Recovery Time	$I_{SD}=-16A, di_{SD}/dt=100A/\mu s$	-	26	-	ns
Q_{rr}	Reverse Recovery Charge		-	19	-	nC
Dynamic Characteristics^e						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	-	3.2	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-20V,$ Frequency=1.0MHz	-	2764	-	pF
C_{oss}	Output Capacitance		-	417	-	
C_{rss}	Reverse Transfer Capacitance		-	325	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	-	15	-	ns
t_r	Turn-on Rise Time		-	12	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	56	-	
t_f	Turn-off Fall Time		-	21	-	
Gate Charge Characteristics^e						
Q_g	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-10V,$ $I_{DS}=-16A$	-	60	-	nC
Q_{gs}	Gate-Source Charge		-	7.6	-	
Q_{gd}	Gate-Drain Charge		-	15	-	

Note d : Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

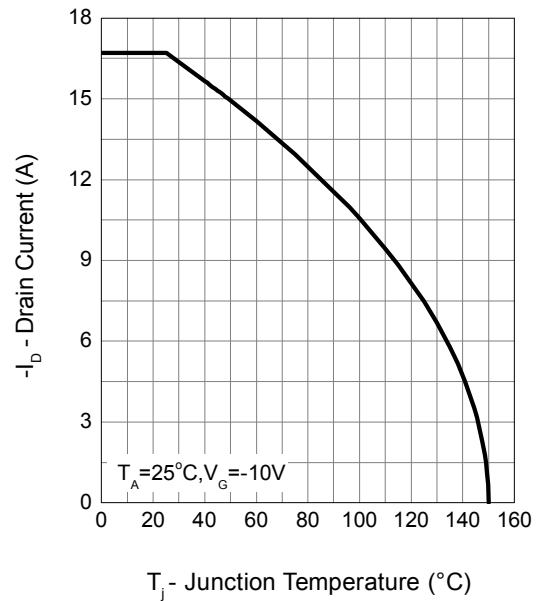
Note e : Guaranteed by design, not subject to production testing.

Typical Characteristics

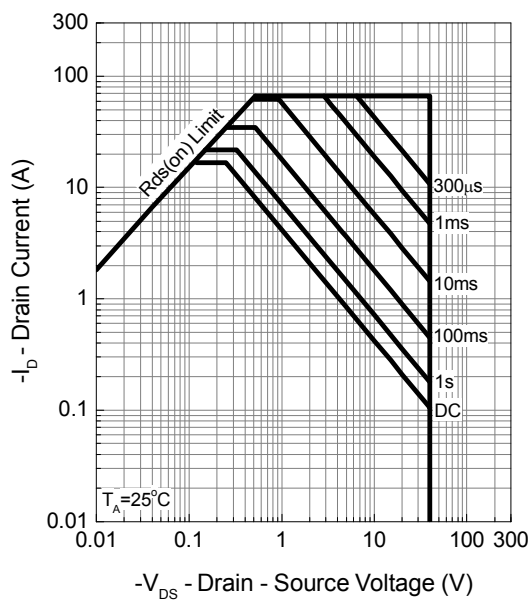
Power Dissipation



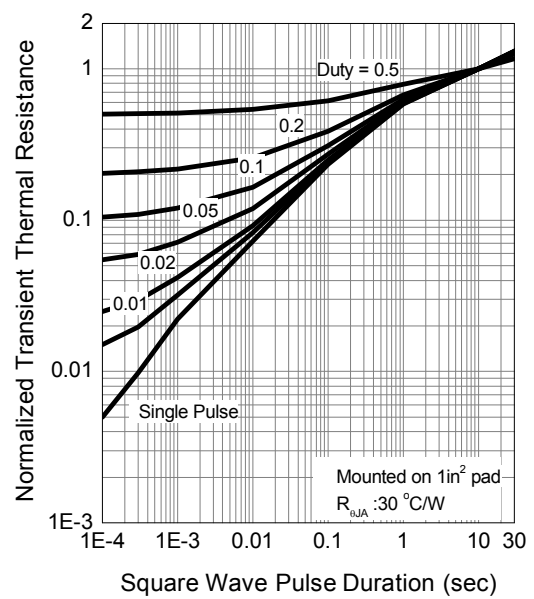
Drain Current



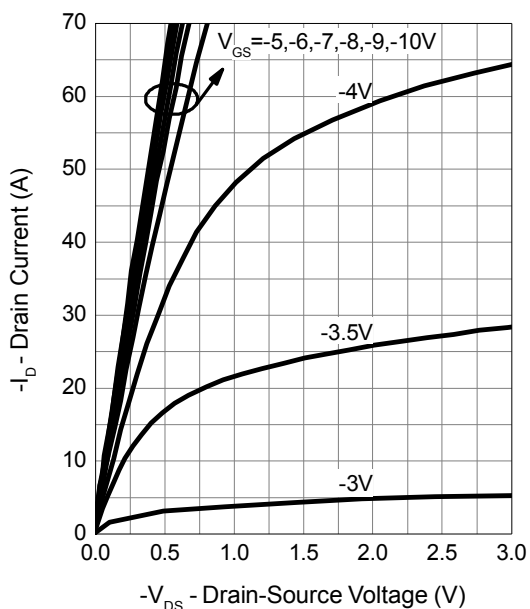
Safe Operation Area



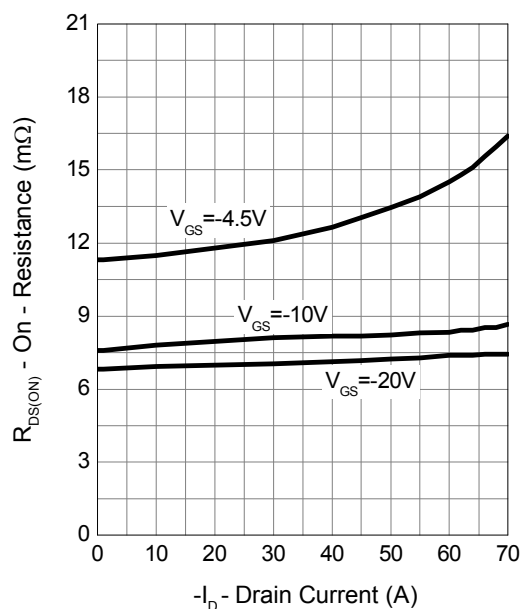
Thermal Transient Impedance



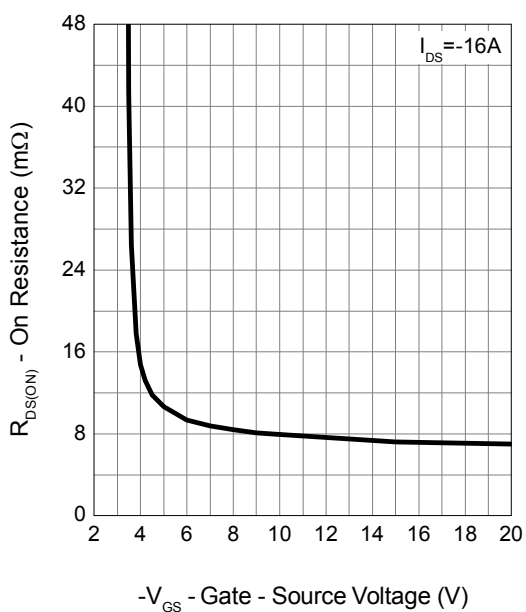
Output Characteristics



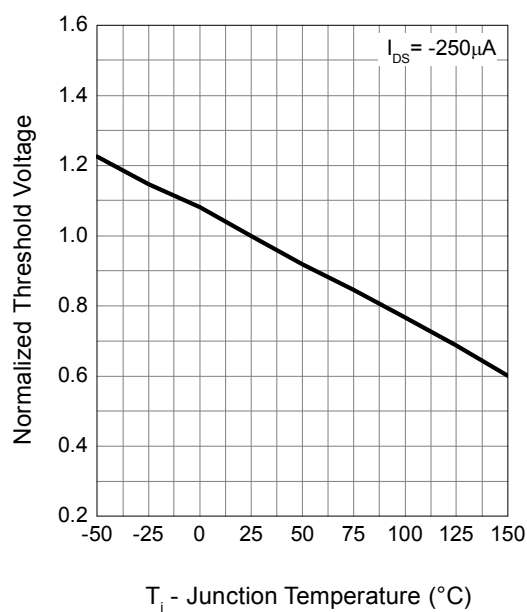
Drain-Source On Resistance



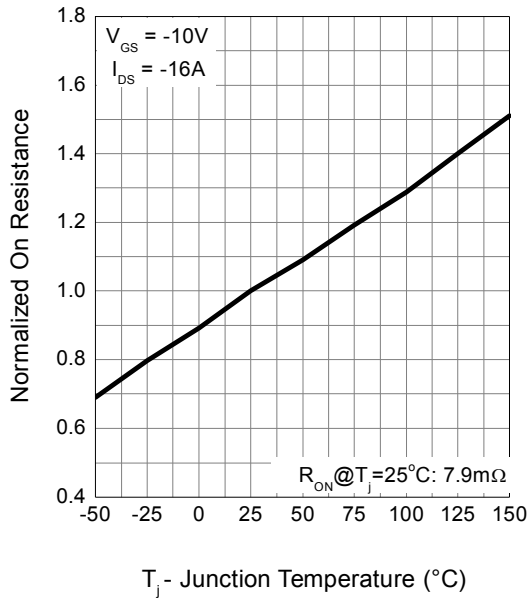
Gate-Source On Resistance



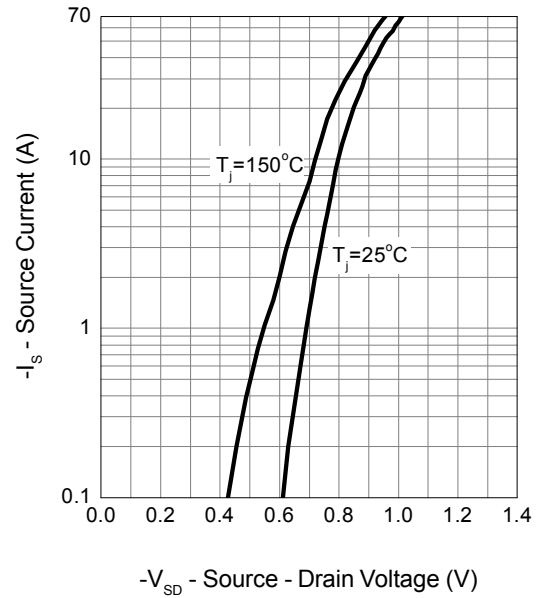
Gate Threshold Voltage



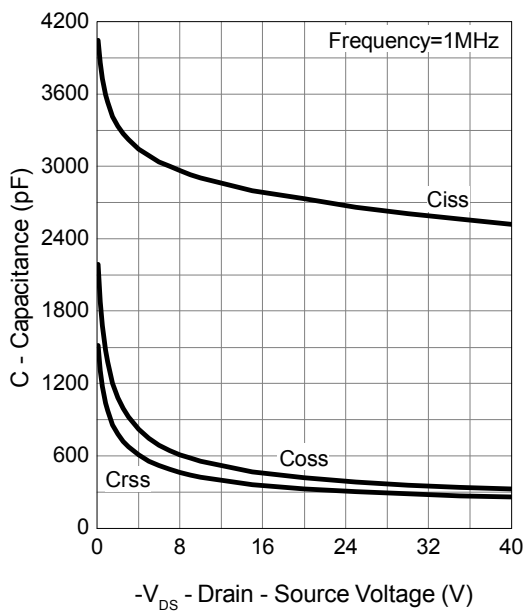
Drain-Source On Resistance



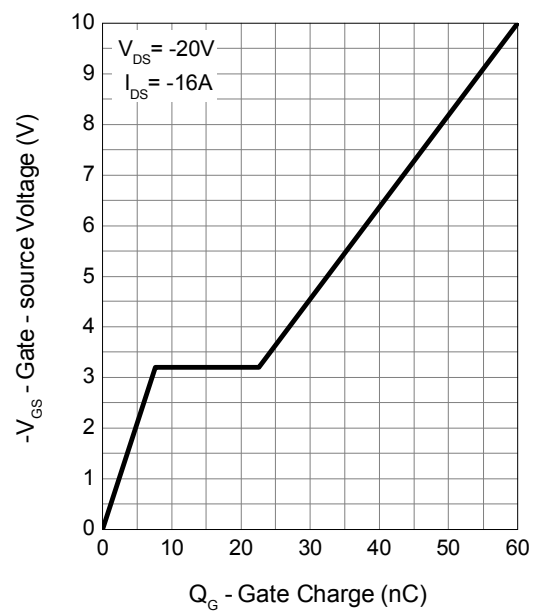
Source-Drain Diode Forward



Capacitance



Gate Charge





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