

**N&P-Channel MOSFET** 

## **General Description**

The WSP6067A is the highest performance trench N-ch and P-ch MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WSP6067A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

#### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

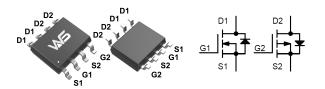
### **Product Summery**

BVDSS	RDSON	ID
60V	38mΩ	7A
-60V	80mΩ	-5A

## **Applications**

- High Frequency Point-of-Load Synchronous Buck Converter.
- Networking DC-DC Power System
- Load Switch

### **SOP-8 Pin Configuration**



## **Absolute Maximum Ratings**

		Rat	ing	
Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DS}$	Drain-Source Voltage	60	-60	V
$V_{GS}$	Gate-Source Voltage	±20	±20	V
I <sub>D</sub> @T <sub>C</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	7.0	-5.0	Α
I <sub>D</sub> @T <sub>C</sub> =100℃	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	4.0	-2.5	Α
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	28	-20	Α
EAS	Single Pulse Avalanche Energy <sup>3</sup>	22	28	mJ
I <sub>AS</sub>	Avalanche Current	21	-24	Α
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	2.0	2.0	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^{\circ}$

## **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
R <sub>0JA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>		85	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>		62.5	°C/W



## N-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	60			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25℃ , I <sub>D</sub> =1mA		0.063		V/°C
D	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =5A		38	52	mΩ
R <sub>DS(ON)</sub>	Static Dialii-Source On-Resistance	V <sub>GS</sub> =4.5V , I <sub>D</sub> =4A		55	75	1117.5
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1	2	3	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> -V <sub>DS</sub> , I <sub>D</sub> -230uA		-5.24		mV/℃
l	Drain Source Leakage Current	$V_{DS}$ =48V , $V_{GS}$ =0V , $T_{J}$ =25 $^{\circ}$ C			1	uA
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	- uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20 V$ , $V_{DS}$ = $0 V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =4A		28		S
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.8	4.3	Ω
$Q_{g}$	Total Gate Charge (4.5V)			19	25	
$Q_{gs}$	Gate-Source Charge	$V_{DS}$ =48V , $V_{GS}$ =4.5V , $I_{D}$ =4A		2.6		nC
$Q_gd$	Gate-Drain Charge			4.1		
T <sub>d(on)</sub>	Turn-On Delay Time			3		
T <sub>r</sub>	Rise Time	V <sub>DD</sub> =30V , V <sub>GS</sub> =10V ,		34		20
T <sub>d(off)</sub>	Turn-Off Delay Time	$R_G=3.3\Omega$ , $I_D=1A$		23		ns
T <sub>f</sub>	Fall Time			6		
C <sub>iss</sub>	Input Capacitance			1027		
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		65		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			45		

### **Guaranteed Avalanche Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
EAS	Single Pulse Avalanche Energy <sup>5</sup>	V <sub>DD</sub> =25V , L=0.1mH , I <sub>AS</sub> =22A	12			mJ

## **Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			2.5	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,6</sup>				24	Α
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A,T <sub>J</sub> =25℃			1.3	V

#### Note:

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, t<10 sec.
- 2. The data tested by pulsed , pulse width  $\leq 300 \text{us}$  , duty cycle  $\leq 2\%$
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =25V, $V_{GS}$ =10V,L=0.1mH, $I_{AS}$ =22A
- 4.The power dissipation is limited by 150 °C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



**N&P-Channel MOSFET** 

## P-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-60			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA		-0.03		V/°C
D	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-3A		80	100	m()
R <sub>DS(ON)</sub>	Static Dialii-Source On-Resistance	V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-2A		100	115	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	\/ -\/   - 350\	-1.2	-1.75	-2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=-250uA$		4.56		mV/℃
	Drain Source Leakage Current	V <sub>DS</sub> =-48V , V <sub>GS</sub> =0V , T <sub>J</sub> =25℃			1	
I <sub>DSS</sub>	Drain-Source Leakage Current	$V_{DS}$ =-48V , $V_{GS}$ =0V , $T_{J}$ =55 $^{\circ}\mathrm{C}$			5	uA uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-3A		8.5		S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		1.5	2.7	Ω
Qg	Total Gate Charge (-4.5V)			13		
$Q_gs$	Gate-Source Charge	$V_{DS}$ =-48V , $V_{GS}$ =-10V , $I_{D}$ =-3A		2.2		nC
Q <sub>gd</sub>	Gate-Drain Charge			6.3		
T <sub>d(on)</sub>	Turn-On Delay Time			9.2		
Tr	Rise Time	V <sub>DD</sub> =-30V , V <sub>GS</sub> =-10V ,		20.1		
T <sub>d(off)</sub>	Turn-Off Delay Time	$R_G=3.3\Omega$ , $I_D=-1A$		46.7		ns
T <sub>f</sub>	Fall Time			9.4		<b>7</b>
C <sub>iss</sub>	Input Capacitance			1137		
Coss	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		76		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50		

### **Guaranteed Avalanche Characteristics**

Symbo	Parameter	Conditions	Min.	Тур.	Max.	Unit
EAS	Single Pulse Avalanche Energy <sup>5</sup>	V <sub>DD</sub> =-25V , L=0.1mH , I <sub>AS</sub> =-24A	13			mJ

## **Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current <sup>1,6</sup>	-V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-2.5	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,6</sup>				-10	Α
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25℃			-1.2	V

#### Note

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper,t<10sec.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =-25V,  $V_{GS}$ =-10V, L=0.1mH,  $I_{AS}$ =-24A
- 4.The power dissipation is limited by 150℃ junction temperature
- 5. The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



## **N-Channel Typical Characteristics**

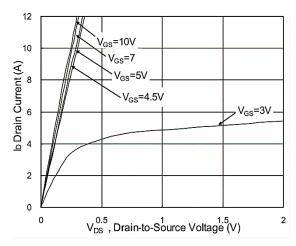


Fig.1 Typical Output Characteristics

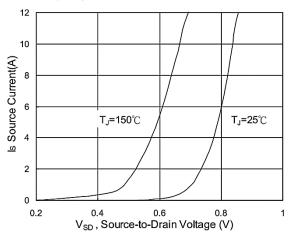


Fig.3 Source Drain Forward Characteristics

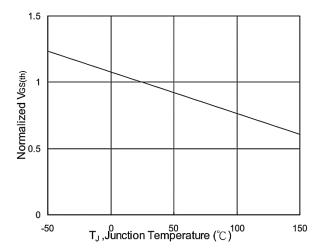


Fig.5 Normalized  $V_{\text{GS(th)}}$  vs.  $T_J$ 

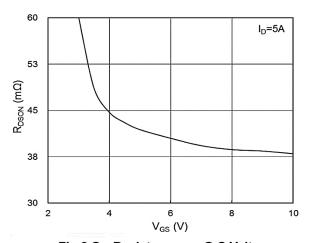


Fig.2 On-Resistance vs. G-S Voltage

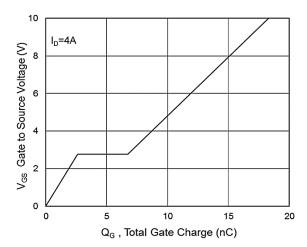


Fig.4 Gate-Charge Characteristics

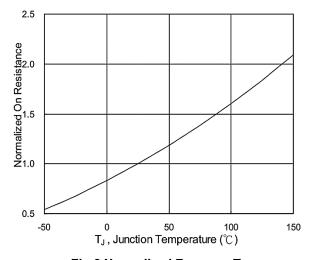
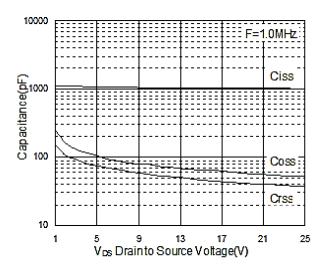


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>







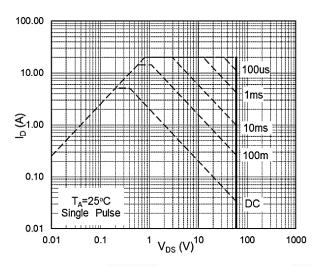


Fig.7 Capacitance

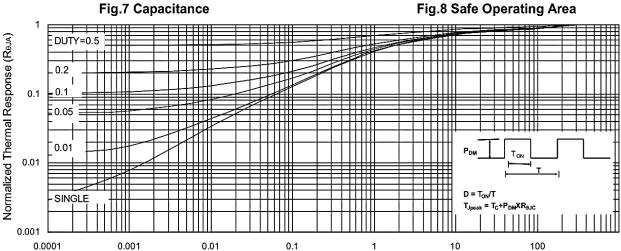


Fig.9 Normalized Maximum Transient Thermal Impedance

t, Pulse Width (s)

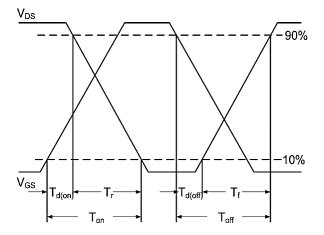


Fig.10 Switching Time Waveform

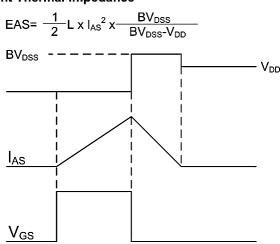


Fig.11 Unclamped Inductive Waveform



## **P-Channel Typical Characteristics**

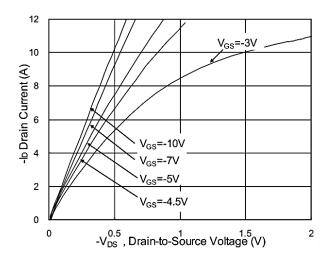


Fig.1 Typical Output Characteristics

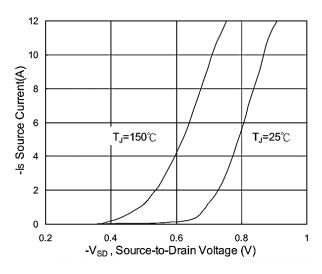


Fig.3 Source Drain Forward Characteristics

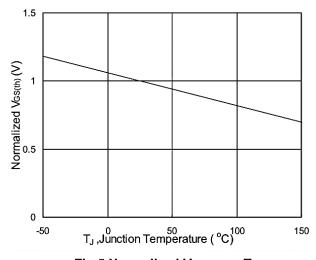


Fig.5 Normalized  $V_{\text{GS(th)}}$  vs.  $T_{\text{J}}$ 

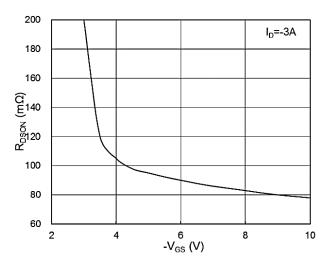


Fig.2 On-Resistance vs. G-S Voltage

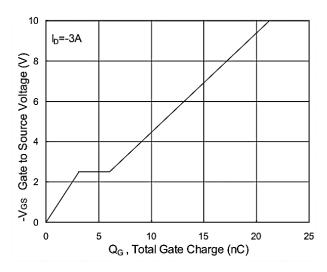


Fig.4 Gate-Charge Characteristics

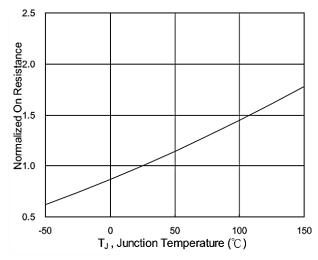
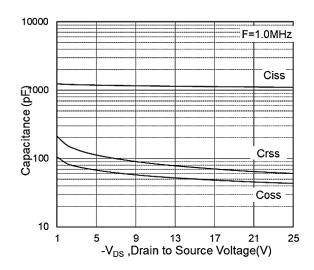


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>





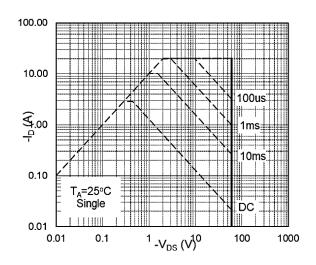


Fig.7 Capacitance

Fig.8 Safe Operating Area

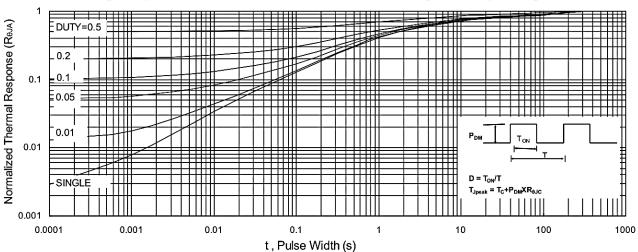


Fig.9 Normalized Maximum Transient Thermal Impedance

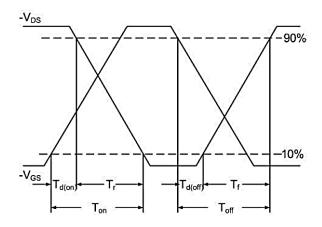


Fig.10 Switching Time Waveform

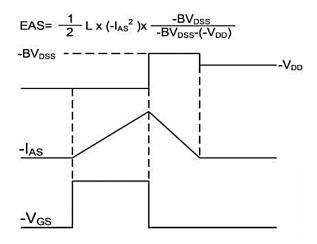


Fig.11 Unclamped Inductive Waveform



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DMN1006UCA6-7 DMN16M9UCA6-7 STF5N65M6 IRF40H233XTMA1 IPSA70R950CEAKMA1 IPSA70R2K0CEAKMA1 STU5N65M6
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