

General Description

The WST3400A is the highest performance trench N-Ch MOSFET with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the small power switching and load switch applications.

The WST3400A meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv/dt} effect decline
- Green Device Available

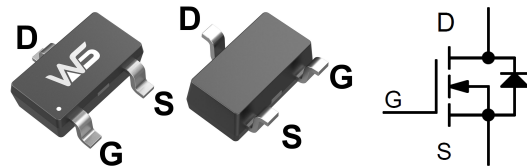
Product Summary

BVDSS	R _{DS(on)}	I _D
30V	20mΩ	6.4A

Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23-3L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V _{DS}	Drain-Source Voltage	30		V
V _{GS}	Gate-Source Voltage	±12		V
I _D @T _c =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	7.7	6.4	A
I _D @T _c =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	6.2	5.4	A
I _{DM}	Pulsed Drain Current ²	23		A
P _D @T _A =25°C	Total Power Dissipation ³	1.32	1	W
P _D @T _A =70°C	Total Power Dissipation ³	0.84	0.64	W
T _{STG}	Storage Temperature Range	-55 to 150		°C
T _J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	125	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	95	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	80	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.025	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =5A	---	20	31	mΩ
		V _{GS} =2.5V, I _D =4A	---	28	46	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	0.5	0.8	1.2	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.8	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =5A	---	7	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.5	5	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =5A	---	5.8	8.4	nC
Q _{gs}	Gate-Source Charge		---	2.4	3.5	
Q _{gd}	Gate-Drain Charge		---	2.0	2.9	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =10V, R _G =3.3Ω I _D =5A	---	2.3	4.8	ns
T _r	Rise Time		---	7.6	14	
T _{d(off)}	Turn-Off Delay Time		---	21	44	
T _f	Fall Time		---	3.8	8	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	520	880	pF
C _{oss}	Output Capacitance		---	72	112	
C _{rss}	Reverse Transfer Capacitance		---	56	91	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	1.8	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	22	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =5A, di/dt=100A/μs, T _J =25°C	---	18	---	nS
Q _{rr}	Reverse Recovery Charge		---	3	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper,t<10sec.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

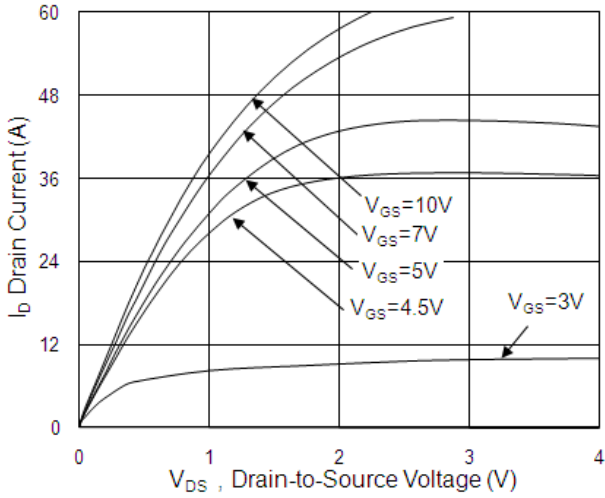


Fig.1 Typical Output Characteristics

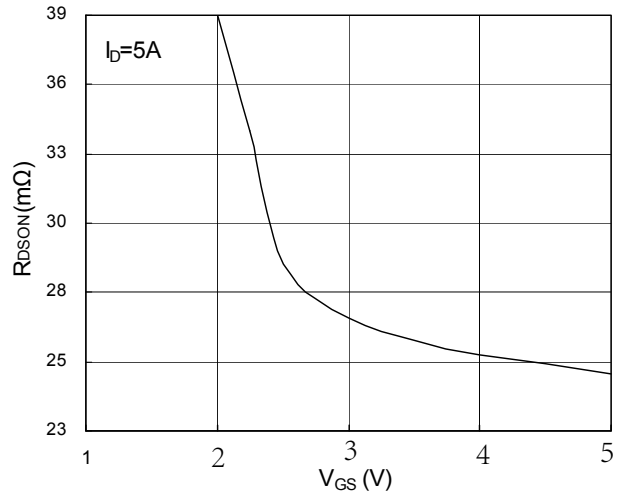


Fig.2 On-Resistance vs. Gate-Source

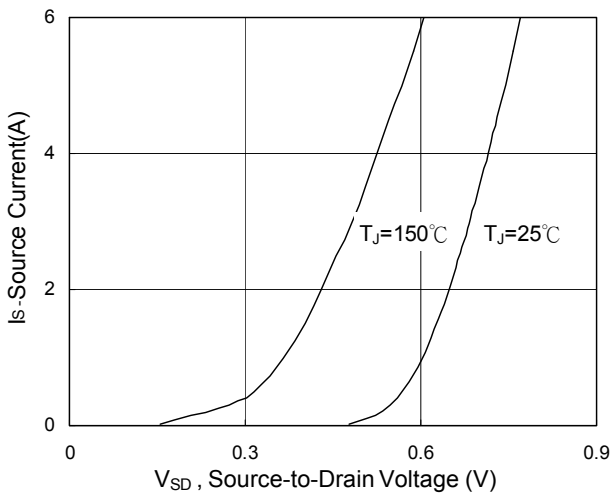


Fig.3 Forward Characteristics Of Reverse

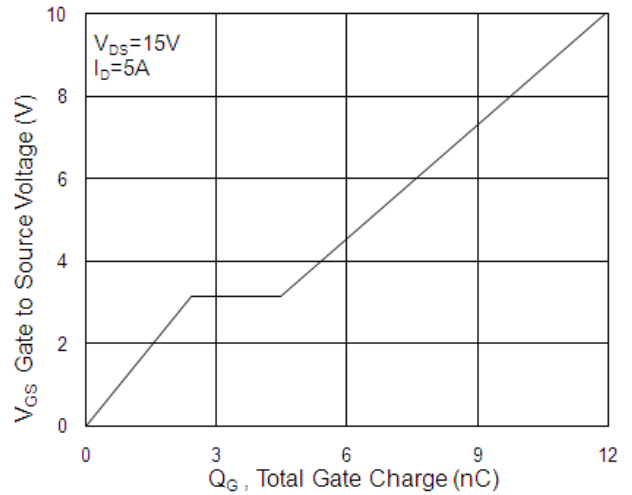


Fig.4 Gate-Charge Characteristics

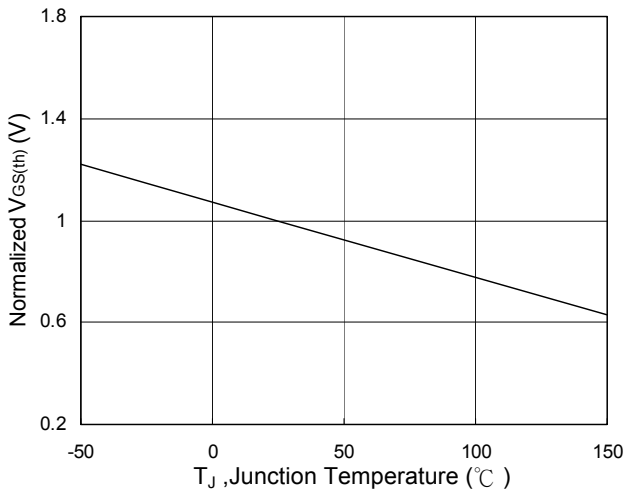


Fig.5 Normalized V_{GS(th)} vs. T_J

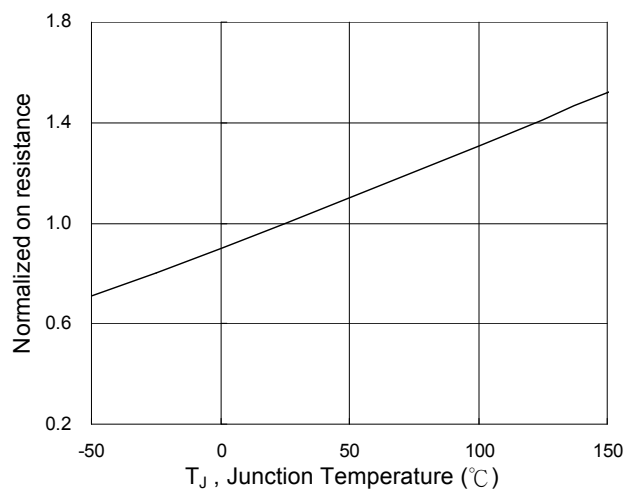


Fig.6 Normalized R_{DSON} vs. T_J

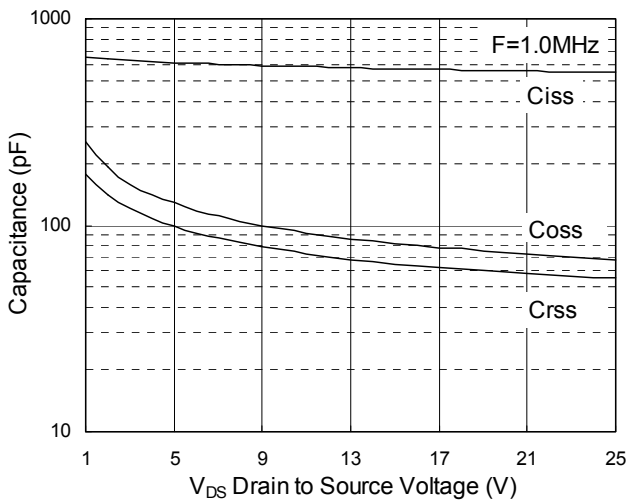


Fig.7 Capacitance

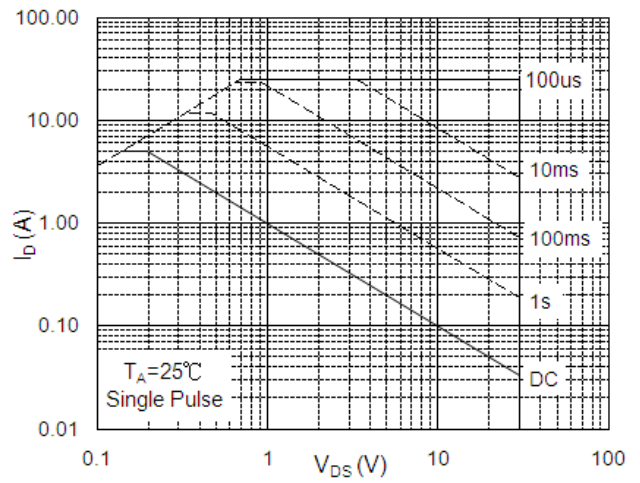


Fig.8 Safe Operating Area

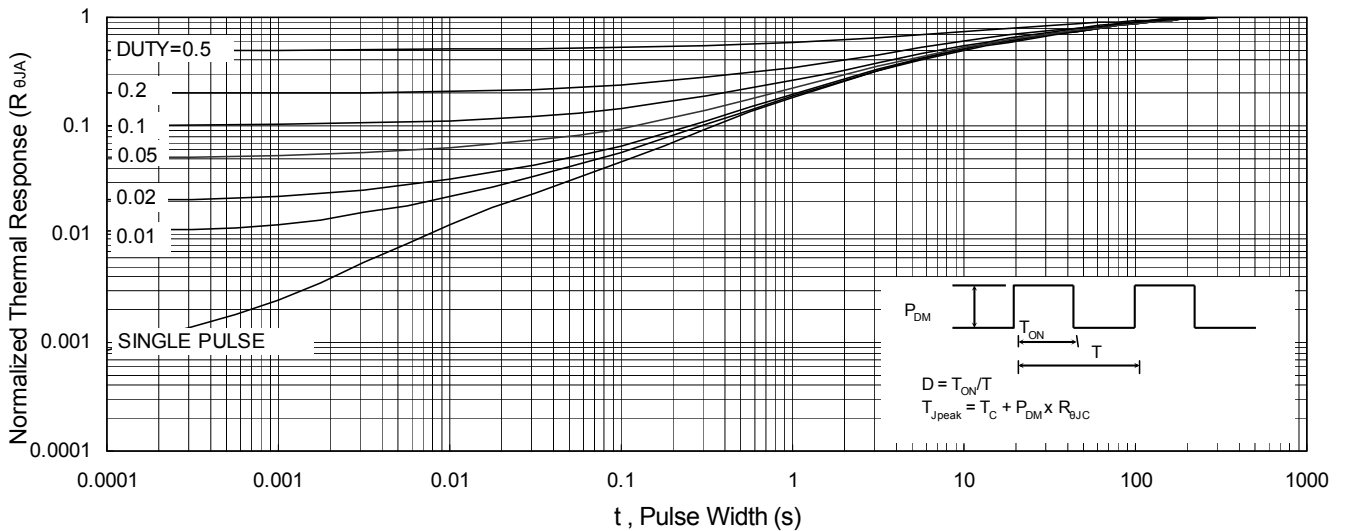


Fig.9 Normalized Maximum Transient Thermal Impedance

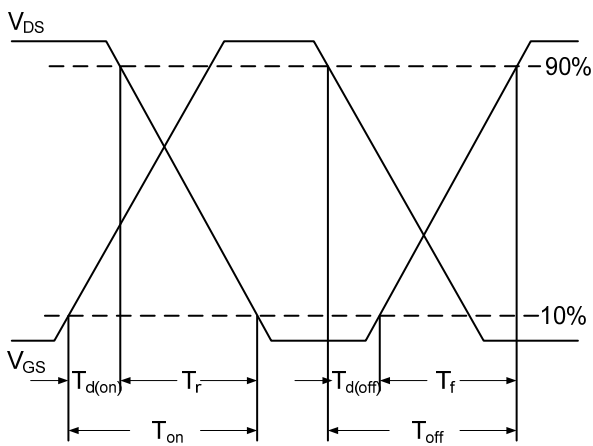


Fig.10 Switching Time Waveform

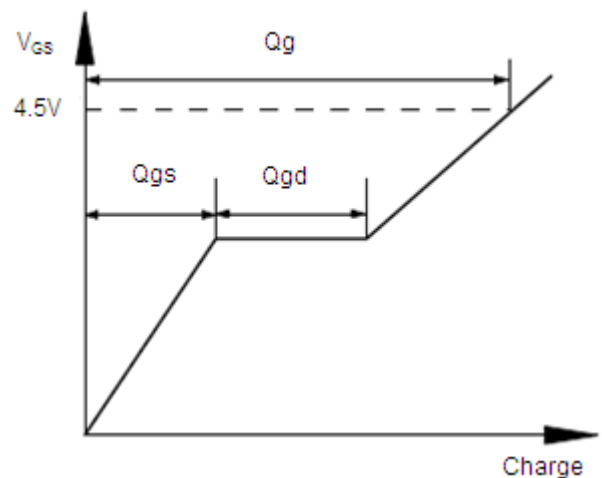


Fig.11 Gate Charge Waveform



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