

## **General Description**

The WST3423 is the highest performance trench P-ch MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST3423 meet the RoHS and Green Product requirement with full function reliability approved.

#### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

## **Product Summery**

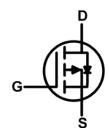
BVDSS	RDSON	ID
-20V	100mΩ	-2.9A

## **Applications**

- High Frequency Point-of-Load Synchronous s Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

# **SOT-23N Pin Configuration**





# **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units	
$V_{DS}$	Drain-Source Voltage	-20	V	
$V_{GS}$	Gate-Source Voltage	±12	V	
I <sub>D</sub> @T <sub>c</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-2.9	А	
I <sub>D</sub> @T <sub>c</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-1.9	А	
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-10	А	
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup>	1	W	
T <sub>STG</sub>	Storage Temperature Range -55 to 150		$^{\circ}$	
TJ	Operating Junction Temperature Range	-55 to 150	$^{\circ}$	

#### **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>		125	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case <sup>1</sup>		80	°C/W



# Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-20			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃ , I <sub>D</sub> =-1mA		-0.016		V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-2A		100	130	mΩ
		V <sub>GS</sub> =-2.5V , I <sub>D</sub> =-1A		145	170	
		V <sub>GS</sub> =-1.8V , I <sub>D</sub> =-1.5A		185	220	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-0.3	-0.5	-1	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient			3.97		mV/℃
	Drain Source Leakage Current	vent $V_{DS}$ =-16V , $V_{GS}$ =0V , $T_{J}$ =25°C $V_{DS}$ =-16V , $V_{GS}$ =0V , $T_{J}$ =55°C			-1	
I <sub>DSS</sub>	Drain-Source Leakage Current				-5	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm 8V$ , $V_{DS}$ = $0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-2A		5.9		S
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		13.1	26.2	Ω
Qg	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-15V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-2A		5.6	7.8	
Q <sub>gs</sub>	Gate-Source Charge			0.72	1.0	nC
Q <sub>gd</sub>	Gate-Drain Charge			1.45	2.0	
T <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD}$ =-15V , $V_{GS}$ =-4.5V , $R_{G}$ =3.3 $\Omega$ $I_{D}$ =-2A		4	8.0	
Tr	Rise Time			25.6	46	
T <sub>d(off)</sub>	Turn-Off Delay Time			26	52	ns
T <sub>f</sub>	Fall Time			12.4	24.8	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		332	465	
C <sub>oss</sub>	Output Capacitance			48	67	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			42	59	

## **Diode Characteristics**

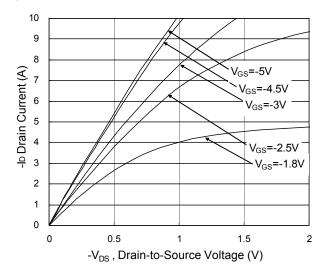
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current <sup>1,4</sup>	V =V =0V Force Current			-2.4	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-10	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25℃			-1.2	V
t <sub>rr</sub>	Reverse Recovery Time			23		nS
Q <sub>rr</sub>	Reverse Recovery Charge	lF=-2A , dl/dt=100A/µs , T <sub>J</sub> =25℃		4.7		nC

#### Note:

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, t<10 sec.
- 2.The data tested by pulsed , pulse width  $\,\leq\,300\text{us}$  , duty cycle  $\,\leq\,2\%$
- 3.The power dissipation is limited by 150  $^{\circ}\mathrm{C}$  junction temperature
- 4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



# **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

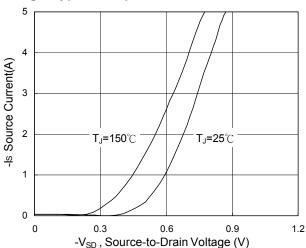


Fig.3 Forward Characteristics Of Reverse

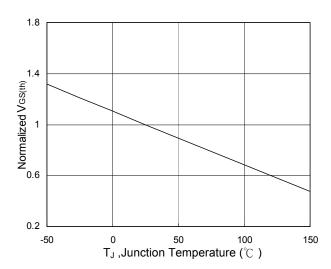


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

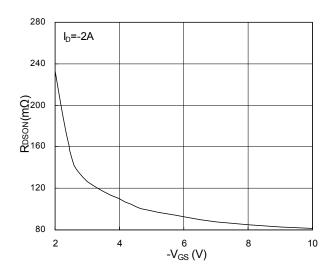


Fig.2 On-Resistance vs. Gate-Source

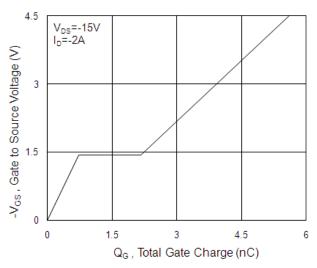


Fig.4 Gate-Charge Characteristics

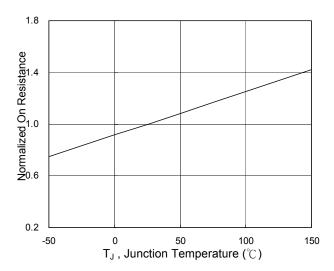
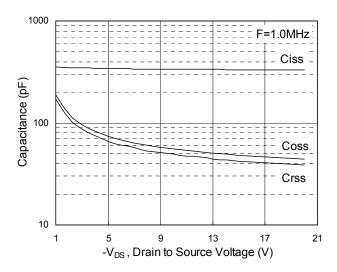


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>





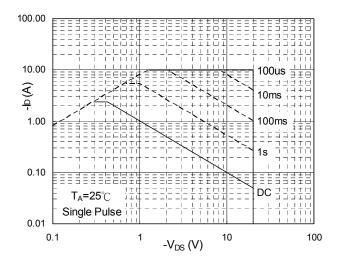


Fig.7 Capacitance

Fig.8 Safe Operating Area

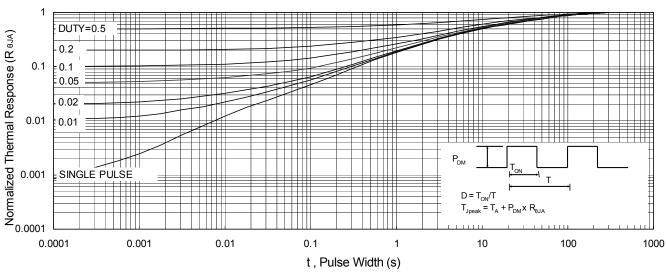


Fig.9 Normalized Maximum Transient Thermal Impedance

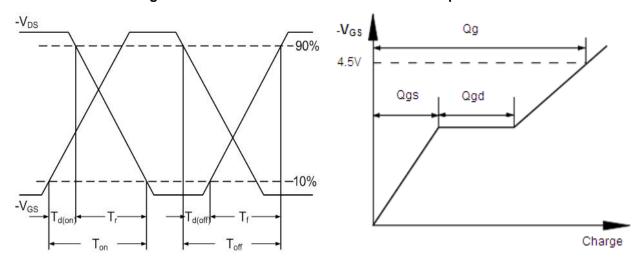


Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform



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