

W7500x Data Sheet

Version 1.0.8



<http://www.wiznet.co.kr>

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the W7500/W7500P microcontrollers.

This document should be read in conjunction with the W7500x reference manual (RM). The reference manual is available from the WIZnet website www.wizwiki.net.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The W7500x microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (128 Kbytes of Flash memory and 16Kbytes of SRAM), and TCP/IP offload engine, an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two SPIs and three UARTs), one 12-bit ADC, 4 general-purpose timers and eight advanced control PWM timer.

The W7500x microcontrollers operate in the 0 to +70 °C temperature range from a 2.7 to 3.6V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The W7500x microcontrollers include devices in two different packages from include PHY and non-include PHY.

These features make the W7500x microcontrollers suitable for a wide range of IoT applications such as application control and user interfaces.

Table 1. W7500/W7500P family device features and peripheral counts

| Peripherals | | W7500 | W7500P |
|------------------------|---------------|--|--|
| Flash memory in Kbytes | | 128 | |
| SRAM in Kbytes | | 16 | |
| Timers | RTC | 1 | |
| | Watch Dog | 1 | |
| | Dual Timer | 2 | |
| | PWM | up to 8 | |
| Comm | UART | up to 3 | |
| | SPI | up to 2 | |
| | TCP/IP Socket | 8 | |
| Internal PHY | | No | Yes |
| GPIOs | | 53 | 34 |
| 12-bit ADC | | up to 8 | |
| RNG | | 1 | |
| DMA channel | | 6 | |
| CPU frequency | | 48MHz | |
| Operating voltage | | 2.7 to 3.6V | |
| Operating temperatures | | Ambient temp : -40 to 85°C Junction temp : -30 to 105°C | Ambient temp : 0 to 70°C Junction temp : 0 to 105°C |
| Package | | LQFP64 | |

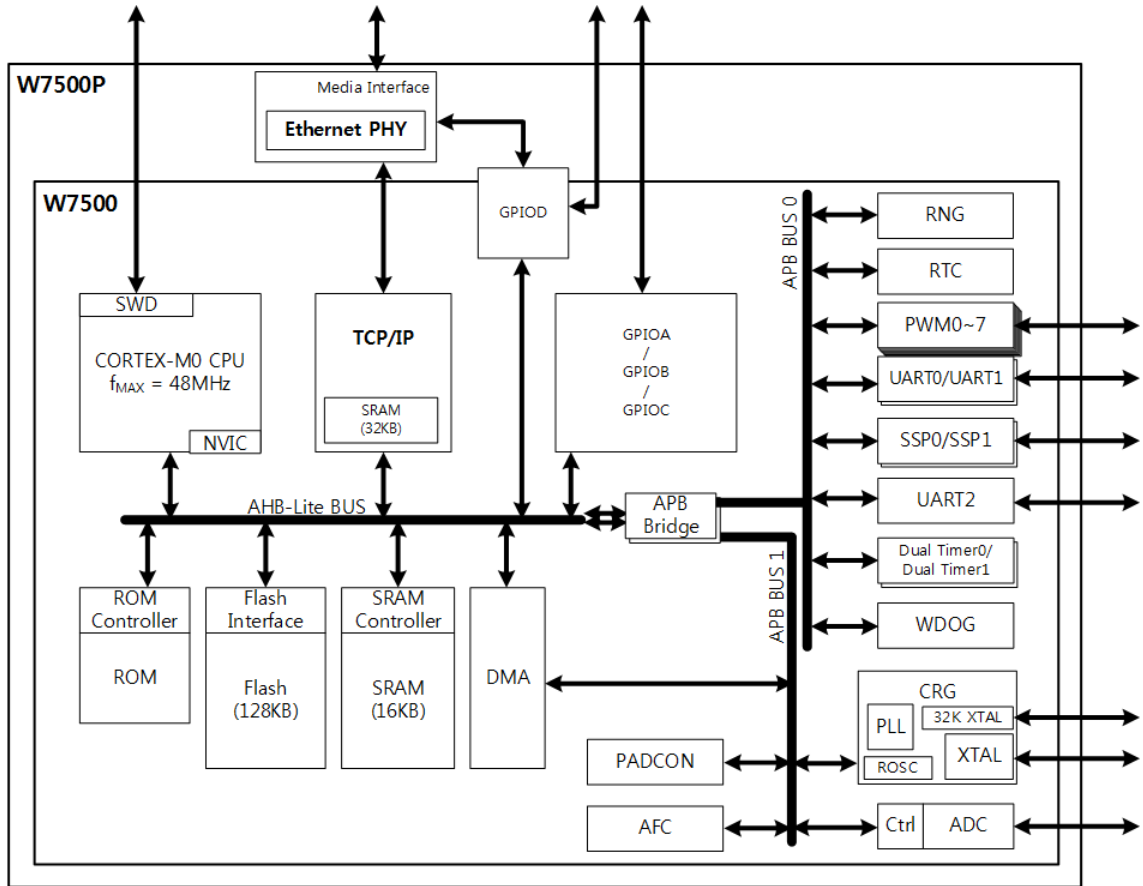


Figure 1. W7500x System Architecture

3 Functional overview

3.1 ARM®-Cortex®-M0 core with embedded Flash and SRAM

The ARM® Cortex®-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The W7500x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

- Figure 1 shows the general block diagram of the W7500x family.

3.2 Memories

Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

3.3 Boot modes

W7500x has three different boot modes that can be selected through the BOOT pin as shown in Table 2.

Table 2 operation of mode selection

| BOOT pin | Mode | Aliasing |
|----------|------|---|
| 0 | APP | User code execute in Main Flash memory. |
| 1 | ISP | In this mode, W7500x can support ISP function in order to control flash using serial interface. |

3.4 System configuration controller (SYSCFG)

Main purposes of the system configuration controller are the following

- The ability to enable an automatic reset if the system locks up
- Information about the cause of the last reset

3.5 Power management

3.5.1 Power supply schemes

W7500x embeds a voltage regulator in order to supply the internal 1.5V digital power domain. Require a 2.7V ~ 3.6V operating supply voltage (VDD). ADC ref voltage is same as VDD

3.5.2 Low-power modes

W7500x is in RUN mode after a system or power reset. There are two low power modes to save power when the CPU does not need to be kept running. These modes are useful for instances like when the CPU is waiting for an external interrupt. Please note that there is no power-off mode for W7500x.

The device features two low-power modes:

- Sleep mode
- Deep Sleep mode

Additionally, the power consumption can be reducing by following method:

User can slow down the system clocks

User can gate the clocks to the peripherals when they are unused.

Sleep mode / Deep sleep mode

W7500x has two kinds of sleep modes. One is Sleep mode and the other is Deep sleep mode. Two of them are almost the same except the clock gated peripherals kinds. Table 3 shows the Sleep mode summary.

Table 3 W7500x sleep mode summary

| Mode | Entry | Wakeup | Effect on clocks |
|-----------------|-----------------------------|---------------|--|
| Sleep mode | DEEPSLEEP = 0 Enable WFI | Any interrupt | CPU clock OFF APB Bus Clock ON AHB Bus clock ON Memory clocks ON |
| | DEEPSLEEP = 0 Enable WFE | Wakeup event | |
| Deep Sleep mode | DEEPSLEEP = 1 Enable WFI | Any interrupt | CPU clock OFF APB Bus Clock OFF AHB Bus clock OFF Memory clocks OFF |
| | DEEPSLEEP = 1 Enable WFE | Wakeup event | |

3.6 Clocks and startup

Two clock sources can be used to drive the system clock.

- External oscillator clock (8MHz ~ 24MHz) (OCLK)
- Internal 8MHz RC oscillator clock (RCLK)

One additional clock source

- 32.768KHz low speed external crystal which derives the real time clock.

There is a PLL

One PLL is integrated

- Input clock range is from 8MHz to 24MHz
- Frequency can be generated by M/N/OD registers. (refer register description)
- Bypass option enabled

There are many generated clocks for independent operating with system clock

- System clock (FCLK)
- ADC clock (ADCCLK)
- SSP0, SSP1 clock (SSPCLK)
- UART0, UART1 clock (UARTCLK)
- Two Timer clocks (TIMCLK0, TIMCLK1)
- 8ea PWM clocks (PWMCLK0 - PWMCLK7)
- Real time clock (RTCCLK)
- WDOG clock (WDOGCLK)
- Random number generator clock (RNGCLK)

RNGCLK have only one source (pll output) and no prescaler

Some of the generated clocks turn off automatically when CPU enters sleep mode.

- ADCCLK, RNGCLK

Generate two Hardware TCPIP Clocks (MII_RXC, MII_TXC) are from external PADs.

Hardware TCPIP Clocks can be gated by register control.

All clocks generated from CRG can be monitored.

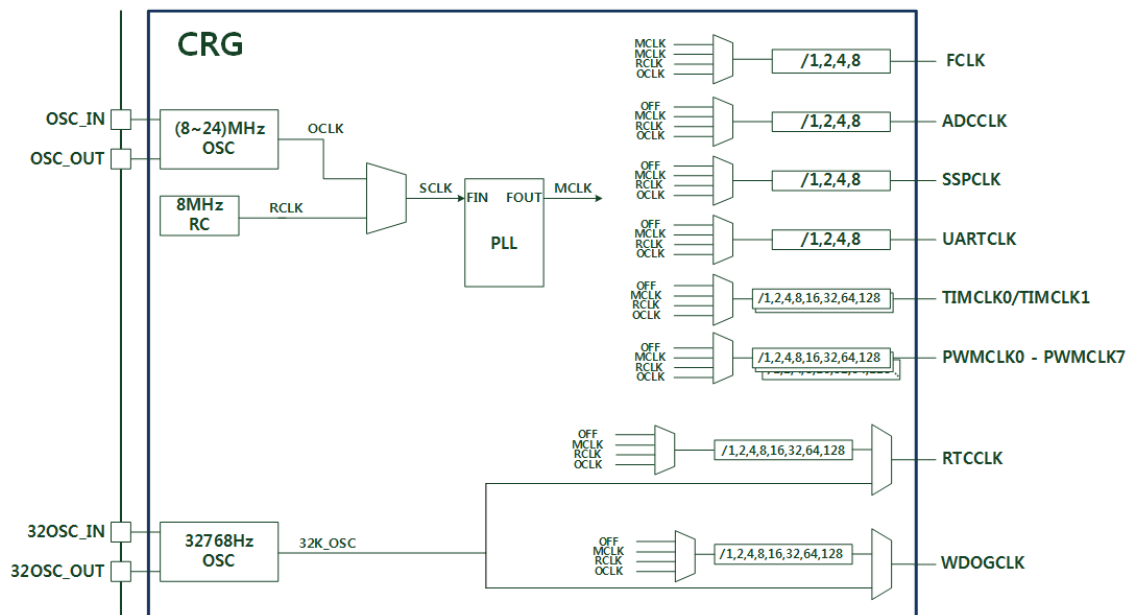


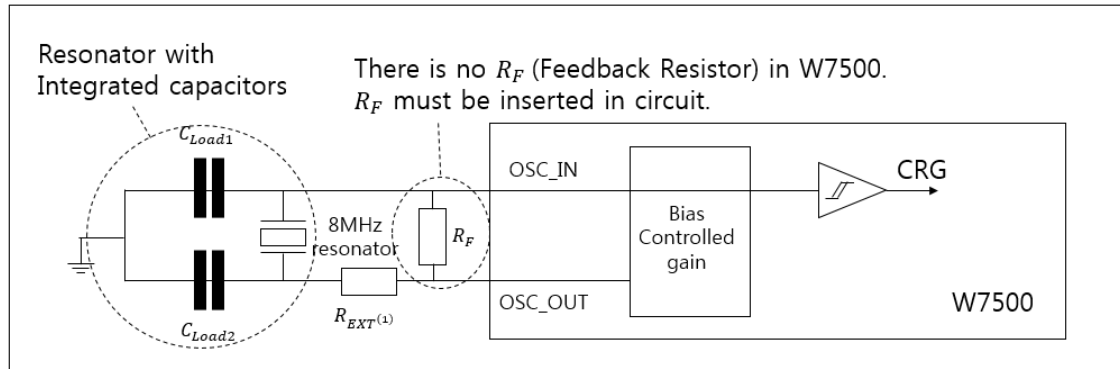
Figure 2. CRG block diagram

3.6.1 External Oscillator Clock

The External oscillator clock (OCLK) can be supplied with a 8 to 24 MHz crystal/ceramic resonator oscillator. In the Typical application, Figure 3, R_F must be inserted in External oscillator clock circuit. In W7500x, there is no supported R_F for External oscillator clock (see Figure 3).

For C_{Load1} and C_{Load2} , it is recommended to use external ceramic capacitors in the 5 pF to 25 pF range (typ.) and are usually the same size, designed for application, and selected to match the requirements of the crystal or resonator (see Figure 3).

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



¹ R_{EXT} value depends on the crystal characteristics

Figure 3 Typical application with an 8 MHz crystal

3.6.2 RC oscillator clock

RC oscillator clock (RCLK) signal is generated from an internal 8MHz RC oscillator. RC oscillator has the advantage of providing a clock source at low cost (no external components). However the RC oscillator is less accurate than the external crystal or ceramic resonator.

Accuracy : 1% at $T_A = 25^\circ\text{C}$ (User don't need to calibration)

3.6.3 PLL

The internal PLL can be used to multiply the External Oscillator Clock (OCLK) or RC Oscillator Clock (RCLK). PLL input can be selected by register.

PLL output clock can be generated by following the equations below.

- $F_{OUT} = F_{IN} \times M / N \times 1 / OD$

-

Where:

- $M = M[5] \times 2^5 + M[4] \times 2^4 + M[3] \times 2^3 + M[2] \times 2^2 + M[1] \times 2 + M[0] \times 1$
- $N = N[5] \times 2^5 + N[4] \times 2^4 + N[3] \times 2^3 + N[2] \times 2^2 + N[1] \times 2 + N[0] \times 1$
- $OD = 2^{(2 \times OD[1])} \times 2^{(1 \times OD[0])}$

3.6.4 Generated clock

Each generated clock source can be selected among 3 clock source as independent by each clock source select register.

- PLL output clock (MCLK)
- Internal 8MHz RC oscillator clock (RCLK)
- External oscillator clock (8MHz ~ 24MHz) (OCLK)

¹ R_{EXT} value depends on the crystal characteristics

- Each generated clock has own prescaler which can be selected individually by each prescale value register.
- FCLK, ADCCLK, SSPCLK, UARTCLK : 1/1, 1/2, 1/4, 1/8
- TIMCLK0, TIMCLK1, PWMCLK0 - PWMCLK7, RTCCLK, WDOGCLK : 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128

3.7 Interrupts and events

3.7.1 Nested vectored interrupt controller (NVIC)

The W7500x family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.7.2 Event controller

The W7500x family is able to handle internal events in order to wake up the core(WFE). The wakeup event can be generated by

- When after DMA process finished (DMA_DONE)

3.8 Tcp/ip offload engine (TOE)

The TCP/IP Core Offload Engine (TOE) is a Hardwired TCP/IP embedded Ethernet controller that provides easier Internet connection to embedded systems. TOE enables users to have Internet connectivity in their applications by using the TCP/IP stack.

WIZnet's Hardwired TCP/IP is the market-proven technology that supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. TOE embeds the 32Kbyte internal memory buffer for the Ethernet packet processing. Using TOE allows users to implement the Ethernet application by adding the simple socket program. It's faster and easier than using any other Embedded Ethernet solutions. 8 independent hardware sockets can be used simultaneously.

TOE also provides WOL (Wake on LAN) to reduce power consumption of the system.

- Supports Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Internal 32Kbytes Memory for TX/RX Buffers
- Not supports IP Fragmentation

3.9 General-purpose inputs/outputs (GPIOs)

The GPIO(General-Purpose I/O Port) is composed of three physical GPIO blocks, each corresponding to an individual GPIO port(PORT A, PORT B and PORT C). The GPIO supports up to 34 programmable input/output pins, depending on the peripherals being used.

- The GPIO peripheral consists the following features.
- GPIO_DATAOUT can SET/CLEAR by the SET register and CLEAR register. (1 for set and 0 for clear)
- Mask registers allow treating sets of port bits as a group leaving other bits unchanged.
- Up to 34 GPIOs depending on configuration
- Programmable control for GPIO interrupts
- Interrupt generation masking
- Edge-triggered on rising, falling, or both

Refer to 'Reference Manual' for more details about each register.

3.10 Pad controller (PADCON)

Pads of W7500x are controllable. User can control pad's characteristic.

W7500x has digital I/O pads and digital/analog mux I/O pads
 Controllable characteristics of pads are pull-up, pull-down, driving strength, input enable, and CMOS/Schmitt trigger input buffer
 Each pad can be controlled individually by register.

Figure 4 shows the function schematic of digital I/O pad of W7500x.

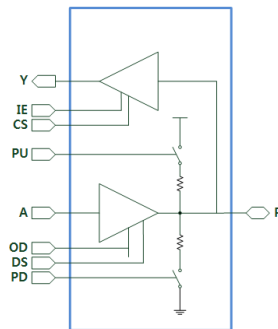


Figure 4. function schematic of digital I/O pad

Figure 5 shows the function schematic of digital/analog mux IO pad of W7500x

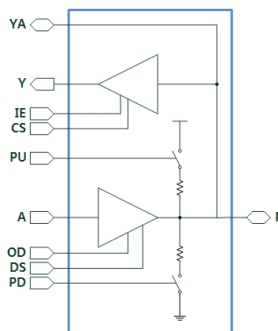


Figure 5. function schematic of digital/analog mux IO pad

Initials of Pad diagram is same as below.

- P - PAD
- A - Digital Output
- YA - Analog Input (connect to ADC input)
- Y - Digital Input
- IE - Input buffer enable

| Condition | | A | Y | P |
|----------------------------------|-------------|--------|---------|-----|
| Input buffer enable (IE = 1) | Output mode | OUT | OUT | OUT |
| | Input mode | No use | IN | IN |
| Input buffer disable (IE = 0) | Output mode | OUT | Low (0) | OUT |
| | Input mode | No use | IN | IN |

- CS - CMOS/Schmitt trigger input buffer select
- PU - Pull-up enable
- PD - Pull-down enable
- OD - Open Drain
- DS - Driving strength select

| Condition | | Rise/Fall Time (nSec) | | Propagation Delay (nSec) | |
|------------------|---------------------|-----------------------|-----|--------------------------|-----|
| Driving Strength | Capacitance loading | Min | Max | Min | Max |
| Low (DS = 1) | 25pF | 4 | 18 | 7 | 27 |
| | 100pF | 11 | 53 | 11 | 44 |
| High (DS = 0) | 25pF | 1 | 8 | 4 | 16 |
| | 100pF | 4 | 23 | 7 | 24 |

User can set pad condition with IE, CS, PU/PD, OD, DS by register. And pads are can be controlled individually.

3.11 Alternative function controller (AFC)

Each functional PADS have several functions.
Users can select a function in Alternate Function Controller block.

Each functional pad has 2 ~ 4 functions.
Pads can be selected by each registers individually.
Each pad can be used as an external interrupt source.

Table 4 shows the function table of each functional pad.

Table 4 functional description table

| Pins | | Pin name | Alternate function | | | |
|-------|--------|----------|--|-----------------------|-----------|-----------|
| W7500 | W7500P | | default | 2nd | 3rd | 4th |
| 29 | 27 | PA_00 | GPIOA_0 | GPIOA_0 | PWM6/CAP6 | |
| 30 | 28 | PA_01 | GPIOA_1 | GPIOA_1 | PWM7/CAP7 | |
| 31 | 29 | PA_02 | GPIOA_2 | GPIOA_2 | CLKOUT | |
| 49 | 30 | PA_03 | SWCLK | GPIOA_3 | | PWM0/CAP0 |
| 50 | 31 | PA_04 | SWDIO | GPIOA_4 | | PWM1/CAP1 |
| 33 | 19 | PA_05 | SSEL0 | GPIOA_5 | SCL1 | PWM2/CAP2 |
| 34 | 20 | PA_06 | SCLK0 | GPIOA_6 | SDA1 | PWM3/CAP3 |
| 35 | 21 | PA_07 | MISO0 | GPIOA_7 | U_CTS1 | PWM4/CAP4 |
| 36 | 22 | PA_08 | MOSI0 | GPIOA_8 | U_RTS1 | PWM5/CAP5 |
| 37 | 23 | PA_09 | SCL0 | GPIOA_9 | U_TXD1 | PWM6/CAP6 |
| 38 | 24 | PA_10 | SDA0 | GPIOA_10 | U_RXD1 | PWM7/CAP7 |
| 40 | 41 | PA_11 | U_CTS0 | GPIOA_11 | SSEL1 | |
| 41 | 42 | PA_12 | U_RTS0 | GPIOA_12 | SCLK1 | |
| 42 | 43 | PA_13 | U_TXD0 | GPIOA_13 | MISO1 | |
| 43 | 44 | PA_14 | U_RXD0 | GPIOA_14 | MOSI1 | |
| 44 | - | PA_15 | GPIOA_15 | GPIOA_15 | | |
| 45 | 45 | PB_00 | SSEL1 | GPIOB_0 | U_CTS0 | |
| 46 | 46 | PB_01 | SCLK1 | GPIOB_1 | U_RTS0 | |
| 47 | 47 | PB_02 | MISO1 | GPIOB_2 | U_TXD0 | |
| 48 | 48 | PB_03 | MOSI1 | GPIOB_3 | U_RXD0 | |
| 24 | - | PB_04 | TXEN | GPIOB_4 | | |
| 25 | - | PB_05 | COL | GPIOB_5 | | |
| 16 | 15 | PB_06 | RXD3 ¹⁾ / DUP ²⁾ | GPIOB_6 ¹⁾ | | |
| 17 | - | PB_07 | RXCLK | GPIOB_7 | | |

| | | | | | | |
|----|----|-------|-----------|----------|-------------------------|------|
| 18 | - | PB_08 | DUP | GPIOB_8 | | |
| 19 | - | PB_09 | TXCLK | GPIOB_9 | | |
| 20 | - | PB_10 | TXD0 | GPIOB_10 | | |
| 21 | - | PB_11 | TXD1 | GPIOB_11 | | |
| 22 | - | PB_12 | TXD2 | GPIOB_12 | | |
| 23 | - | PB_13 | TXD3 | GPIOB_13 | | |
| 26 | - | PB_14 | GPIOB_14 | GPIOB_14 | | |
| 27 | - | PB_15 | GPIOB_15 | GPIOB_15 | | |
| 53 | 53 | PC_00 | U_CTS1 | GPIOC_0 | PWM0/CAP0 | |
| 54 | 54 | PC_01 | U_RTS1 | GPIOC_1 | PWM1/CAP1 ¹⁾ | |
| 55 | 55 | PC_02 | U_TXD1 | GPIOC_2 | PWM2/CAP2 | |
| 56 | 56 | PC_03 | U_RXD1 | GPIOC_3 | PWM3/CAP3 ¹⁾ | |
| 57 | 57 | PC_04 | SCL1 | GPIOC_4 | PWM4/CAP4 | |
| 58 | 58 | PC_05 | SDA1 | GPIOC_5 | PWM5/CAP5 | |
| 51 | 11 | PC_06 | GPIOC_6 | GPIOC_6 | U_TXD2 | |
| 52 | - | PC_07 | GPIOC_7 | GPIOC_7 | U_RXD2 | |
| 1 | 1 | PC_08 | PWM0/CAP0 | GPIOC_8 | SCL0 | AIN7 |
| 2 | 2 | PC_09 | PWM1/CAP1 | GPIOC_9 | SDA0 | AIN6 |
| 3 | 3 | PC_10 | U_TXD2 | GPIOC_10 | PWM2/CAP2 | AIN5 |
| 4 | 4 | PC_11 | U_RXD2 | GPIOC_11 | PWM3/CAP3 | AIN4 |
| 5 | 5 | PC_12 | AIN3 | GPIOC_12 | SSEL0 | AIN3 |
| 6 | 6 | PC_13 | AIN2 | GPIOC_13 | SCLK0 | AIN2 |
| 7 | 7 | PC_14 | AIN1 | GPIOC_14 | MISO0 | AIN1 |
| 8 | 8 | PC_15 | AIN0 | GPIOC_15 | MOSIO | AIN0 |
| 11 | - | PD_00 | CRS | GPIOD_0 | | |
| 12 | - | PD_01 | RXDV | GPIOD_1 | | |
| 13 | - | PD_02 | RXD0 | GPIOD_2 | | |
| 14 | - | PD_03 | RXD1 | GPIOD_3 | | |
| 15 | - | PD_04 | RXD2 | GPIOD_4 | | |

1) Only W7500

2) Only W7500P

3.12 External interrupt (EXTI)

Each functional pads are connected to the external interrupt(EXTINT) source.

- All functional pads can be used as an external interrupt source regardless of any set of pad function.
- External Interrupt controller has the following functions and can be controlled by registers.
- Interrupt mask (enable or disable, default : disable)
- Interrupt polarity (rising or falling, default : rising)

All pads are connected to the control register individually. (External interrupt mask register and External Interrupt polarity register)

External interrupt working as following expression:

- Each pad interrupt = Interrupt mask & (Interrupt polarity ^ Pad input)
- EXTINT = any Each pad interrupt

Figure 6 shows the External Interrupt diagram.

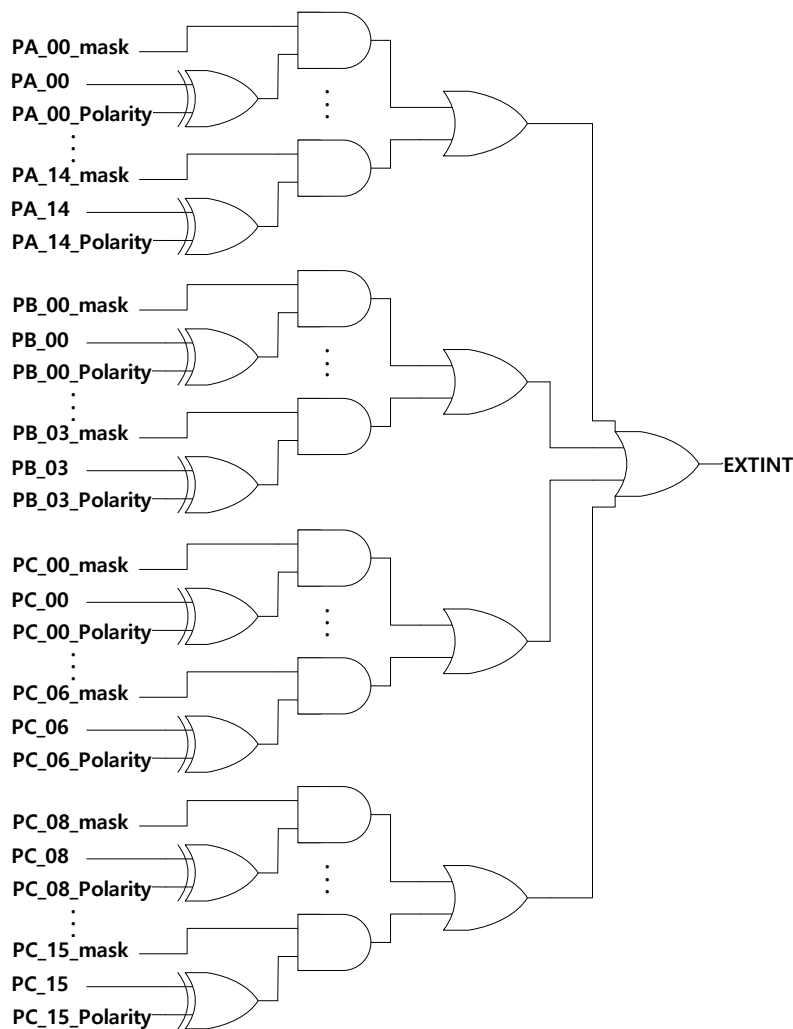


Figure 6. External Interrupt diagram

3.13 Direct memory access controller (DMA)

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The DMA controller has up to 6 channels in total, each dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests. For more details, refer to “PrimeCell® μ DMA Controller (PL230)” from the Technical Reference Manual

- 6 channels
- Each channel is connected to dedicated hardware DMA requests and software trigger is also supported on each channel.
- Priorities between requests from the DMA channels are software programmable (2 levels consisting of high, default)
- Memory-to-memory transfer (software request only)
- TCP/IP-to-memory transfer (software request only)
- SPI/UART-to-memory transfer (hardware request and software request)
- Access to Flash, SRAM, APB and AHB peripherals as source and destination

DMA request mapping

The hardware requests from the peripherals (UART0, UART1, SSP0, SSP1) are simply connected to the DMA. Refer to Table 5 which lists the DMA requests for each channel.

Table 5 Summary of the DMA requests for each channel

| | Channel 1 | Channel 2 | Channel 3 | Channel 4 | Channel 5 | Channel 6 |
|---------------------------------|--------------------|--------------------|----------------------|----------------------|-----------|-----------|
| Hardware Request | SSP0_TX SSP0_RX | SSP1_TX SSP1_RX | UART0_TX UART0_RX | UART1_TX UART1_RX | NONE | NONE |
| Software Request ⁽¹⁾ | Support | Support | Support | Support | Support | Support |

Software request is the only way to use DMA for memory-to-memory or TCP/IP-to-memory.

3.14 Analog to digital converter (ADC)

ADC is a 12bit analog-to-digital converter. It has up to 9 multiplexed channels allowing it to measure signals from 8 externals and 1 internal source.

ADC of various channels can be performed in single mode. The result of the ADC is stored in 12 bit register.

- 12bit configuration resolution
- Conversion time : Max 10MHz (Sampling time can be programmable)
- 8 channel for external analog inputs
- 1 channel for internal LDO(1.5v) voltage
- Start of conversion can be initiated by software.
- Convert selected inputs once per trigger.
- Interrupt generation at the end of conversion.

3.15 Timers and watchdogs

3.15.1 System tick timer

System tick timer(SysTick) is part of the ARM Cortex-M0 core

- Simple 24bit timer.
- Clocked internally by the system clock or the system clock/2.

The SysTick timer is an integral part of Cortex-M0. The SysTick timer is intended to generate a fixed 10 millisecond interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices.

The SysTick timer can be used for :

- An RTOS tick timer which fires at a programmable rate (for example 100 Hz) and invokes a SysTick routine.
- A high-speed alarm timer using the core clock.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

3.15.2 Pulse-Width Modulation (PWM)

The PWM consists a 8-channel 32-bit Timer/Counter driven by a programmable prescaler. The function of the PWM is based on the basic Timer. Each timer and counter runs independently.

The PWM can be used to control the width of the pulse, formally the pulse duration, to generate output waveform or to count the counter triggered by external input.

- Counter or Timer operation can use the peripheral clock, external clock source, or one of the capture inputs as the clock source.
- Eight independent 32-bit Timer/Counter driven by a programmable 6 bits prescaler runs as the PWM or standard timer if the PWM mode is not enabled.
- Eight PWM output waveforms.
- Each of Timer/Counter can have different or same clock source.
- Counter or timer operation.
- Eight capture registers that can take the timer value when an external input signal. A capture event can generate an interrupt signal optionally.
- 32-bit match register and limit register.

3.15.3 Dual timers

The dual timer consists two programmable 32-bit or 16-bit Free-running counters(FRCs) that can generate interrupts when they reach 0. There are two dual timers and 4 FRCs. One dual timer has one interrupt handler, resulting in two interrupts of timers. Also one dual timer has one clock but two clock enable signals. Users can select one repetition modes one-shot or wrapping mode, and wrapping mode consists free-running and periodic mode. Two FRCs are one set so two FRCs has one clock, reset, and interrupt but each FRC has an individual clock enable.

- One dual timer has two Free-Running Counters(FRCs).
- One dual timer has one interrupt handler and one clock.

- One dual timer has two clock enable signals.
- There are 2 dual timers.
- A 32-bit or a 16-bit down counter.
- One of the following repetition modes: one-shot and wrapping mode.
- One of the following wrapping modes: Free-running and periodic mode.
- There is a prescaler that can divide down the clock rate by 1, 16, or 256.

3.15.4 Watchdog timer

The watchdog is based on a 32-bit down-counter that is initialized from the Reload Register, WDTLoad. The watchdog generates a regular interrupt depending on a programmed value. The counter decreases by one on each positive clock edge of watchdog clock.

The watchdog monitors the interrupt and asserts a reset request signal when the counter reaches 0 and the counter is stopped. On the next enabled watchdog clock edge, the counter is reloaded from the WDTLoad Register and the countdown sequence continues. The watchdog reasserts the reset signal if the interrupt is not cleared by the time the counter next reaches 0.

The watchdog applies a reset to a system in the event of a software failure to provide a way to recover from software crashes. Users can enable or disable the watchdog unit as required.

- 32-bit down counter.
- Internally resets chip if not periodically reloaded.
- The watchdog timer has lock register to prevent rogue software from disabling the watchdog timer functionality.
- The watchdog timer clock(WDTCLK) and system clock(PCLK) are synchronous.

3.16 Real-time clock (RTC)

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a timer-of-day clock/calendar with programmable alarm interrupt.

Calendar with year, month, day, weekday, hours, minutes, and seconds
Programmable alarm with interrupt function

3.16.1 RTC clock

RTC Clock (RTCCLK) can be selected among several clocks (32768Hz oscillator, MCLK, RCLK, OCLK). Please refer to the Clock Reset Generator chapter for configuring the clock.

If the 32768Hz oscillator clock is used, the divider generates 1 Hz clock internally.

If the DIVRST (Bit[1] of RTC Control Register) value is high, the RTC Divider is cleared. If the DIVRST value is low, the divider operates.

3.16.2 RTC interrupt

RTC has two kinds of interrupt source, Counter Interrupt and Alarm Interrupt.

Interrupts are enabled in the NVIC using the appropriate Interrupt Set Enable register.

There are following Counter Interrupts: Second, Minute, Hour, Day (Day of Week), Date (Day of Month) and Year.

Each bit of RTCINTM (Interrupt Mask Register) can disable or enable interrupt for each Counter Interrupt.

Alarm Interrupt can be generated when the Alarm matches with Counter.

3.17 Universal asynchronous receiver/transmitter (UART)

The device embeds three universal asynchronous receivers/transmitters (UART0, UART1, UART2) which communicate at speeds of up to 3 Mbit/s.

The UART supports synchronous one-way communication, half-duplex single wire communication, and UART0,1 supports multiprocessor communications(CTS/RTS) but UART2 unsupported multiprocessor communications UART2 is called the SUART(Simple UART).

- Serial-to-parallel conversion on data received from a peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device
- Data size of 5,6,7 and 8 bits
- One or two stop bits
- Even, odd, stick, or no-parity bit generation and detection
- Support of hardware flow control
- Programmable FIFO disabling for 1-byte depth.
- Programmable use of UART or IrDA SIR input/output
- False start bit detection

UART bidirectional communication requires a minimum of two pins: RX, TX

The frame are comprised of:

- An Idle Line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- 1, 1.5, 2 Stop bits indicating that the frame is complete
- The USART interface uses a baud rate generator
- A status register (UART1_RISR)
- data registers (UART1DR)
- A baud rate register (UART1_IBRD,UART1_FBRD)

3.18 Synchronous Serial Port (SSP)

The SSP block is an IP provided by ARM (PL022 “PrimeCell® Synchronous Serial Port”). Additional details about its functional blocks may be found in “ARM PrimeCell® Synchronous Serial Port (PL022) Technical Reference Manual”.

- The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:
 - A MOTOROLA SPI-compatible interface
 - A TEXAS INSTRUMENTS synchronous serial interface
 - A National Semiconductor MICROWIRE® interface.
- The SPI interface operates as a master or slave interface. It supports bit rates up to 20 MHz in master mode and up to 4 MHz in slave mode.
- Parallel-to-serial conversion on data written to an internal 16-bit wide, 8-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 16-bit wide, 8-location deep receive FIFO
- Programmable data frame size from 4 to 16 bits
- Programmable clock bit rate and prescaler. The input clock may be divided by a factor of 2 to 254 in steps of two to provide the serial output clock
- Programmable clock phase and polarity.

3.19 Random number generator (RNG)

RNG is a 32bit random number generator. RNG generates power on random number when power on reset. RNG can run/stop by software. RNG seed value and polynomial of RNG can be modified by software.

- 32bit pseudo random number generator
- Formula of pseudo random number generator (polynomial) can be modified.
- Seed value of random generator can be modified.
- Support power on reset random value.
- Random value can be obtains by control start/stop by software.

4 Pinout and descriptions

4.1 Pin layout

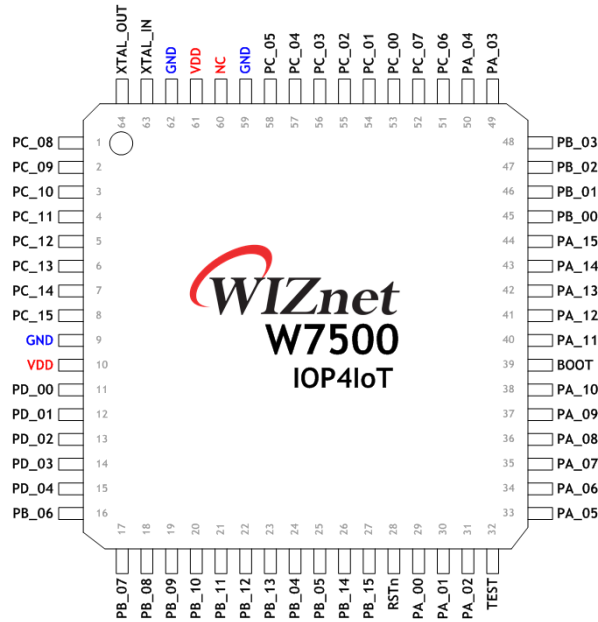


Figure 7 W7500 pin layout

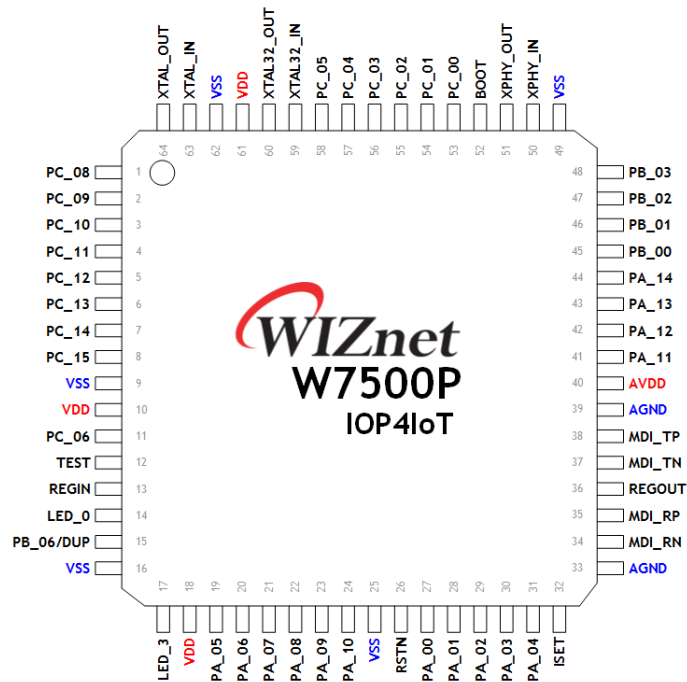


Figure 8 W7500P pin layout

4.2 Pin descriptions

4.2.1 W7500 Pin Description

Table 6. Pin Type Notation

| Type | Description |
|------|--------------|
| I | Input |
| O | Output |
| IO | Input/Output |
| A | Analog |
| PWR | Power |
| GND | Ground |

Table 7 W7500 Pin Description

| PIN No | Symbol | Type | Function | | | |
|--------|--------|------|---------------|--------------|--------------|--------------|
| | | | Main Function | 2nd Function | 3rd Function | 4th Function |
| 1 | PC_08 | AIO | PWM0/CAP0 | GPIO3_8 | SCL0 | AIN7 |
| 2 | PC_09 | AIO | PWM1/CAP1 | GPIO3_9 | SDA0 | AIN6 |
| 3 | PC_10 | AIO | U_TXD2 | GPIO3_10 | PWM2/CAP2 | AIN5 |
| 4 | PC_11 | AIO | U_RXD2 | GPIO3_11 | PWM3/CAP3 | AIN4 |
| 5 | PC_12 | AIO | AIN3 | GPIO3_12 | SSEL0 | AIN3 |
| 6 | PC_13 | AIO | AIN2 | GPIO3_13 | SCLK0 | AIN2 |
| 7 | PC_14 | AIO | AIN1 | GPIO3_14 | MISO0 | AIN1 |
| 8 | PC_15 | AIO | AIN0 | GPIO3_15 | MOSIO | AIN0 |
| 9 | GND | GND | GND | | | |
| 10 | VDD | PWR | VDD | | | |
| 11 | PD_00 | IO | CRS/TXD3 | GPIO4_0 | | |
| 12 | PD_01 | IO | RXDV/TXD2 | GPIO4_1 | | |
| 13 | PD_02 | IO | RXD0/TXD1 | GPIO4_2 | | |
| 14 | PD_03 | IO | RXD1/TXD0 | GPIO4_3 | | |
| 15 | PD_04 | IO | RXD2/TXCLK | GPIO4_4 | | |
| 16 | PB_06 | IO | RXD3/DUP | GPIO2_6 | | |
| 17 | PB_07 | IO | RXCLK/RXCLK | GPIO2_7 | | |
| 18 | PB_08 | IO | DUP/RXD3 | GPIO2_8 | | |
| 19 | PB_09 | IO | TXCLK/RXD2 | GPIO2_9 | | |

| PIN No | Symbol | Type | Function | | | |
|--------|--------|------|---------------|--------------|--------------|--------------|
| | | | Main Function | 2nd Function | 3rd Function | 4th Function |
| 20 | PB_10 | IO | TXD0/RXD1 | GPIO2_10 | | |
| 21 | PB_11 | IO | TXD1/RXD0 | GPIO2_11 | | |
| 22 | PB_12 | IO | TXD2/RXDV | GPIO2_12 | | |
| 23 | PB_13 | IO | TXD3/CRS | GPIO2_13 | | |
| 24 | PB_04 | IO | TXEN | GPIO2_04 | | |
| 25 | PB_05 | IO | COL | GPIO2_05 | | |
| 26 | PB_14 | IO | MDIO/MDC | GPIO2_14 | | |
| 27 | PB_15 | IO | MDC/MDIO | GPIO2_15 | | |
| 28 | RSTn | I | RSTn | | | |
| 29 | PA_00 | IO | GPIO1_0 | GPIO1_0 | PWM6/CAP6 | |
| 30 | PA_01 | IO | GPIO1_1 | GPIO1_1 | PWM7/CAP7 | |
| 31 | PA_02 | IO | GPIO1_2 | GPIO1_2 | CLKOUT | |
| 32 | TEST | IO | TEST | | | |
| 33 | PA_05 | IO | SSEL0 | GPIO1_5 | SCL1 | PWM2/CAP2 |
| 34 | PA_06 | IO | SCLK0 | GPIO1_6 | SDA1 | PWM3/CAP3 |
| 35 | PA_07 | IO | MISO0 | GPIO1_7 | U_CTS1 | PWM4/CAP4 |
| 36 | PA_08 | IO | MOSI0 | GPIO1_8 | U_RTS1 | PWM5/CAP5 |
| 37 | PA_09 | IO | SCL0 | GPIO1_9 | U_TXD1 | PWM6/CAP6 |
| 38 | PA_10 | IO | SDA0 | GPIO1_10 | U_RXD1 | PWM7/CAP7 |
| 39 | BOOT | IO | BOOT | | | |
| 40 | PA_11 | IO | U_CTS0 | GPIO1_11 | SSEL1 | |
| 41 | PA_12 | IO | U_RTS0 | GPIO1_12 | SCLK1 | |
| 42 | PA_13 | IO | U_TXD0 | GPIO1_13 | MISO11 | |
| 43 | PA_14 | IO | U_RXD0 | GPIO1_14 | MOSI1 | |
| 44 | PA_15 | IO | GPIO1_15 | GPIO1_15 | | |
| 45 | PB_00 | IO | SSEL1 | GPIO2_0 | U_CTS0 | |
| 46 | PB_01 | IO | SCLK1 | GPIO2_1 | U_RTS0 | |
| 47 | PB_02 | IO | MISO1 | GPIO2_2 | U_TXD0 | |

| PIN No | Symbol | Type | Function | | | |
|--------|----------|------|---------------|--------------|--------------|--------------|
| | | | Main Function | 2nd Function | 3rd Function | 4th Function |
| 48 | PB_03 | IO | MOSI1 | GPIO2_3 | U_RXD0 | |
| 49 | PA_03 | IO | SWCLK | GPIO1_3 | | PWM0/CAP0 |
| 50 | PA_04 | IO | SWDIO | GPIO1_4 | | PWM1/CAP1 |
| 51 | PC_06 | IO | GPIO3_6 | GPIO3_6 | U_TXD2 | |
| 52 | PC_07 | IO | GPIO3_7 | GPIO3_7 | U_RXD2 | |
| 53 | PC_00 | IO | U_CTS1 | GPIO3_0 | PWM0/CAP0 | |
| 54 | PC_01 | IO | U_RTS1 | GPIO3_1 | PWM1/CAP1 | |
| 55 | PC_02 | IO | U_TXD1 | GPIO3_2 | PWM2/CAP2 | |
| 56 | PC_03 | IO | U_RXD1 | GPIO3_3 | PWM3/CAP3 | |
| 57 | PC_04 | IO | SCL1 | GPIO3_4 | PWM4/CAP4 | |
| 58 | PC_05 | IO | SDA1 | GPIO3_5 | PWM5/CAP5 | |
| 59 | GND | GND | GND | | | |
| 60 | NC | NC | NC | | | |
| 61 | VDD | PWR | VDD | | | |
| 62 | GND | GND | GND | | | |
| 63 | XTAL_IN | I | Xtal in | | | |
| 64 | XTAL_OUT | O | Xtal out | | | |

4.2.2 W7500P Pin Description

Table 8. W7500P Pin Description

| PIN No | Symbol | Type | Function | | | | |
|--------|-----------|------|---------------|--------------|--------------|--------------|-------|
| | | | Main Function | 2nd Function | 3rd Function | 4th Function | PHY |
| 1 | PC_08 | AIO | PWM0/CAP0 | GPIO3_8 | SCL0 | AIN7 | |
| 2 | PC_09 | AIO | PWM1/CAP1 | GPIO3_9 | SDA0 | AIN6 | |
| 3 | PC_10 | AIO | U_TXD2 | GPIO3_10 | PWM2/CAP2 | AIN5 | |
| 4 | PC_11 | AIO | U_RXD2 | GPIO3_11 | PWM3/CAP3 | AIN4 | |
| 5 | PC_12 | AIO | AIN3 | GPIO3_12 | SSEL0 | AIN3 | |
| 6 | PC_13 | AIO | AIN2 | GPIO3_13 | SCLK0 | AIN2 | |
| 7 | PC_14 | AIO | AIN1 | GPIO3_14 | MISO0 | AIN1 | |
| 8 | PC_15 | AIO | AIN0 | GPIO3_15 | MOSIO | AIN0 | |
| 9 | VSS | GND | VSS | | | | |
| 10 | VDD | PWR | VDD | | | | |
| 11 | PC_06 | IO | GPIO3_6 | GPIO3_6 | U_TXD2 | | |
| 12 | TEST | IO | TEST | | | | |
| 13 | REGIN | PWR | REGIN | | | | |
| 14 | LED_0 | IO | LED_0 | | | | LED_0 |
| 15 | PB_06/DUP | IO | DUP | | | | DUP |
| 16 | VSS | IO | VSS | | | | |
| 17 | LED_3 | IO | LED_3 | | | | LED_3 |
| 18 | VDD | PWR | VDD_IO | | | | |
| 19 | PA_05 | IO | SSEL0 | GPIO1_5 | SCL1 | PWM2/CAP2 | |
| 20 | PA_06 | IO | SCLK0 | GPIO1_6 | SDA1 | | |
| 21 | PA_07 | IO | MISO0 | GPIO1_7 | U_CTS1 | PWM4/CAP4 | |
| 22 | PA_08 | IO | MOSIO | GPIO1_8 | U_RTS1 | PWM5/CAP5 | |
| 23 | PA_09 | IO | SCL0 | GPIO1_9 | U_TXD1 | PWM6/CAP6 | |
| 24 | PA_10 | IO | SDA0 | GPIO1_10 | U_RXD1 | PWM7/CAP7 | |
| 25 | VSS | IO | VSS_IO | | | | |
| 26 | RSTN | I | RSTN | | | | |

| PIN No | Symbol | Type | Function | | | | |
|--------|----------|------|----------------|--------------|--------------|--------------|--------|
| | | | Main Function | 2nd Function | 3rd Function | 4th Function | PHY |
| 27 | PA_00 | IO | GPIO1_0 | GPIO1_0 | PWM6/CAP6 | | |
| 28 | PA_01 | IO | GPIO1_1 | GPIO1_1 | PWM7/CAP7 | | |
| 29 | PA_02 | IO | GPIO1_2 | GPIO1_2 | CLKOUT | | |
| 30 | PA_03 | IO | GPIO1_3 | GPIO1_3 | | PWM0/CAPO | |
| 31 | PA_04 | IO | GPIO1_4 | GPIO1_4 | | | |
| 32 | ISET | I | ISET | | | | ISET |
| 33 | AGND | GND | AGND | | | | |
| 34 | MDI_RN | IO | MDI_RN | | | | MDI_RN |
| 35 | MDI_RP | IO | MDI_RP | | | | MDI_RP |
| 36 | REGOUT | PWR | REGOUT | | | | |
| 37 | MDI_TN | IO | MDI_TN | | | | MDI_TN |
| 38 | MDI_TP | IO | MDI_TP | | | | MDI_TP |
| 39 | AGND | GND | AGND | | | | |
| 40 | AVDD | PWR | AVDD | | | | |
| 41 | PA_11 | IO | U_CTS0 | GPIO1_11 | SSEL1 | | |
| 42 | PA_12 | IO | U_RTS0 | GPIO1_12 | SCLK1 | | |
| 43 | PA_13 | IO | U_TXD0 | GPIO1_13 | MISO1 | | |
| 44 | PA_14 | IO | U_RXD0 | GPIO1_14 | MOSI1 | | |
| 45 | PB_00 | IO | SSEL1 | GPIO2_0 | U_CTS0 | | |
| 46 | PB_01 | IO | SCLK1 | GPIO2_1 | U_RTS0 | | |
| 47 | PB_02 | IO | MISO1 | GPIO2_2 | U_TXD0 | | |
| 48 | PB_03 | IO | MOSI1 | GPIO2_3 | U_RXD0 | | |
| 49 | VSS | PWR | VSS_IO | | | | |
| 50 | XPHY_IN | I | 25MHz xtal in | | | | |
| 51 | XPHY_OUT | O | 25MHz xtal out | | | | |
| 52 | BOOT | IO | BOOT | | | | |
| 53 | PC_00 | IO | U_CTS1 | GPIO3_0 | PWM0/CAPO | | |
| 54 | PC_01 | IO | U_RTS1 | GPIO3_1 | | | |

| PIN No | Symbol | Type | Function | | | | |
|--------|------------|------|---------------------|--------------|--------------|--------------|-----|
| | | | Main Function | 2nd Function | 3rd Function | 4th Function | PHY |
| 55 | PC_02 | IO | U_TXD1 | GPIO3_2 | PWM2/CAP2 | | |
| 56 | PC_03 | IO | U_RXD1 | GPIO3_3 | | | |
| 57 | PC_04 | IO | SCL1 | GPIO3_4 | PWM4/CAP4 | | |
| 58 | PC_05 | IO | SDA1 | GPIO3_5 | PWM5/CAP5 | | |
| 59 | XTAL32_IN | I | 32768Hz xtal in | | | | |
| 60 | XTAL32_OUT | O | 32768Hz xtal out | | | | |
| 61 | VDD | PWR | VDD | | | | |
| 62 | VSS | GND | VSS | | | | |
| 63 | XTAL_IN | I | Xtal in | | | | |
| 64 | XTAL_OUT | O | Xtal out | | | | |

5 Electrical characteristics

5.1 Absolute maximum ratings

These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.2 Voltage Characteristics

Table 9 shows the voltage characteristics of W7500x.

Table 9 Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|-----------------|--|----------------|---------|------|
| $V_{DD}-V_{SS}$ | Main supply voltage (VDD) | -0.3 | 3.6 | V |
| V_{IN} | Input voltage on IO pins | $V_{SS} - 0.3$ | 3.6 | V |
| S_{VDDH} | I/O Power on slope | 3.3V/Sec | 1V/uSec | - |
| ΔV_{DD} | Variations between difference VDD power pins | | 50 | mV |
| ΔV_{SS} | Variations between different ground pins | | 50 | mV |

5.3 Current Characteristics

Table 10 shows the current characteristics of W7500x.

Table 10 Current characteristics

| Symbol | Ratings | Max | Unit |
|----------------|--|----------|------|
| I_{VDD_SUM} | Total current into sum of all VDD power lines (source) | 100 | mA |
| I_{VDD} | Maximum current into each ADD power pin (source) | 90 | mA |
| I_{IO_PAD} | Total output current sunk by sum of all IOs and control pins | 75 | mA |
| I_{INJ_PAD} | Single pin input injected current | ± 10 | mA |
| I_{INJ_SUM} | Sum of all input injected current | ± 50 | mA |

5.4 Thermal Characteristics

Table 11 shows the thermal characteristics of W7500x.

Table 11 Thermal Characteristics

| Symbol | Ratings | | Min | Max | Unit |
|---------------|---|--------|-----|-----|------|
| $T_{Storage}$ | Storage temperature range | | -55 | 150 | °C |
| T_{Junc} | Maximum junction temperature under bias | W7500 | -40 | 150 | |
| | | W7500P | 0 | 125 | |
| T_A | Ambient Operating Temperature | W7500 | -40 | 85 | |
| | | W7500P | 0 | 70 | |

5.5 Operating conditions

5.5.1 General Operating Conditions

Table 12 shows the general operating conditions of W7500x.

Table 12 General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|------------------------------|------------|--------------|-----|------|
| f_{CLK} | Internal CPU clock frequency | | 0 | 48 | MHz |
| V_{DD} | Standard operating voltage | | 2.7 | 3.6 | V |
| V_{IO} | Input voltage on PIN | | $V_{SS}-0.3$ | 3.6 | V |

5.6 Supply Current Characteristics

Normal operation

Table 13 shows the Normal operation supply current.

Table 13 Normal operation supply current

| Symbol | Parameter | Conditions1 | Condition2 | Typ | Unit |
|---------------------|----------------|--|----------------------|---|------|
| I _{DD_NOR} | Supply current | Active mode; code While(1) {} Executed from flash memory | System clock = 10MHz | 6.14 (52.14) ⁽¹⁾ (22.14) ⁽²⁾ | mA |
| | | | System clock = 20MHz | 8.82 (54.82) ⁽¹⁾ (24.82) ⁽²⁾ | mA |
| | | | System clock = 40MHz | 14.09 (60.09) ⁽¹⁾ (30.09) ⁽²⁾ | mA |

(1) When PHY Normal mode, W7500P Internal PHY power consumption is 46mA MAX.

(2) When PHY Power down mode, W7500P Internal PHY power consumption is 16mA MAX.

Sleep mode

Table 14 shows the Normal operation supply current.

Table 14 Sleep mode supply current

| Symbol | Parameter | Conditions1 | Condition2 | Typ | Unit |
|---------------------|----------------|--|----------------------|--|------|
| I _{DD_SLP} | Supply current | After enter sleep mode All peripheral clocks ON (same as system clock) | System clock = 10MHz | 3.51 (49.51) ⁽¹⁾ (19.51) ⁽²⁾ | mA |
| | | | System clock = 20MHz | 5.65 (51.65) ⁽¹⁾ (21.65) ⁽²⁾ | mA |
| | | | System clock = 40MHz | 9.61 (55.61) ⁽¹⁾ (25.61) ⁽²⁾ | mA |

(3) When PHY Normal mode, W7500P Internal PHY power consumption is 46mA MAX.

(4) When PHY Power down mode, W7500P Internal PHY power consumption is 16mA MAX.

Deep sleep mode

Table 15 shows the deep sleep mode operation supply current.

Table 15 Deep sleep mode supply current

| Symbol | Parameter | Conditions1 | Condition2 | Typ | Unit |
|----------------------|----------------|---|------------|--|------|
| I _{DD_DSLP} | Supply current | After enter deep sleep mode All peripheral clocks OFF | - | 2.49 (48.49) ⁽¹⁾ (18.49) ⁽²⁾ | mA |

(5) When PHY Normal mode, W7500P Internal PHY power consumption is 46mA MAX.

(6) When PHY Power down mode, W7500P Internal PHY power consumption is 16mA MAX.

5.7 I/O PAD Characteristics

DC Specification

Table 16 shows the DC specification of W7500x I/O PAD.

Table 16 DC specification of PAD

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------------------------|-----------------------------|---|-------|-------|------|
| V _{IH} | I/O Input high voltage | | 2.145 | | V |
| V _{IL} | I/O Input low voltage | | | 1.155 | V |
| V _{HYS} | Schmitt trigger hysteresis | | 0.33 | | V |
| I _{IH} | I/O Input high current | | | 1 | uA |
| I _{IL} | I/O Input low current | | -1 | | uA |
| V _{OH} | I/O Output high voltage | High driving strength Iload = 6mA Low driving strength Iload = 3mA | 2.5 | | V |
| V _{OL} | I/O Output low voltage | High driving strength Iload = 6mA Low driving strength Iload = 3mA | | 0.5 | V |
| R _{pup} R _{pdn} | Pull-up /Pull-down resistor | | 20 | 100 | KOhm |

Flash memory

Table 17 shows the flash memory reliability characteristics of W7500x

Table 17 Flash memory Reliability Characteristics

| Symbol | Parameter | Min | Unit |
|------------------|------------------|--------|--------|
| N _{END} | Sector Endurance | 10,000 | Cycles |
| T _{DR} | Data Retention | 10 | Years |

5.8 Electrical Sensitivity Characteristics

Electrostatic discharge (ESD)

Table 18 shows the ESD information of W7500x

Table 18 Electrostatic discharge (ESD)

| Symbol | Parameter | Test Method | Min | Max | Unit |
|-----------------------|---|--------------|-------|-----|------|
| V _{ESD(HBM)} | Electrostatic discharge (Human body model) | AEC-Q100-002 | ±2000 | - | V |
| V _{ESD(CDM)} | Electrostatic discharge (Charge device model) | AEC-Q100-011 | ±500 | - | V |

Static latch-up

Table 19 shows the Static latch-up information of W7500x

Table 19 Static latch-up

| Symbol | Parameter | Test Method | Min | Max | Unit |
|------------------|--|--------------|------|-----|------|
| I _{LAT} | Latch up current at 125 °C ambient temperature | AEC-Q100-004 | ±100 | - | V |

5.9 Reset & PLL Characteristics

PLL Electrical characteristics

Table 20 shows the PLL characteristics of W7500x

Table 20 PLL electrical characteristics

| Symbol | Parameter | Min | Max | Unit |
|------------|-----------------------|-----|-----|------|
| t_d | RSTn to PD delay time | 5 | - | us |
| t_{rst} | Reset pulse width | 2 | - | us |
| t_{lock} | Lock time | - | 0.2 | ms |

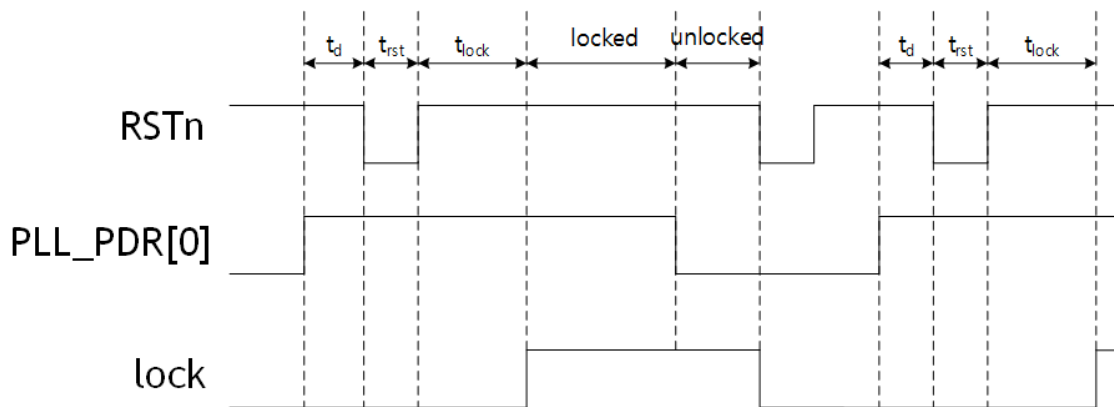


Figure 9 Power Down operation Timing Sequence for PLL

Notice:

PLL_PDR[0] is LSB of PLL_PDR. please refer from Reference Manual.

lock signal is internal signal.

1, t_d is the RSTn to PLL_PDR[0] delay time, which need larger than 5us.

2, t_{rst} is the reset pulse width, which need larger than 2us.

3, t_{lock} is the lock time, which is less than 0.2ms.

4, When PLL_PDR[0] changes from "1" to "0", the lock signal stays in "1" until a reset pulse comes. But the PLL is in unlocked state during this period.

5.10 ADC Characteristics

ADC Electrical characteristics

Table 21 shows the ADC electrical characteristics of W7500x

Table 21 ADC electrical characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|------------------------------------|------------|-------------|-----------|-------|-------------|
| IN[15:0] | Analog input channel | | V_{SS} | - | VREFP | V |
| VREFP | Reference voltage of REFP | | | V_{DD} | | V |
| RES | Resolution | | | 12 | | Bits |
| Offset error | | | -3.0 | ± 1.5 | 3.0 | LSB |
| INL | Integral non-linearity error | | -2.0 | ± 1.0 | 2.0 | LSB |
| DNL | Differential non-linearity error | | -1.0 | ± 0.8 | 1.5 | LSB |
| Fclk | Clock frequency | | | | 16 | MHz |
| SPS | Sampling rate | | 30 | 500 | 1000 | K |
| TS | Sampling time | | $4/F_{clk}$ | | | |
| TC | Conversion time | | | 12 | | $1/F_{clk}$ |
| SNDR | Signal-noise plus distortion ratio | At 10KHz | | 64 | | dB |
| THD | Total harmonic distortion | At 10KHz | | -65 | | dB |
| SFDR | Spurious-free dynamic range | At 10KHz | | 64 | | dB |

ADC Transform function description

Figure 10. ADC transform function shows the ADC transform function of W7500x.

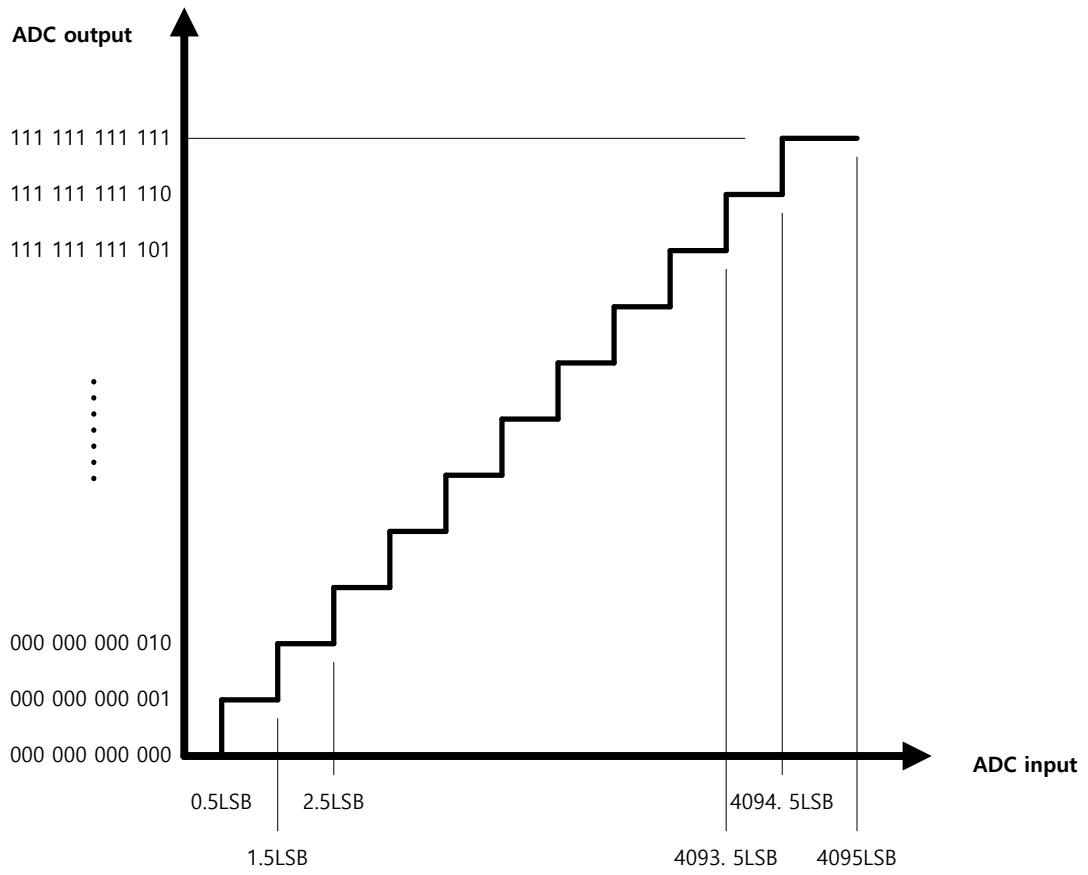


Figure 10. ADC transform function

5.11 SSP Interface Characteristics

The maximum SSP speed is 20 Mbit/s in master mode or 4 Mbit/s in slave mode. In slave mode, the maximum SSP clock rate must be 1/12 of the SSP PCLK clock rate.

Table 22 shows the SSP characteristics of W7500x.

Table 22 SSP characteristics

| Symbol | Parameter | Min | Nom | Max | Unit |
|-----------------|-----------------------------------|-----|-----|-------|----------------|
| t_{clk_per} | SSPCLK cycle time | 2 | | 65024 | System clocks |
| t_{clk_high} | SSPCLK high time | - | 0.5 | | t_{clk_per} |
| t_{clk_low} | SSPCLK low time | - | 0.5 | | t_{clk_per} |
| t_{clkrf} | SSPCLK rise/fall time | - | 6 | 10 | |
| t_{DMd} | Data from master valid delay time | 0 | - | 1 | System clocks |
| t_{DMs} | Data from master setup time | 1 | - | - | System clocks |
| t_{DMh} | Data from master hold time | 2 | - | - | System clocks |
| t_{Dss} | Data from slave setup time | 1 | - | - | System clocks |
| t_{Dsh} | Data from slave hold time | 2 | - | - | System clocks |

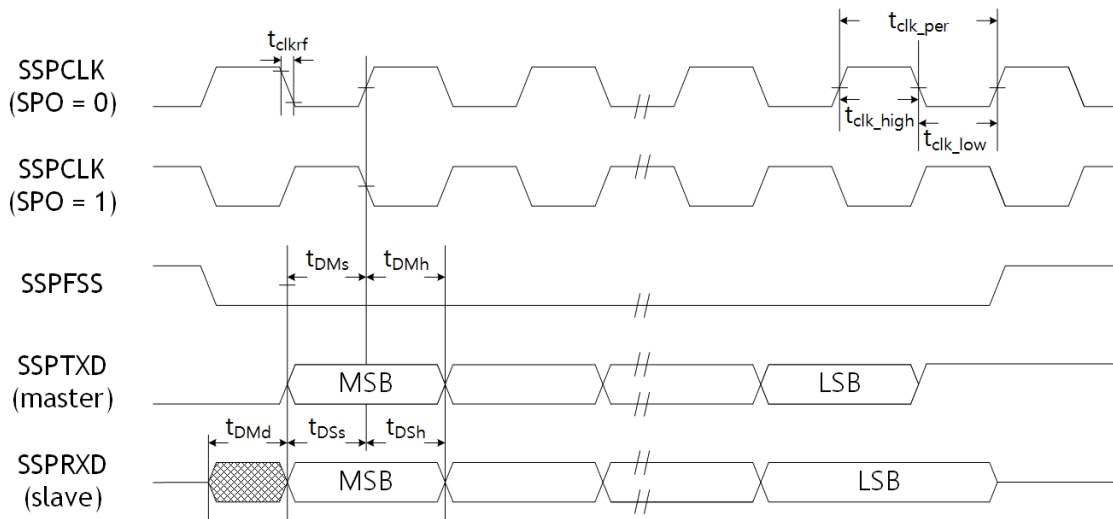


Figure 11. SSP Timing for SPI Frame format, with SPH = 1

6 Package Information

6.1 Package dimension information

Figure 12 shows the package dimension information.

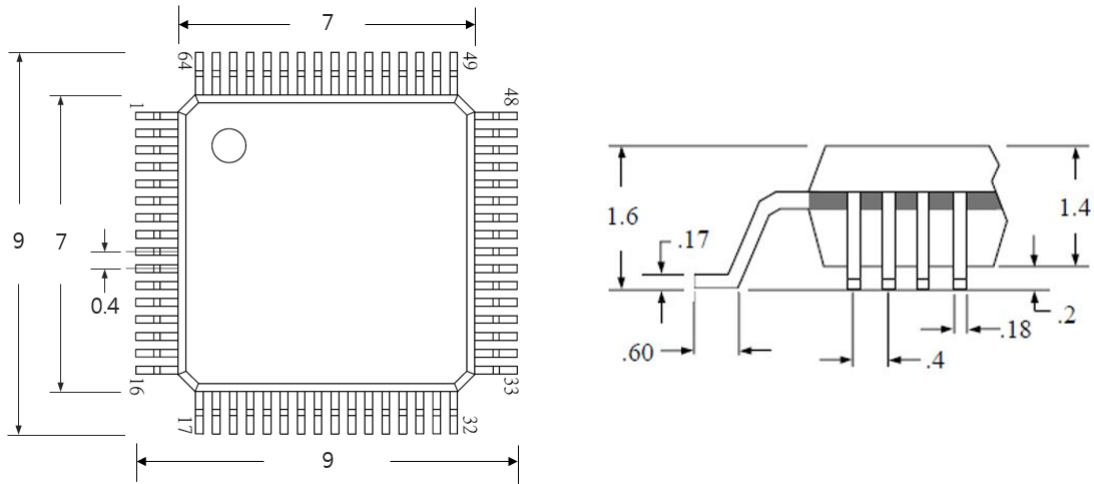


Figure 12. Package Dimension Information

Document History Information

| Version | Date | Descriptions |
|------------|-----------|---|
| Ver. 1.0.0 | 18SEP2017 | Initial Release |
| Ver. 1.0.1 | 26OCT2017 | Fixed value Driving Strength condition in PADCON. |
| Ver. 1.0.2 | 09NOV2017 | Fixed Typo I/O Pad Characteristics VOL description (high -> low) |
| Ver. 1.0.3 | 30NOV2017 | Fixed figure 8. (W7500P Pin out) |
| Ver. 1.0.4 | 18DEC2017 | Add Reset & PLL characteristics. |
| Ver. 1.0.5 | 30JAN2018 | <ol style="list-style-type: none">Fixed figure 8 (W7500P Pin layout) / Added subhead (4.2.1 W7500, 4.2.2 W7500P) / Fixed table 8(modified Symbol name)Modified SRAM description (2. Description) |
| Ver. 1.0.6 | 05FEB2018 | Add info about W7500P power consumption.(Current Characteristics) |
| Ver. 1.0.7 | 27JUL2018 | Fixed figure 2. CRG Diagram (Input Information of WDOGCLK, TIMCLK0, TIMCLK1). |
| Ver. 1.0.8 | 17OCT2018 | Fixed Power Supply description (271V - 5.5V -> 2.7V - 3.6V) |
| Ver. 1.0.9 | 11NOV2019 | Fixed 5.2 I/O Power on slope (5V/sec -> 3.3V) |

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