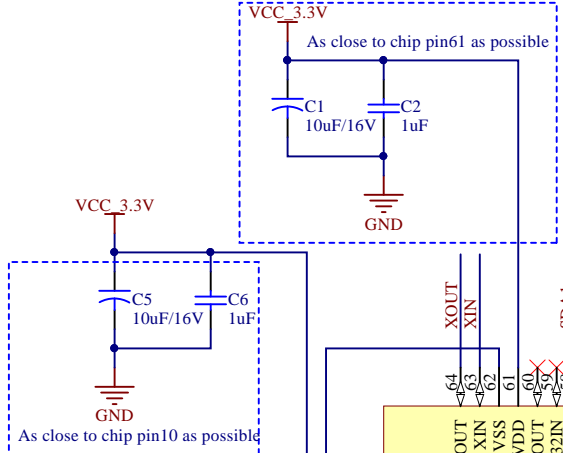


PHY link status
TCP connection status

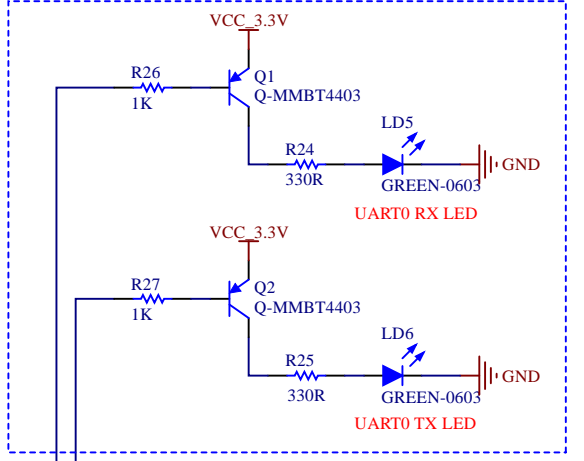
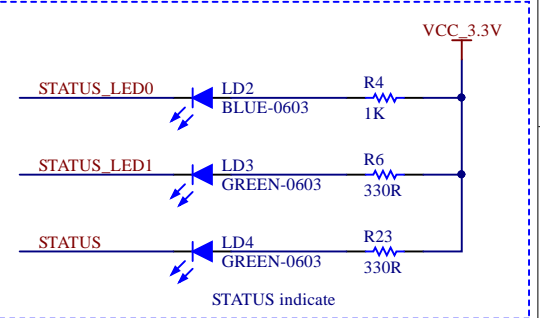
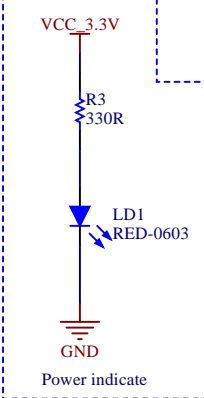
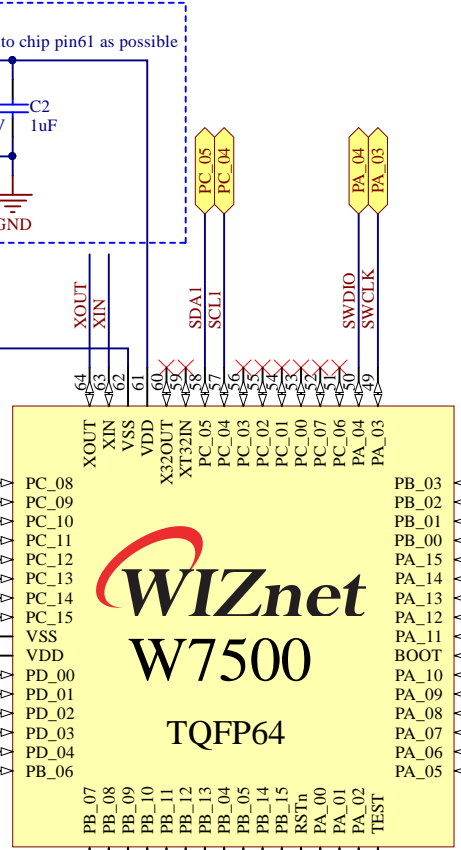
Optional_I2C_SCL0
Optional_I2C_SDA0

Optional_SPL_SSEL0
Optional_SPL_SCLK0
Optional_SPL_MISO0
Optional_SPL_MOSI0



PC_08 STATUS_LED0
PC_09 STATUS_LED1
PC_10 U_TXD2
PC_11 U_RXD2
PC_12 Expansion_GPIO_D
PC_13 Expansion_GPIO_C
PC_14 Expansion_GPIO_B
PC_15 Expansion_GPIO_A

PD_00 CRS
PD_01 RXDV
PD_02 RXD0
PD_03 RXD1
PD_04 RXD2
PD_06 RXD3



PB_03 SPI_MOSI1
PB_02 SPI_MISO1
PB_01 SPI_SCLK1
PB_00 SPI_SSEL1

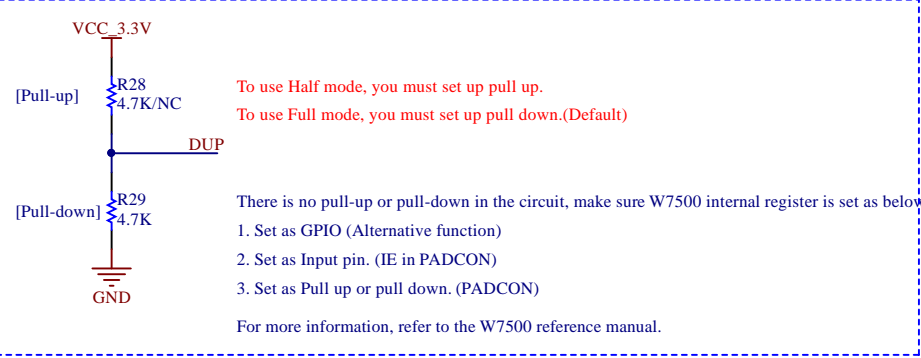
For Serial Flash Pins

PA_14 U_RXD0
PA_13 U_TXD0
PA_12 U_RTS0
PA_11 U_CTS0
PA_10 U_DTR0
PA_09 U_DSR0
PA_08 APP_BOOT
PA_07 STATUS

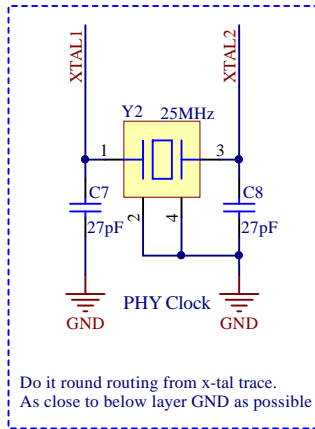
with PHY_LINK Status function (output signal)
with HW_Trigger pin function (output signal)

MDIO(PB_14),MDC(PB_15) pin is should be handled as GPIOs.

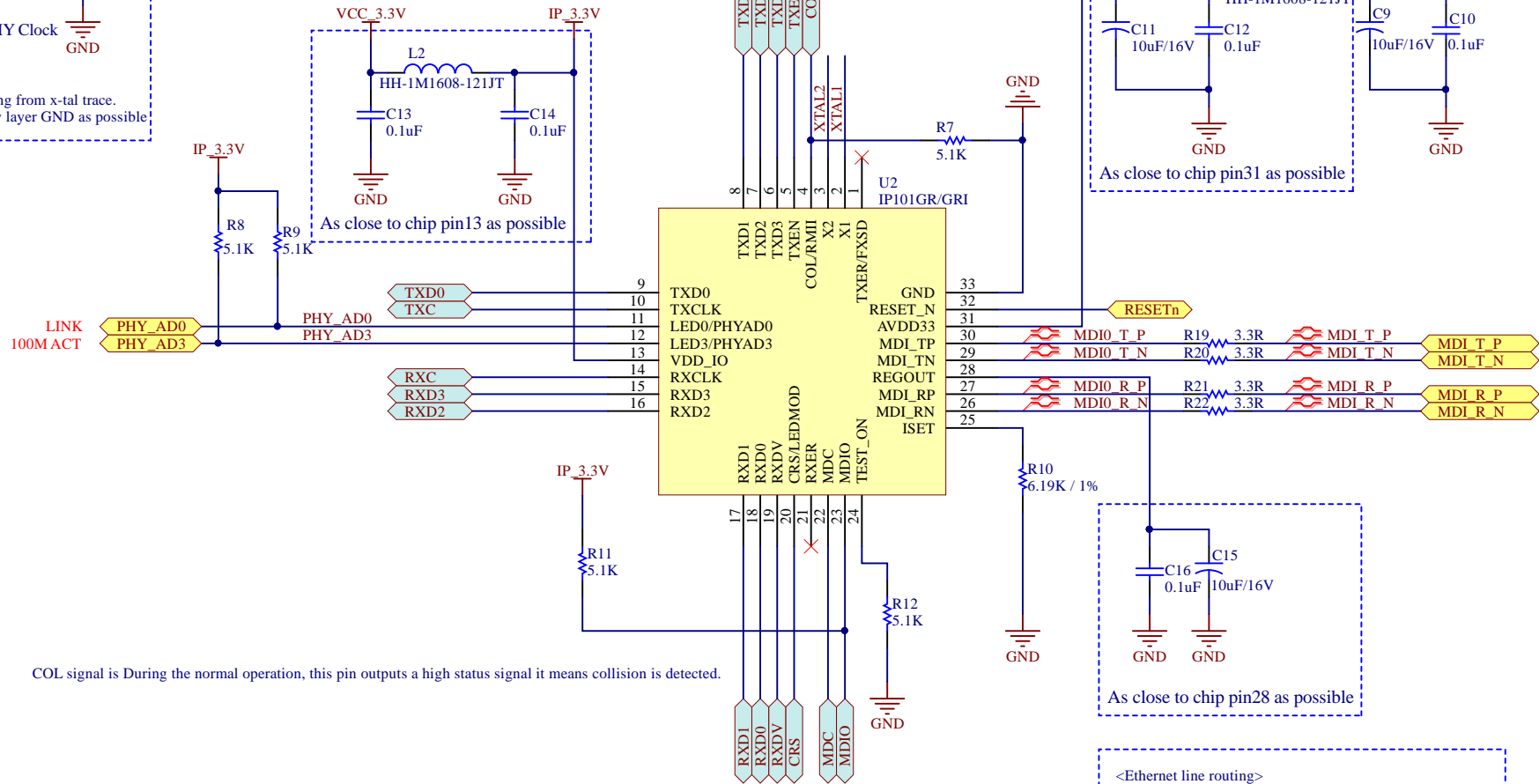
PA_00 is PHY LINK check pin(input). This pin checks PHY link from peer
This pin should be connected to the LINK status signal of the RJ-45.



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Team: Team Module	Drawn By: Edward			



Do it round routing from x-tal trace.
As close to below layer GND as possible



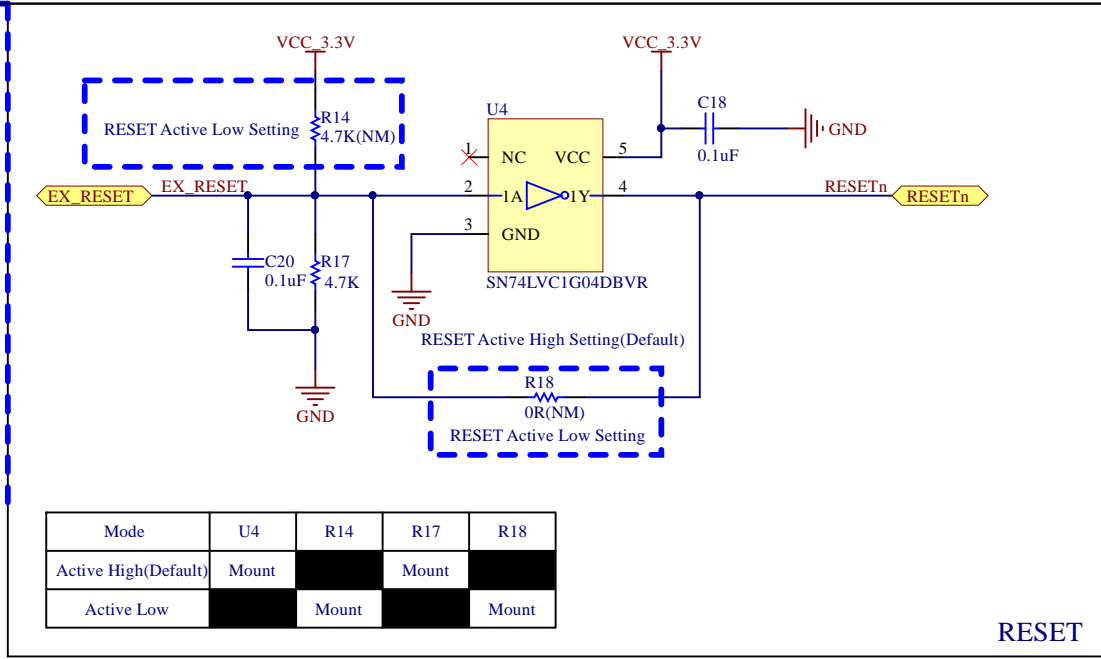
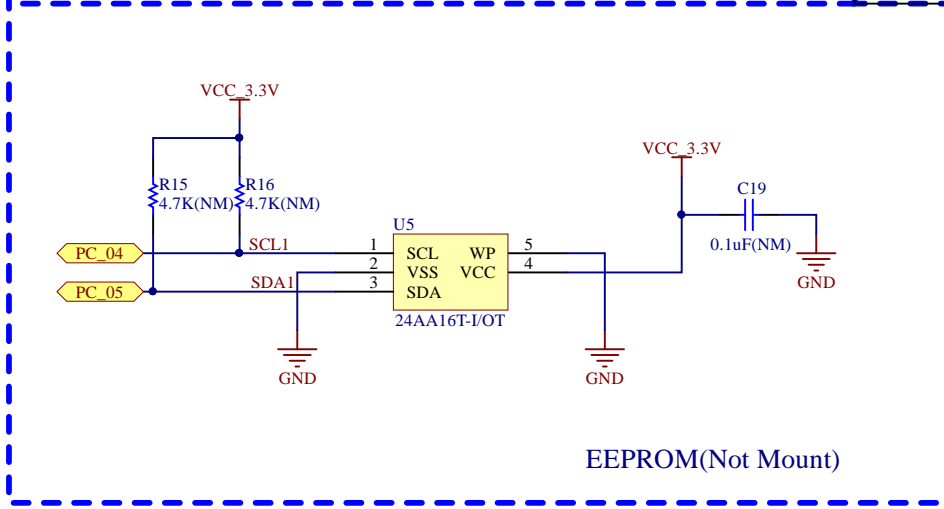
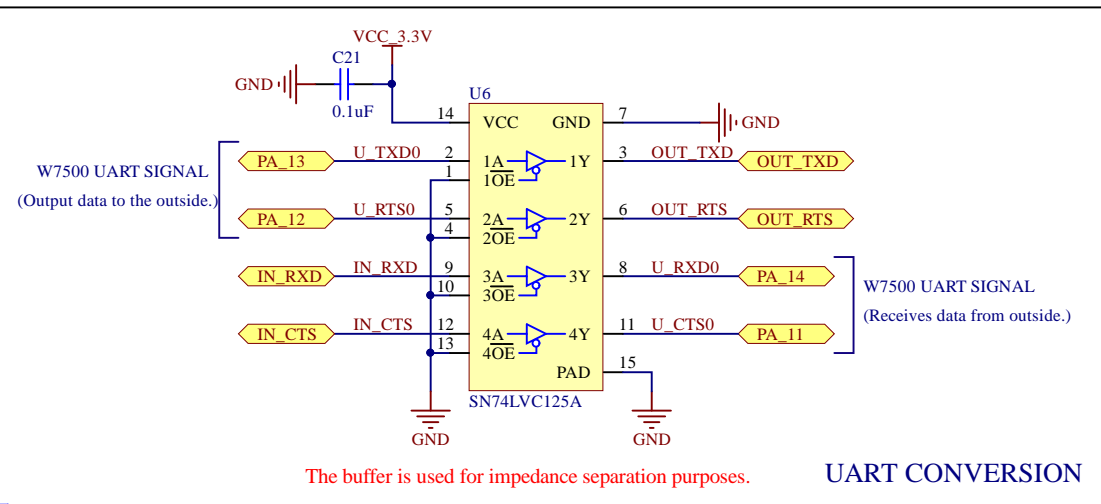
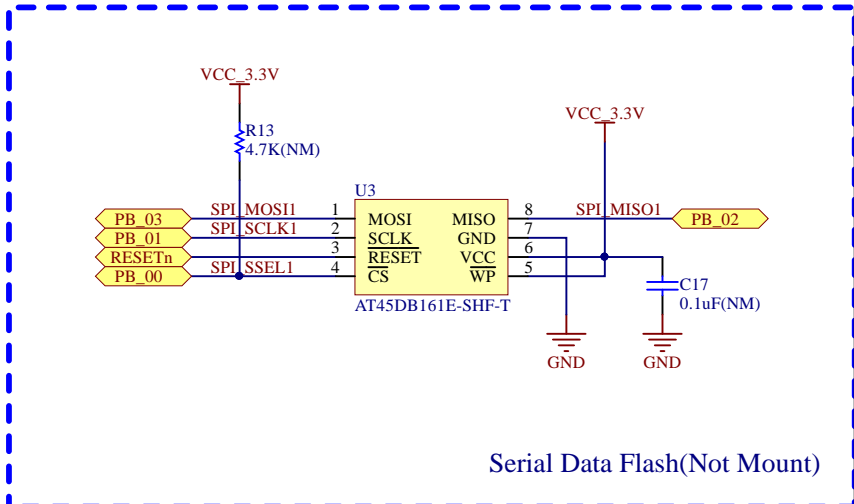
COL signal is During the normal operation, this pin outputs a high status signal it means collision is detected.

As close to chip pin31 as possible

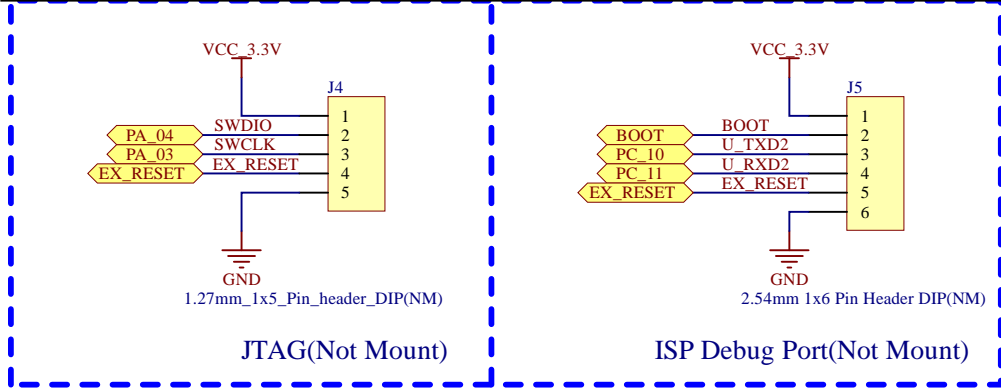
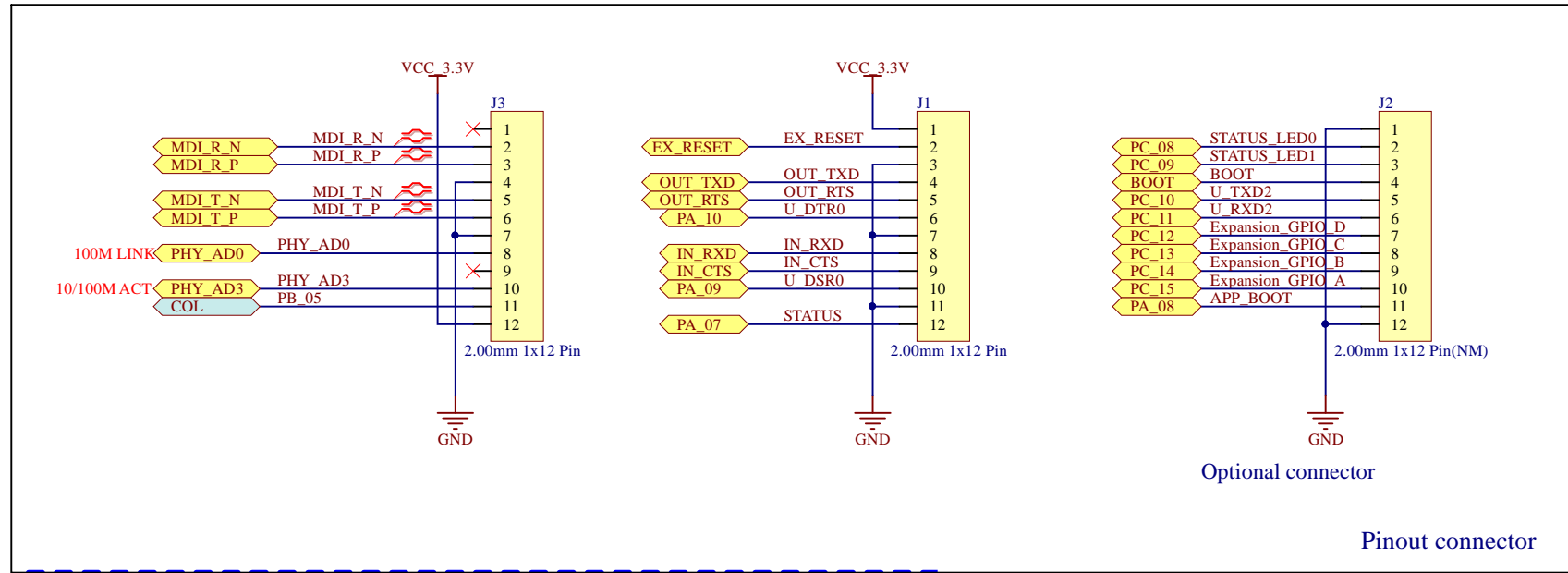
As close to chip pin28 as possible

<Ethernet line routing>
Do not position to other elements(R,L,C) to RJ-45 below
There should be no other signal under the differential signal.

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Mode	U4	R14	R17	R18
Active High(Default)	Mount		Mount	
Active Low		Mount		Mount



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[SL30210110-SWH](#) [SE308-T](#) [FCOPPER-SFP-100](#) [7506GX2](#) [708FX2-SC](#) [508TX](#) [316TX](#) [306TX](#) [306FX2-ST](#) [BB-SG30000324-51](#)