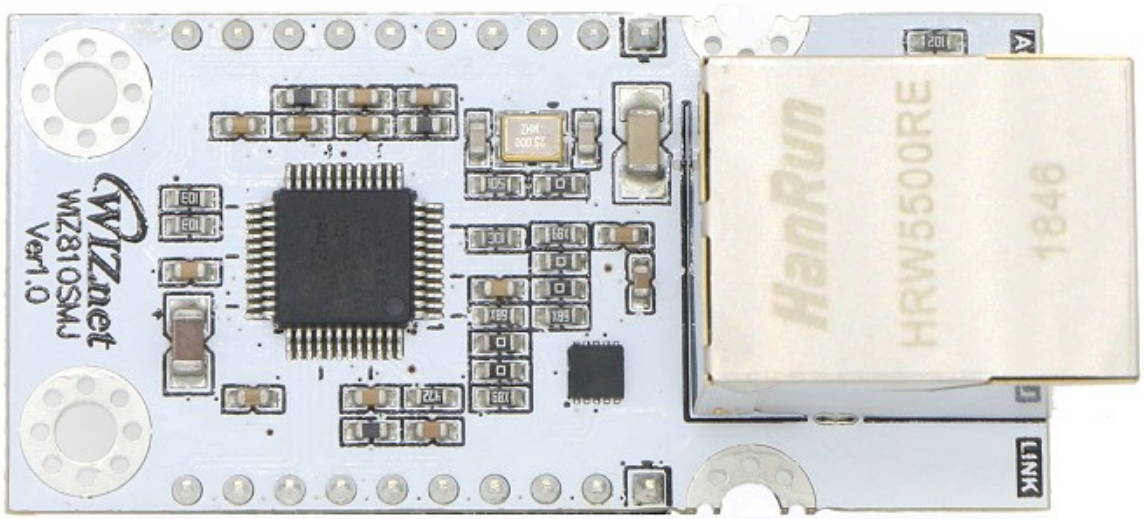
WIZ810SMJ Datasheet

(Version 1.0)



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Document Revision History

Date	Revision	Changes
2018-12-28	V1.0	Official Release

Contents

1. Introduction

WIZ810SMJ is the network module that includes W5100S (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W5100S and Transformer.
The WIZ810SMJ is an ideal option for users who want to develop their Internet enabling systems rapidly.

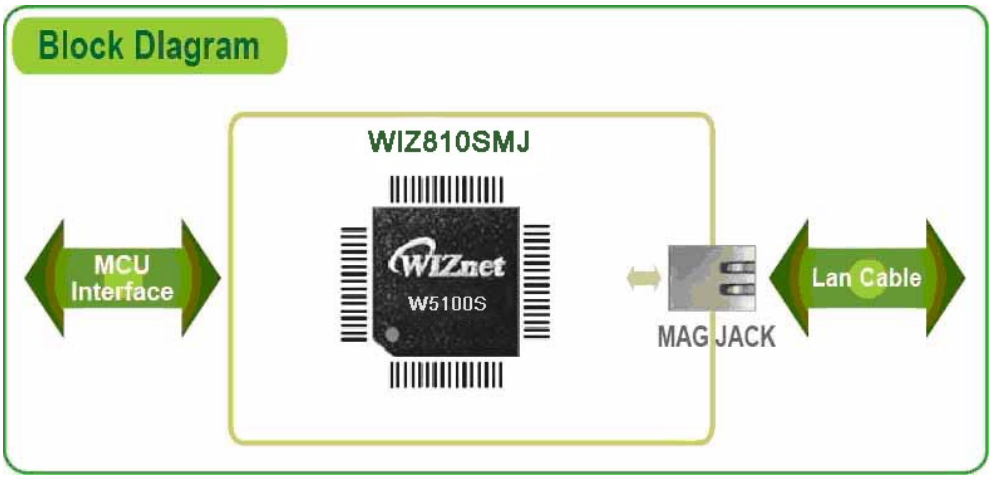
For the detailed information on implementation of Hardware TCP/IP, refer to the W5100S Datasheet.

WIZ810SMJ consists of W5100S and MAG-JACK.

- TCP/IP, Ethernet MAC : W5100S
- Ethernet PHY : Included in W5100S
- Connector : MAG-JACK(RJ45 with Transformer)

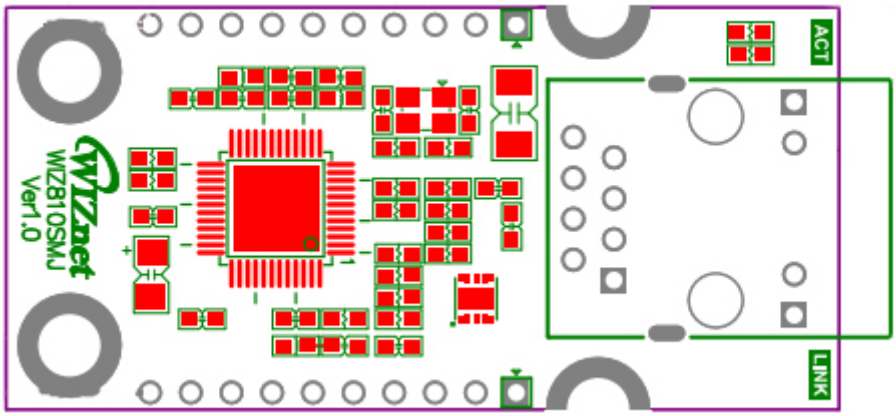
1.1. Feature

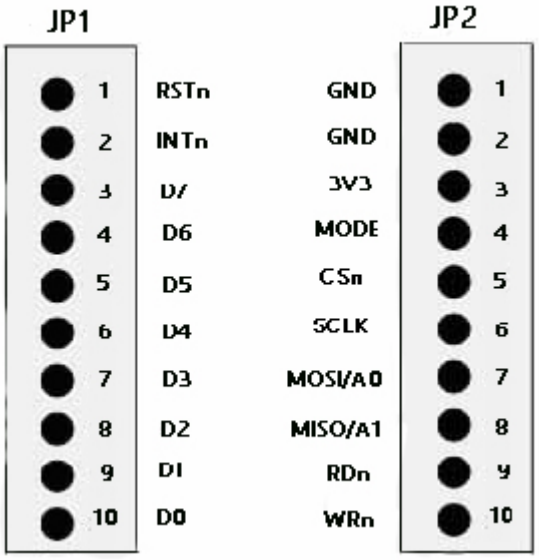
- Support Hardwired Internet protocols
  : TCP, UDP, WOL over UDP, ICMP, IGMPv1/v2, IPv4, ARP, PPPoE
- Support 4 independent SOCKETs simultaneously
- Supports half/full duplex operation
- Support SOCKET-less command
  : ARP-Request, PING-Request
- Support Ethernet Power down mode & Main Clock gating for power save
- Support Wake on LAN over UDP
- Supports high speed SPI Interface (SPI mode 0/3), Parallel System Bus with 2 Address signal & 8bit Data
- Internal 16Kbytes Memory for TX/ RX Buffers
- 10BaseT/100BaseTX Ethernet PHY Integrated
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Supports Wake On LAN
- Support Auto-MDIX only when Auto-Negotiation mode
- 3.3V operation with 5V I/O signal tolerance
- Interfaces with two 2.54mm pitch 1 x 10 header pin
- Temperature : -40 ~ 85℃(Operation)



2. Pin assignment & description

2.1. Pin assignment





2.2. Pin description

Symbol	Type	Pin No.	Description
MODE	**I**	JP2:4	**W5100S Interface Mode Selection.** Interface Mode is selected by MOD [2]. “0”: SPI Mode. “1”: Parallel Bus Mode.
CSn	**I**	**JP2:5**	**W5100S Chip Select** Low : Select High : No Select
SCLK	**I**	**JP2:6**	**SPI Clock** On SPI Mode, it is used to SPI Clock. But on Parallel Bus Mode, it must be connected to GND or be floated.
MOSI/ A0	**I**	**JP2:7**	**SPI Master Output Slave Input / Address 0** MOSI: On SPI Mode, SPI Data is received from HOST. ADDR0: On Parallel Bus Mode, it is used to Address 0.
MISO/ A1	**I/O**	**JP2:8**	**SPI Master Input Slave Output / Address 1** MISO: On SPI Mode, SPI Data is transmitted to HOST. ADDR1: On Parallel Bus Mode, It is used to Address 1.
RDn	**I**	JP2:9	**Read Strobe** On Parallel Bus Mode, it indicates Read Operation. On SPI Mode, it must be connected to 3V3D or be floated.
WRn	**I**	JP2:10	**Write Strobe** On Parallel Bus Mode, it indicates Write Operation.

D7~D0	**I/O**	JP1:10 JP1:9 JP1:8 JP1:7 JP1:6 JP1:5 JP1:4 JP1:3	**8 Bits Data Bus** On Parallel Bus Mode, DAT [7:0] receives Data from HOST or W5100 S. On SPI Mode, DAT [7:0] must be floated.
INTn	**O**	JP1:2	**Interrupt** When the event occurs during W5100S Ethernet Communication, INTn notices to HOST. Low : Interrupt Occurred High : No Interrupt Refer to IEN (Interrupt pin Enable) in MR2 (Mode Register 2), INTPTMR (Interrupt Pending Time Register), IMR W5100S Datasheet Version1.0.0 15 / 109 (Interrupt Mask Register), IMR2 (Interrupt Mask Register 2), SLIMR (SOCKET-less Interrupt Mask Register)
RSTn	**I**	JP1:1	**Reset** RSTn initializes W5100S. RSTn must be asserted to Low longer than 500ns. After asserted RSTn, W5100S spends 60.3ms for initialization. Low : W5100S initialized. High : Normal Operation.

2.3. Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP2:3	Power : 3.3 V power supply
GND	P	JP2:1, JP2:2	Ground

2.4. Miscellaneous Signals

Symbol	Type	Pin No.	Description
RSTn	**I**	**JP1:1**	**RSTn:** This pin is active low input to initialize or re-initialize W5100S. By asserting this pin low for at least 60.3 m s ,all internal registers will be re-initialized to their default states.

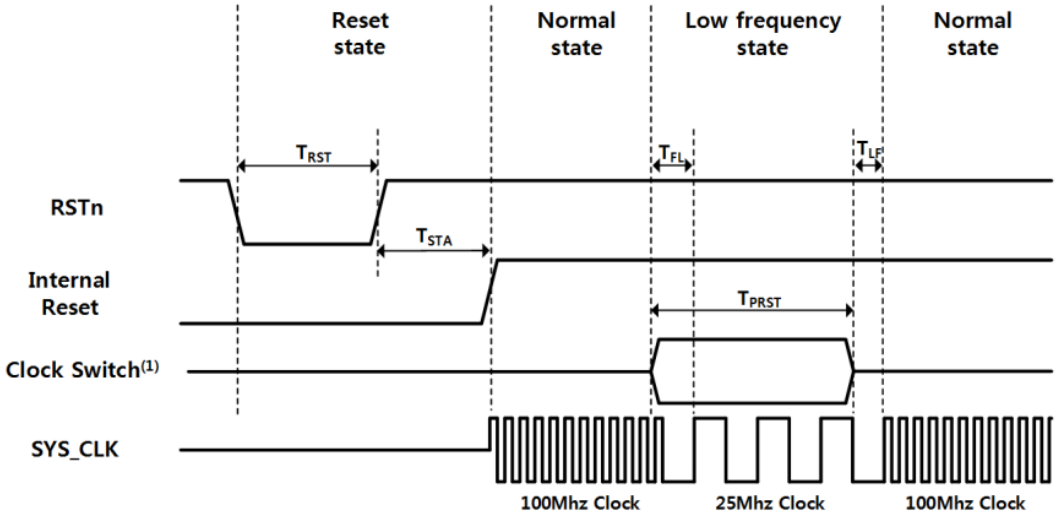
3. Timing diagram

WIZ810SMJ provides following interfaces of W5100s.

-. Parallel bus access

-. SPI access

3.1. Reset Timing

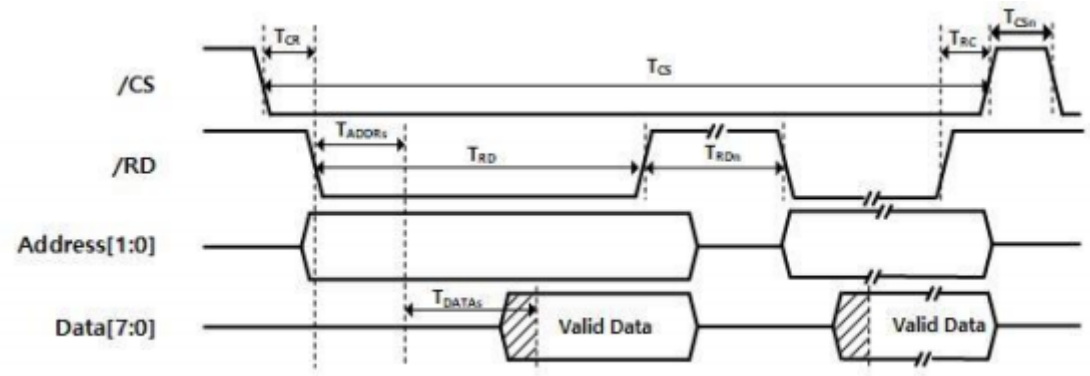


Symbol	Description	Min	Typ	Max
T_{RST}	Reset Time	210 ns	330 ns	560 ns-
T_{STA}	Stable Time	-		60.3 ms
T_{FI}	Fast to Low Time by MR2[CLKSEL]	100 ns		-
T_{FI}	Fast to Low Time by PHYCR1[Reset] or PHYCR1[PWDN]	300 ns		
T_{PRST}	PHY Auto Reset Time	0.6 ms		-
T_{PRST}	PHY Power Down Time	200 us		
T_{PRST}	Clock Switch Time	200 ns		
T_{LF}	Low to Fast Time by MR2[CLKSEL]	100 ns		-
T_{LF}	Low to Fast Time by PHYCR1[Reset] or PHYCR1[PWDN]	100 ns		

**COMMENT*: *PHY Power-down Mode has T_{FI} and T_{LF} (In PHY Power-down Mode, SYS_CLK switches to Low Clock. After T_{FI}, User can be disable PHY Power-down Mode.)*

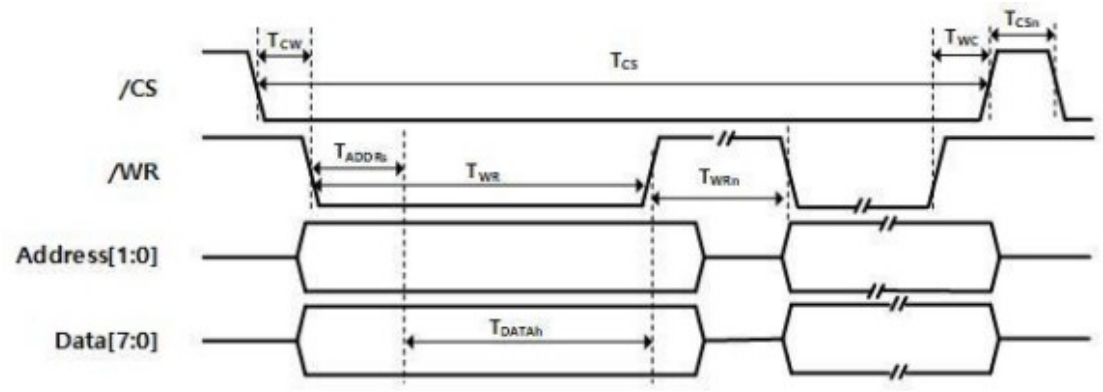
**CAUTION*: *User must not set PHY Auto Reset and PHY Power-down Mode at the same time*

3.2. BUS Access Read Timing



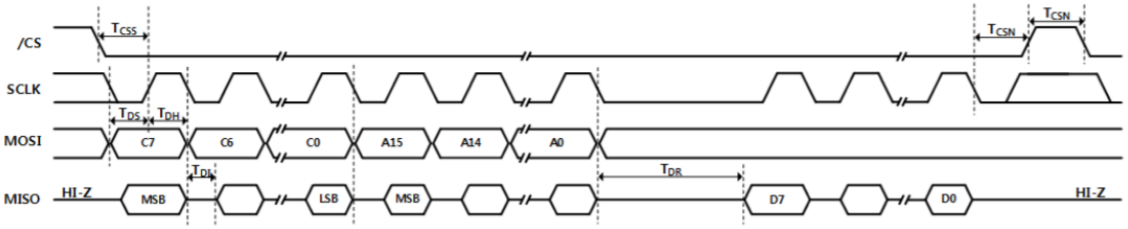
Symbol	Description	Min	Max
T_{ADDRs}	Address Setup Time	SYS_CLK	
T_{CR}	/CS Low to /RD Low Time	0 ns	
T_{cs}	/CS Low Time	4 SYS_CLK	
T_{RC}	/RD High to /CS High Time	0 ns	
T_{csn}	/CS Next Assert Time	3 SYS_CLK	
T_{RD}	/RD Low Time	4 SYS_CLK	
T_{RDn}	/RD Next Assert Time	3 SYS_CLK	
T_{DATAs}	DATA Setup Time		3 SYS_CLK+5ns

3.3. BUS Access Write Timing



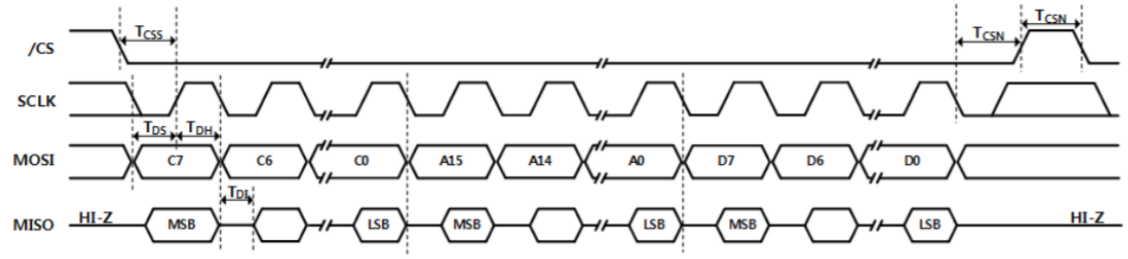
Symbol	Description	Min	Max
T_{ADDRs}	Address Setup Time	SYS_CLK	
T_{CW}	/CS Low to /WR Low Time	0 ns	
T_{cs}	/CS Low Time	4 SYS_CLK	
T_{WC}	/WR High to /CS High Time	0 ns	
T_{csn}	/CS Next Assert Time	3 SYS_CLK	
T_{WR}	/WR Low Time	4 SYS_CLK	
T_{WRn}	/WR Next Assert Time	3 SYS_CLK	
T_{DATAs}	DATA Setup Time	2 SYS_CLK	

3.4. SPI Access Read Timing



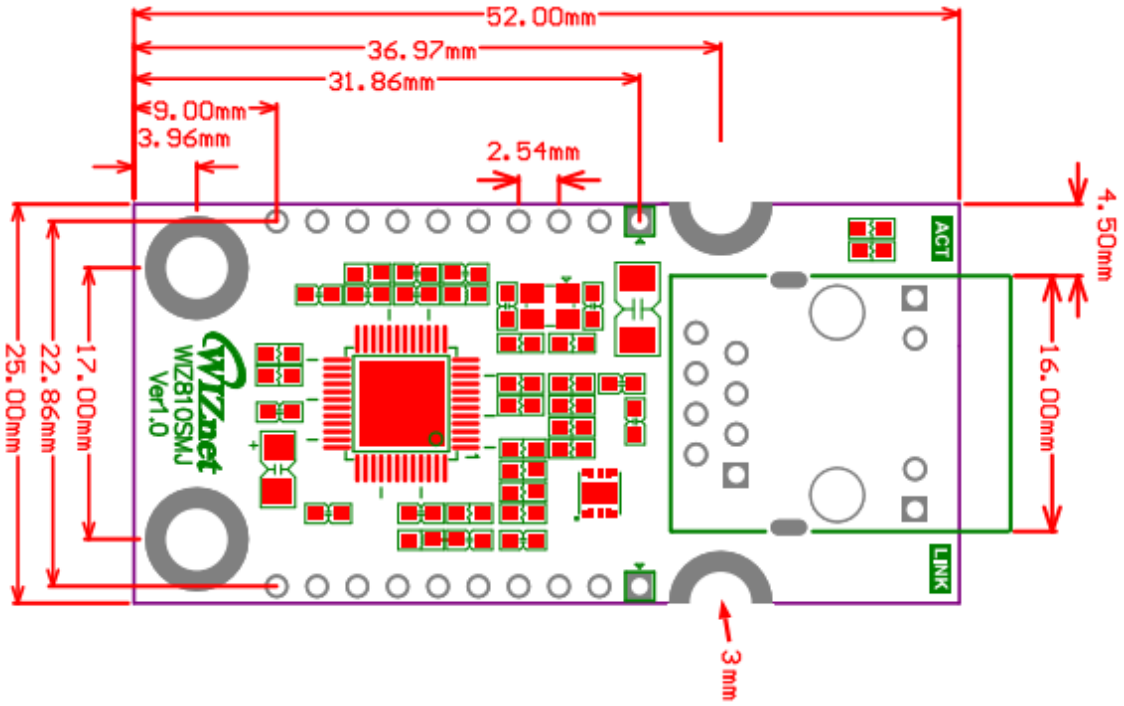
Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK		ns
T_{CSN}	SCSn Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{DI}	Data Invalid Time	7		ns
T_{DR}	Data Ready Time	6 SYS_CLK + 30		ns

3.5. SPI Access Write Timing

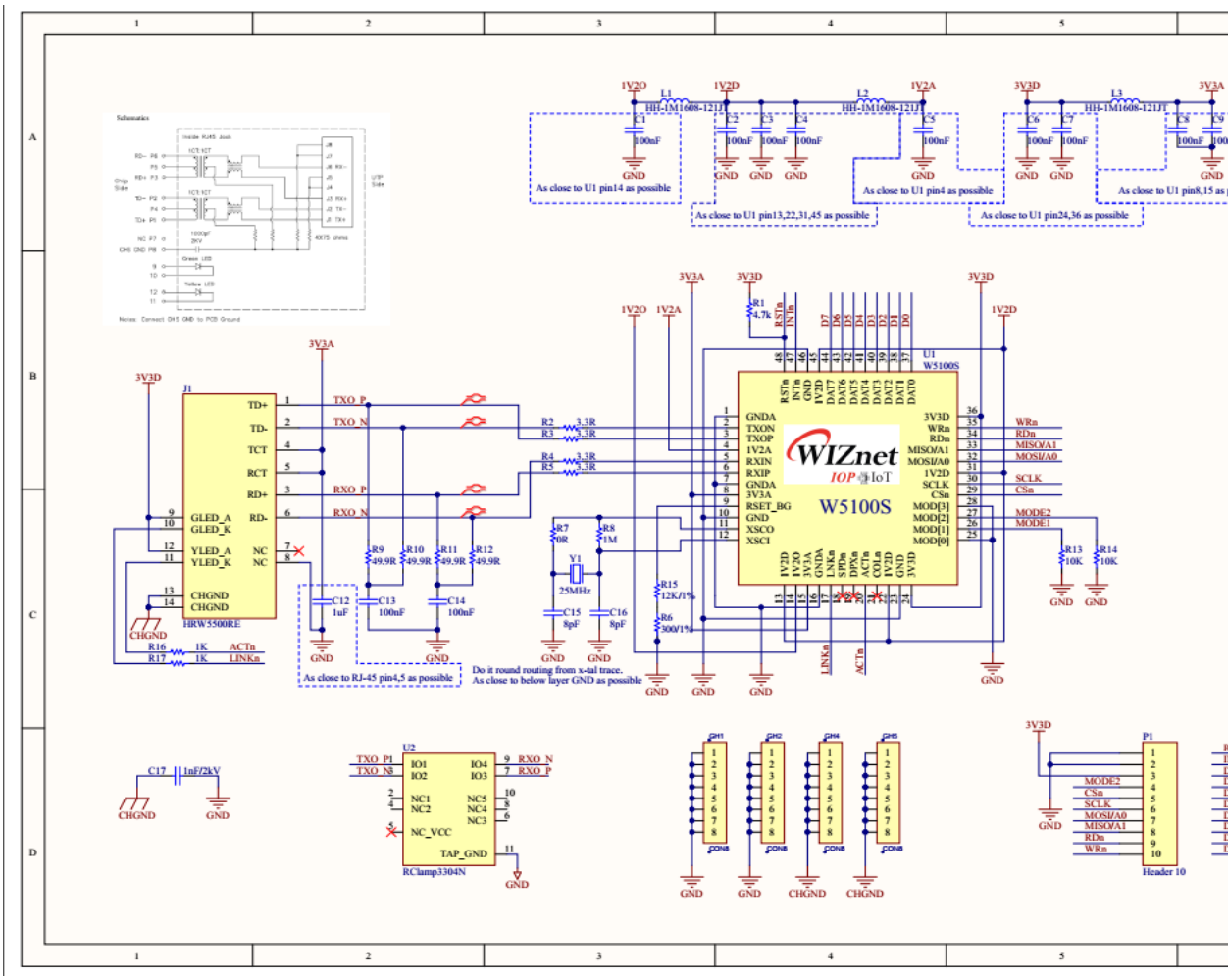


Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK		ns
T_{CSN}	SCSn Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{DI}	Data Invalid Time	7		ns

4. Dimensions



5. Reference Schematics



6. Warranty

WIZnet Co., Ltd. offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1) YEAR for the WIZ810Sio module and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in 3.Warranty. The warranty applies only to defects which occur during normal use and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occurring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.co.kr

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