

# C3M0040120J1

Silicon Carbide Power MOSFET C3M™ MOSFET Technology N-Channel Enchancement Mode

#### **Features**

- 3rd generation SiC MOSFET technology
- · Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q,,)
- Halogen free, RoHS compliant

#### **Benefits**

- · Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- · Increase system switching frequency

### **Applications**

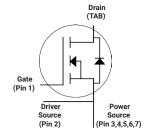
- Datacenter and Telecom Power Supplies
- EV Battery Chargers
- High voltage DC/DC converters
- Energy Storage Systems
- Solar Inverters

### **Package**









Part Number	Package	Marking
C3M0040120J1	TO-263-7L XL	C3M0040120J1

### Maximum Ratings (T<sub>c</sub> = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note	
V <sub>DSmax</sub>	Drain - Source Voltage	1200	٧	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 100 μA		
$V_{GSmax}$	Gate - Source Voltage (dynamic)	-8/+19	٧	AC (f >1 Hz)	Note 1	
$V_{GSop}$	Gate - Source Voltage (static)	-4/+15	٧	Static	Note 2	
,	Continuous Dusin Coment	64	А	$V_{GS} = 15 \text{ V}, T_{C} = 25^{\circ}\text{C}$	Fig. 19	
I <sub>D</sub>	Continuous Drain Current	42		$V_{GS} = 15 \text{ V}, T_{C} = 100^{\circ}\text{C}$		
I <sub>D(pulse)</sub>	Pulsed Drain Current	100	А	Pulse width t <sub>P</sub> limited by T <sub>jmax</sub>		
P <sub>D</sub>	Power Dissipation	272	W	T <sub>c</sub> =25°C, T <sub>J</sub> = 150 °C	Fig. 20	
$T_{J}$ , $T_{stg}$	Operating Junction and Storage Temperature	-40 to +150	°C			
T <sub>L</sub>	Solder Temperature	260	°C	1.6mm (0.063") from case for 10s		

Note (1): When using MOSFET Body Diode  $V_{GSmax} = -4V/+19V$ 

Note (2): MOSFET can also safely operate at 0/+15 V



# **Electrical Characteristics** ( $T_c = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions	Note	
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	1200			٧	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 100 μA		
		1.8	2.7	3.6	٧	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 9.2 mA	Fig. 11	
$V_{\text{GS(th)}}$	Gate Threshold Voltage		2.2		٧	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 9.2 mA, T <sub>J</sub> = 150°C		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		1	50	μΑ	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V		
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15 \text{ V, } V_{DS} = 0 \text{ V}$		
D	Drain-Source On-State Resistance		40	53.5	mΩ	V <sub>GS</sub> = 15 V, I <sub>D</sub> = 33.3 A	Fig. 4,	
R <sub>DS(on)</sub>	Dialif-Source Off-State Resistance		60		111122	$V_{GS} = 15 \text{ V, } I_D = 33.3 \text{ A, } T_J = 150 ^{\circ}\text{C}$	5, 6	
$g_{fs}$	Transconductance		21		S	V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 33.3 A	Fig. 7	
yts	Transconductance		20			V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 33.3 A, T <sub>J</sub> = 150°C		
$C_{iss}$	Input Capacitance		2900					
Coss	Output Capacitance		103		pF	$V_{GS} = 0 \text{ V}, V_{DS} = 1000 \text{ V}$ f = 100  kHz	Fig. 17,	
C <sub>rss</sub>	Reverse Transfer Capacitance		5		]	V <sub>AC</sub> = 25 mV		
Eoss	Coss Stored Energy		60		μJ		Fig. 16	
Eon	Turn-On Switching Energy (Body Diode FWD)		339		$V_{DS} = 800 \text{ V}, V_{GS} = -4 \text{ V}/+15 \text{ V},$			
E <sub>OFF</sub>	Turn Off Switching Energy (Body Diode FWD)		67		μJ	$I_D = 33.3 \text{ A},$ $R_{G(ext)} = 2.5\Omega, L = 99 \mu\text{H},$	Fig. 26	
t <sub>d(on)</sub>	Turn-On Delay Time		13				Fig. 27	
t <sub>r</sub>	Rise Time		18		<u> </u>	$V_{DD} = 800 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}$		
t <sub>d(off)</sub>	Turn-Off Delay Time		22		ns	$R_{G(ext)} = 2.5 \Omega$ , $I_D = 33.3 A$ , L= 99 Timing relative to $V_{DS'}$ Inductive load		
t <sub>f</sub>	Fall Time		8		1	DS,		
R <sub>G(int)</sub>	Internal Gate Resistance		3.5		Ω	f = 1 MHz, V <sub>AC</sub> = 25 mV		
$Q_{gs}$	Gate to Source Charge		35			V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -4 V/15 V		
$Q_{\text{gd}}$	Gate to Drain Charge		27		nC	I <sub>D</sub> = 33.3 A	Fig. 12	
Qg	Total Gate Charge		94			Per IEC60747-8-4 pg 21		



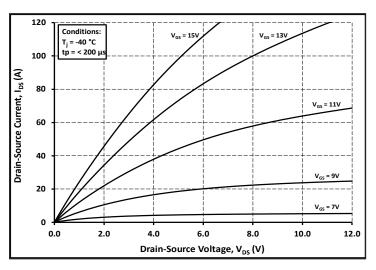
## **Reverse Diode Characteristics** ( $T_c = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Тур.	Max.	Unit	Test Conditions	Note
V <sub>SD</sub> D	Diode Forward Voltage	5.5		٧	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 20 A, T <sub>J</sub> = 25°C	Fig. 8,
		4.5		٧	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 20 A, T <sub>J</sub> = 150°C	
Is	Continuous Diode Forward Current		44	Α	V <sub>GS</sub> = -4 V, T <sub>C</sub> = 25°C	Note 1
S, pulse	Diode pulse Current		100	Α	$V_{GS}$ = -4 V, pulse width $t_P$ limited by $T_{Jmax}$	Note 1
t <sub>rr</sub>	Reverse Recover time	11		ns		
$Q_{rr}$	Reverse Recovery Charge	323		nC	$V_{GS} = -4 \text{ V, } I_{SD} = 33.3 \text{ A, } V_{R} = 800 \text{ V}$ dif/dt = 9890 A/ $\mu$ s	
I <sub>rrm</sub>	Peak Reverse Recovery Current	52		Α		
t <sub>rr</sub>	Reverse Recover time	17		ns		
Q <sub>rr</sub>	Reverse Recovery Charge	150		nC	$V_{SS} = -4 \text{ V, } I_{SD} = 33.3 \text{ A, } V_{R} = 800 \text{ V}$ dif/dt = 1815 A/µs	
I <sub>rrm</sub>	Peak Reverse Recovery Current	16		А		

#### **Thermal Characteristics**

Symbol	Parameter	Тур.	Unit	Test Conditions	Note
R <sub>θJC</sub>	Thermal Resistance from Junction to Case	0.46			F: 04
R <sub>θJA</sub>	Thermal Resistance From Junction to Ambient	40	°C/W		Fig. 21





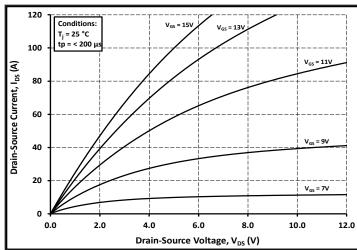
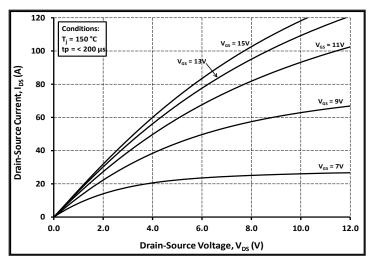


Figure 1. Output Characteristics T<sub>J</sub> = -40 °C





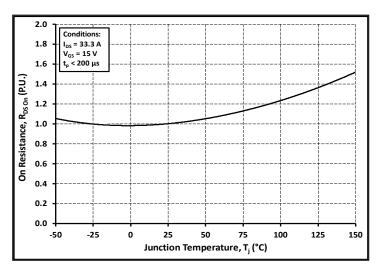
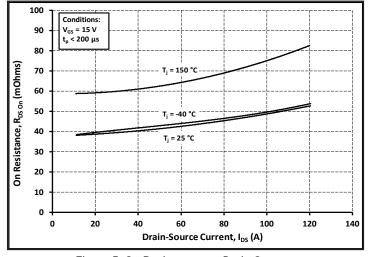


Figure 3. Output Characteristics T<sub>J</sub> = 150 °C

Figure 4. Normalized On-Resistance vs. Temperature



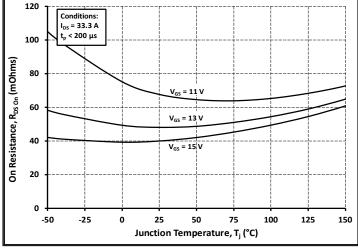
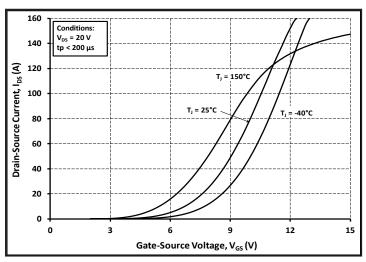


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

Figure 6. On-Resistance vs. Temperature For Various Gate Voltage





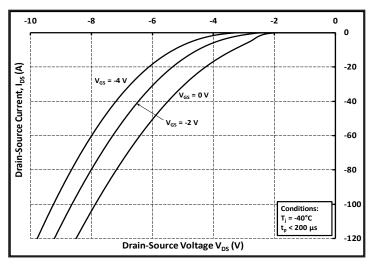
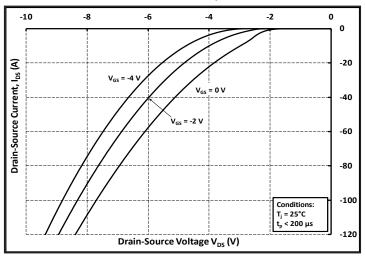


Figure 7. Transfer Characteristic for Various Junction Temperatures





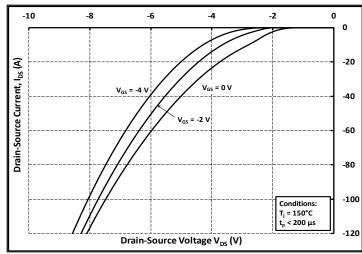
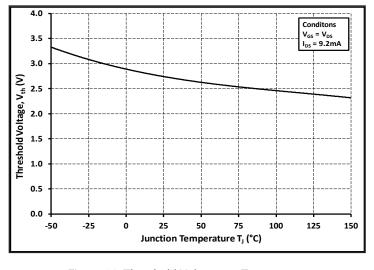


Figure 9. Body Diode Characteristic at 25 °C

Figure 10. Body Diode Characteristic at 150 °C



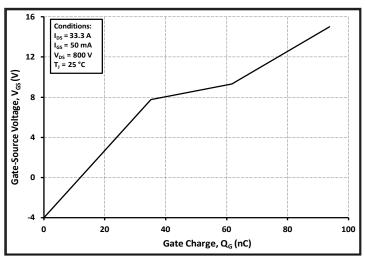
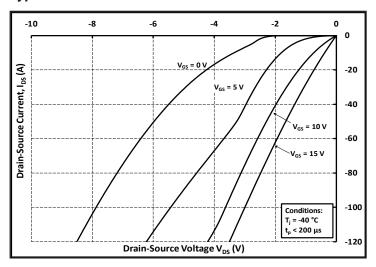


Figure 11. Threshold Voltage vs. Temperature

Figure 12. Gate Charge Characteristics





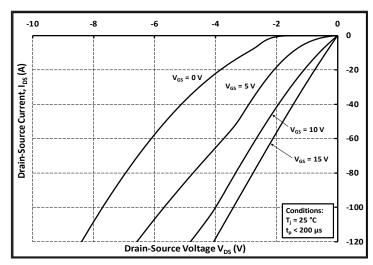
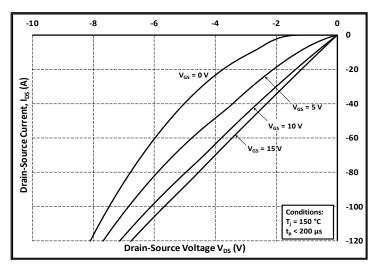


Figure 13. 3rd Quadrant Characteristic at -40 °C





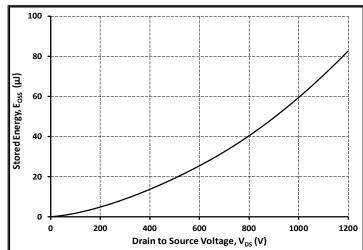
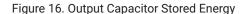
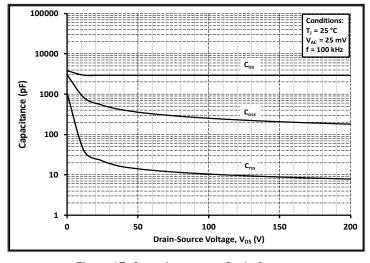


Figure 15. 3rd Quadrant Characteristic at 150 °C





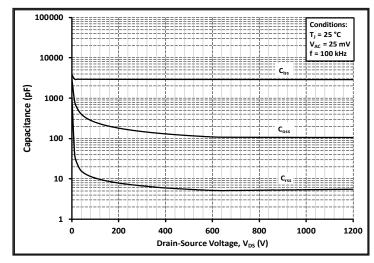
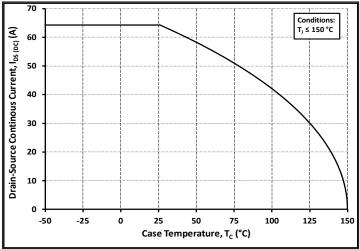


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)





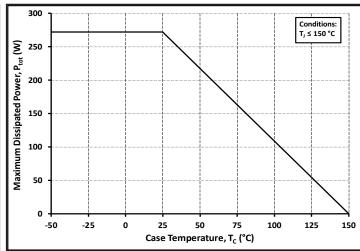
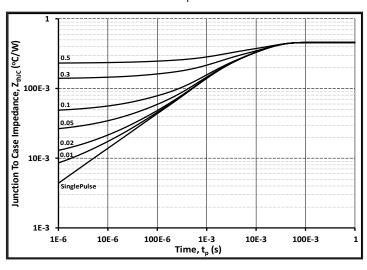


Figure 19. Continuous Drain Current Derating vs.

Case Temperature

Figure 20. Maximum Power Dissipation Derating vs.
Case Temperature



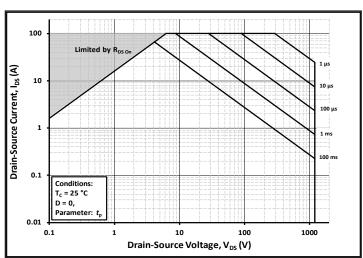
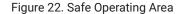
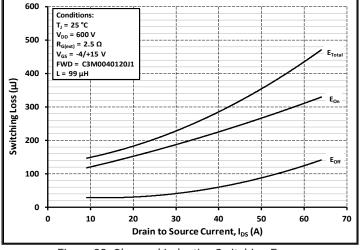


Figure 21. Transient Thermal Impedance (Junction - Case)





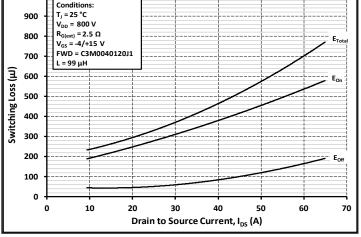
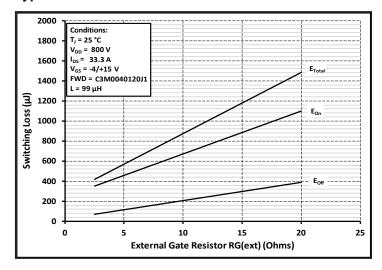


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600V$ )

Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD}$  = 800V)

1000





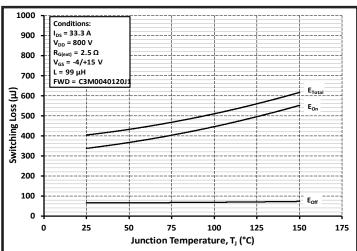


Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$ 

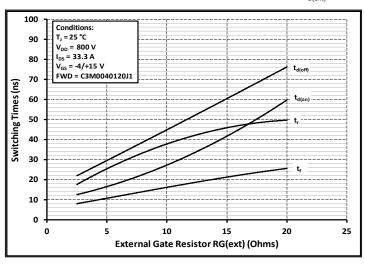


Figure 26. Clamped Inductive Switching Energy vs.
Temperature

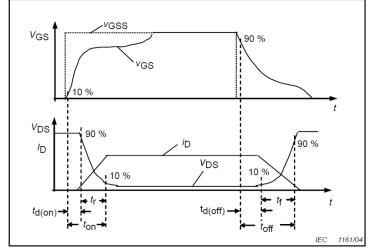


Figure 27. Switching Times vs. R<sub>G(ext)</sub>

Figure 28. Switching Times Definition



#### **Test Circuit Schematic**

Rev. 0, October 2021

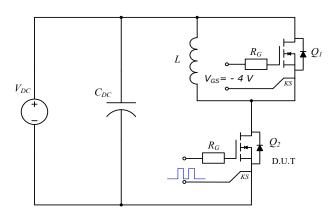


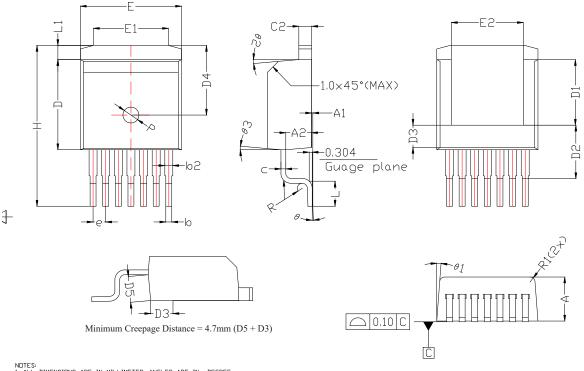
Figure 28. Clamped Inductive Switching Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.



#### **Package Dimensions**

TO-263-7L XL



DIM	MIN	MAX	TYP			
D	9.025	9.125	9.075			
E	10.13	10.23	10.18			
Α	4.30	4.57	4.435			
Н	15.043	17.313	16.178			
D1	6.50	6.70	6.60			
E1	6.50	8.60	7.55			
D2	5	.39 RE	F.			
E2	6.778	7.665	7.223			
D3	2.148		2.248			
D4	7	.00 RE	F.			
D5	2.555		2.605			
A1	0	0.25	0.125			
A2	2.595 REF.					
е	1.5	27 TY	Ρ.			
L	2.324	2.70	2.512			
b	0.50	0.70	0.60			
L1	0.968	1.868	1.418			
b2	0.60	1.00	0.80			
C5	1.17	1.37	1.27			
C	0.281	0.481	0.381			
R	0.506 REF.					
R1	0.50 REF.					
Р	Ø1.60 REF.					
θ	0°	8°	4°			
θ1	4.5°	5.5°	5°			
θ2	4°	6°	5°			
θ3			5°			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETER, ANGLES ARE IN DEGREE.

2. DIMENSION'D' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH SHALL
NOT EXCEED 0.50 MM PER SIDE. DIMENSION'E' DOES NOT INCLUDE MOLD FLASH, GATE BURRS,THE
GATE BURRS SHALL NOT EXCEED 0.30MM.

3. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKGE BOTOM DIMENSIONS D AND E ARE
DETERMINED AT THE DUTERMOST EXTERNES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE
BAR BURRS, GATE BURRS AND INTERLEAD FLASH,BUT INCLUDING ANY MISMATCH BETWEEN THE TOP
AND BOTTOM OF THE PLASTIC BODY.

4. "62" DIMENSION DON'T INCLUDE DAMBAR PROTRUSION.

5. THE VOID SHOULD BE CONTROL WITHIN 0.25MM.

10.8 8.0 8.1 В 16.85 В 1.27 **Package Top View When Solder PCB Pad Layout Top View** Notes: 1. All dimensions are in Millimeters. Angles are in Degrees



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