WPMDM1500602 / 171050601

MagI³C Power Module

VDRM – Variable Step Down Regulator Module

6V – 36V / 5A / 0.8V – 6V Output

DESCRIPTION

The VDRM series of the MagI³C Power Module family provides a fully integrated DC-DC power supply including the buck switching regulator and inductor in a package.

The 171050601 offers high efficiency and delivers up to 5A of output current. It operates with an input voltage from 6V up to 36V. It is designed for fast transient response.

It is available in an innovative industrial high power density TO263-7EP (10.16 x 13.77 x 4.57mm) package that enhances thermal performance and allows for hand or machine soldering.

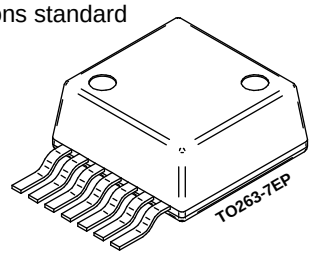
The VDRM regulators have an integrated protection circuit that guards against thermal overstress and electrical damage by using thermal shut-down, overcurrent, short-circuit, overvoltage and undervoltage protection.

TYPICAL APPLICATIONS

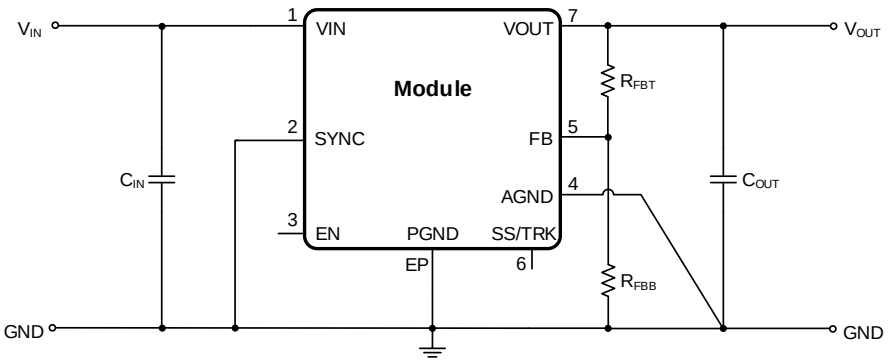
- Point-of-Load DC-DC applications from 9V, 12V, 18V and 24V industrial rails
- Industrial, test & measurement, medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply

FEATURES

- Peak efficiency above 90%
- Current capability up to 5A
- Input voltage range: 6V to 36V
- Output voltage range: 0.8V to 6V
- Reference accuracy: ±2.5%
- No minimum load required
- Integrated shielded inductor solution for quick time to market and ease of use
- Single exposed pad for best-in-class thermal performance
- Low output voltage ripple (< 10mV$_{pp}$)
- Fixed switching frequency: 812kHz (typ.)
- Current Mode control
- Synchronous operation
- Automatic power saving operation at light load
- Undervoltage lockout protection (UVLO)
- Adjustable soft-start and voltage tracking
- Frequency Synchronization with external clock (from 650kHz to 950kHz)
- Thermal shutdown
- Short circuit protection
- Cycle-by-cycle current limit
- Output overvoltage protection
- Package compatible with 171010601, 171012401, 171020601, 171012402, 171030601 and 171032401
- Operating ambient temperature up to 105°C
- RoHS and REACh compliant
- Operating junction temp. range: -40 to 125°C
- Mold compound UL 94 Class V0 (flammability testing) certified
- Complies with EN55032 class B conducted and radiated emissions standard



TYPICAL CIRCUIT DIAGRAM



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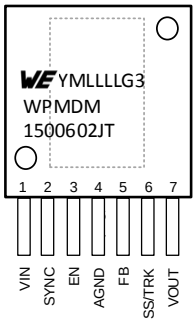
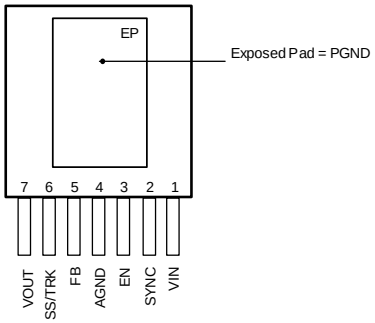
PACKAGE



Top View



Bottom View

MARKING DESCRIPTION

Marking	Description
WE	Würth Elektronik tradename
Y	Year
M	Month
LLLL	Assembly lot code
G3	Lead finish code per Jedec Norm (green 3 mat sin)
WPMDM	Würth Part Description (part 1)
1500602JT	Würth Part Description (part 2)

PIN DESCRIPTION

SYMBOL	NUMBER	TYPE	DESCRIPTION
VIN	1	Power	The supply input pin is a terminal for an unregulated input voltage source. It is required to place the input capacitor nearby the VIN pin and PGND.
SYNC	2	Input	The Sync input pin allows for synchronization of the PWM operating frequency with an external frequency source. Apply a CMOS logic level square wave with a frequency between 650 kHz and 950 kHz. When not using synchronization connect to ground. The module free running PWM frequency is 812kHz (typical).
EN	3	Input	Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.
AGND	4	Supply	The analog ground pin is the reference point for all stated voltages and must be connected to PGND.
FB	5	Input	The feedback pin is internally connected to the regulation circuitry, the over-voltage and short-circuit comparators. The regulation reference point is 0.796V at this input pin. Connect the feedback resistor divider between the output and AGND with the midpoint at this pin to set the output voltage.
SS/TRK	6	Input	The Soft-Start and Tracking pin is to extend the 1.6ms internal soft-start by connecting an external soft-start capacitor. To enable voltage tracking connect to an external resistive divider connected to a higher priority supply rail.
VOUT	7	Power	The output voltage pin is connected to the internal inductor. For the best stability and operation connect the output capacitor between this pin and PGND.
PGND	EP	Power	Exposed Pad - Main node for switch current of internal low-side MOSFET. Used as heat sink for power dissipation during operation. Must be electrically connected to pin 4.

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ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171050601	WPMDM1500602JT	5A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178050601	WPMDM1500602JEV	5A / 0.8-6Vout version	Eval Board	1

PACKAGE COMPATIBLE FAMILY MEMBERS

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171012401	WPMDH1102401JT	1A / 5-24Vout version	TO263-7EP	Tape and Reel, 250 pieces
178012401	WPMDH1102401JEV	1A / 5-24Vout version	Eval Board	1
171012402	WPMDH1152401JT	2A / 5-24Vout version	TO263-7EP	Tape and Reel, 250 pieces
178012402	WPMDH1152401JEV	2A / 5-24Vout version	Eval Board	1
171032401	WPMDH1302401JT	3A / 5-24Vout version	TO263-7EP	Tape and Reel, 250 pieces
178032401	WPMDH1302401JEV	3A / 5-24Vout version	Eval Board	1
171010601	WPMDH1100601JT	1A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178010601	WPMDH1100601JEV	1A / 0.8-6Vout version	Eval Board	1
171020601	WPMDH1200601JT	2A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178020601	WPMDH1200601JEV	2A / 0.8-6Vout version	Eval Board	1
171030601	WPMDH1300601JT	3A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178030601	WPMDH1300601JEV	3A / 0.8-6Vout version	Eval Board	1

SALES INFORMATION

SALES CONTACTS
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/powermodules Technical support: powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN (1)	MAX (1)	
VIN	Input voltage pin	-0.3	40	V
EN, SYNC	Enable and synchronization pins	-0.3	5.5	V
SS/TRK, FB	Soft-Start/Tracking and Feedback pins	-0.3	2.5	V
AGND	AGND to PGND	-0.3	0.3	V
V_{ESD}	ESD Voltage (Human Body Model), according to EN61000-4-2 (2)	-	±2000	V
T_J	Junction temperature	-	150	°C
$T_{storage}$	Assembled, non-operating storage temperature	-65	150	°C
T_{SOLR}	Peak case/leads temperature during reflow soldering, max. 20sec (3)	235	245	°C

OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

SYMBOL	PARAMETER	MIN (1)	TYP (4)	MAX (1)	UNIT
V_{IN}	Input voltage	6	-	36	V
V_{OUT}	Regulated output voltage	0.8	-	6	V
V_{EN}, V_{SYNC}	Enable and Synchronization input voltage	0	-	5	V
T_A	Ambient temperature range	-40	-	105(5)	°C
T_J	Junction temperature range	-40	-	125	°C
I_{OUT}	Nominal output current	-	-	5	A

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP (4)	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance (6)	12	°C/W
Θ_{Jc}	Junction-to-case thermal resistance	1.9	°C/W
T_{SD}	Thermal shutdown, rising	165	°C
	Thermal shutdown hysteresis, falling	15	°C

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ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended junction temperature range of **-40°C to 125°C**. Typical values represent statistically the utmost probable values at the following conditions: V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (4)	MAX (1)	UNIT
Output current						
I_{CL_HS}	High-side current limit threshold		-	7	-	A
I_{CL_LS}	Low-side current limit threshold		-	5.4	-	A
Output voltage						
V_{FB}	Reference accuracy	V_{SS}>0.8V, I_{OUT} = 5A	0.776	0.796	0.816	V
I_{FB}	Feedback input bias current		-	5	-	nA
V_{OUT}	Line regulation	V_{IN} = 12V to 36V I_{OUT} = 1mA	-	±0.02	-	%
	Load regulation	V_{IN} = 12V I_{OUT} = 1mA to 5A	-	1	-	mV/A
	Output voltage ripple	I_{OUT} = 5A C_{OUT} = 220µF, 20mΩ ESR +2 x 22µF MLCC X5R 20MHz BWL	-	6	-	mV_{pp}
Protections						
V_{FB-OVP}	Feedback over voltage protection threshold		-	0.86	-	V
Switching frequency						
f_{SW}	Switching frequency	V_{SYNC} = 0V	711	812	914	kHz
D_{MAX}	Maximum duty cycle		-	83	-	%
f_{CLK}	Synchronization clock frequency range		650	-	950	kHz
V_{CLK-H}	High-level threshold synchronization clock	Relative to AGND	1.5	-	-	V
V_{CLK-L}	Low-level threshold synchronization clock	Relative to AGND	-	-	0.4	V
D_{CLK}	Synchronization clock duty cycle range		15	50	85	%
Enable						
V_{EN}	EN threshold trip point	V_{EN} rising	1.10	1.279	1.458	V
I_{EN}	EN input hysteresis current	V_{EN} > 1.279V	-	-21	-	µA
Soft-Start						
t_{SS}	Internal soft-start time	From rising edge of EN to 80% of V_{OUT}	-	1.6	-	ms
I_{SS}	SS pin source current	V_{SS} = 0V	40	50	60	µA
I_{SS-DIS}	SS discharge current		-	-200	-	µA

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (4)	MAX (1)	UNIT
Efficiency						
η	Efficiency	V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A	-	87	-	%
		V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 5A	-	81	-	%
		V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1A	-	91	-	%
		V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A	-	80	-	%
		V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 5A	-	76	-	%
Input current						
I_Q	Input quiescent current	V_{FB} = 0.86V (7)	-	2.6	-	mA
I_{SD}	Shutdown quiescent input current	V_{EN} = 0V	-	70	-	µA

RELIABILITY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (4)	MAX (1)	UNIT
MTBF(8)	Mean Time Between Failures			$3.46 \cdot 10^7$		h

RoHS, REACh

RoHS Directive	COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK	Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACh Directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorisation and Restriction of Chemicals (REACh)

PACKAGE SPECIFICATIONS

MOLD COMPOUND				WEIGHT
Part Number	**Material**	**UL Class**	**Certificate Number**	
171050601	EME-G760	UL94V-0	E41429	1.54 g

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NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.
(3) JEDEC J-STD020
(4) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.
(5) Depending on heat sink design, number of PCB layers, copper thickness and air flow.
(6) Measured on a 8cm x 8cm four layer PCB, 104µm copper on outer layers and 70µm copper on inner layers, sixty 10mil (254µm) thermal vias, no air flow, and 1W power dissipation
(7) Module ON (Enable floating or high), feedback voltage applied by external source → no PWM switching
(8) Using Bellcore TR332 Model, 50% stress, TA = 40°C, no device burn-in.

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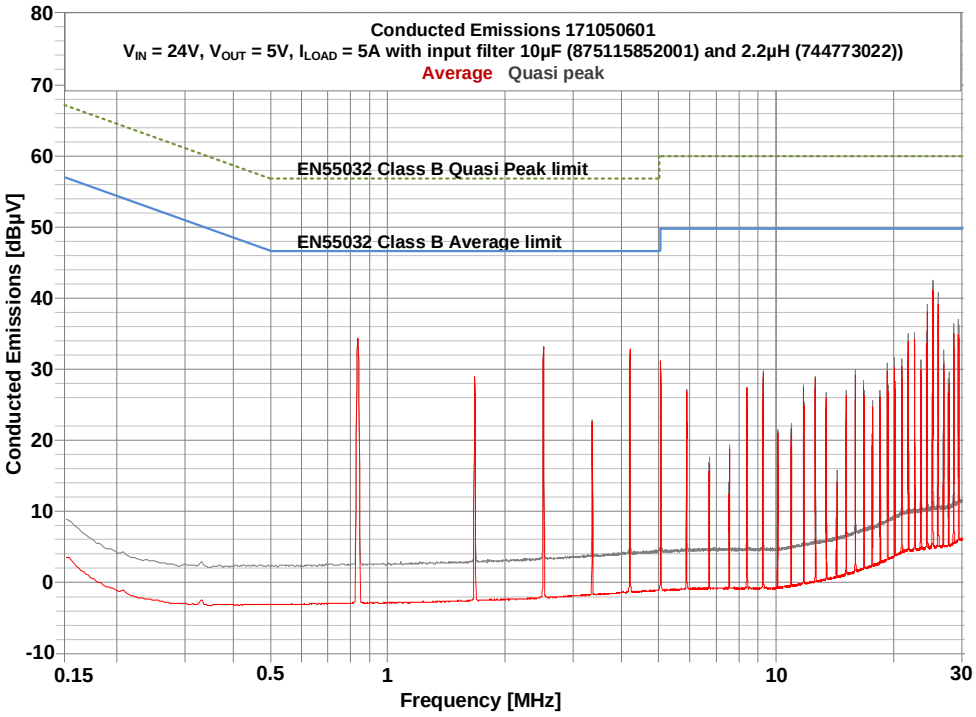
TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 2x10µF (X5R ceramic); C_{OUT} = 2x22µF (ceramic) and 100µF (Polymer), T_{AMB} = 25°C.

RADIATED AND CONDUCTED EMISSIONS (WITH EMI INPUT FILTER)

The 171050601 power module is tested with two EMC configurations (long and short wires between the module and the load) to give more realistic information about implementation in the applications. The test setup is based on CISPR16 with the limit values CISPR32.
Input wire length: 80cm.



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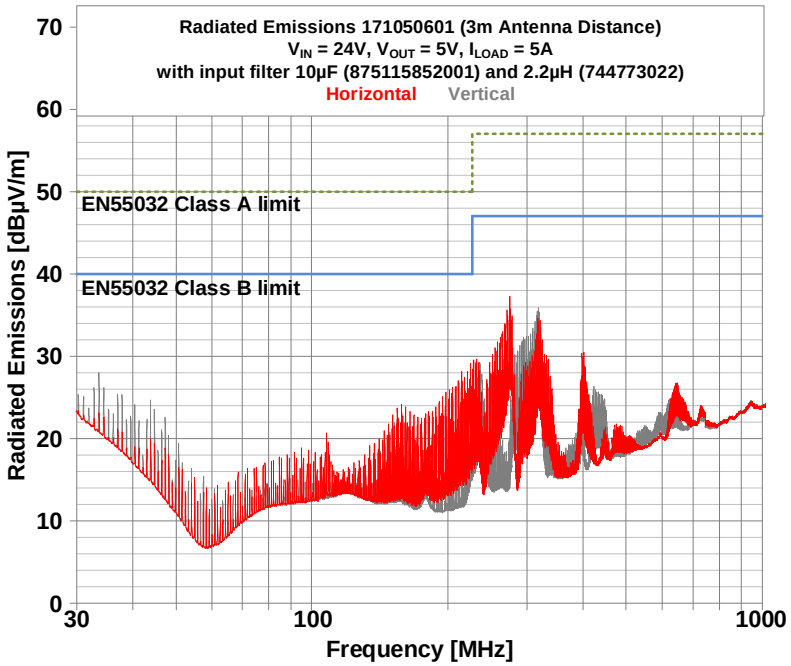
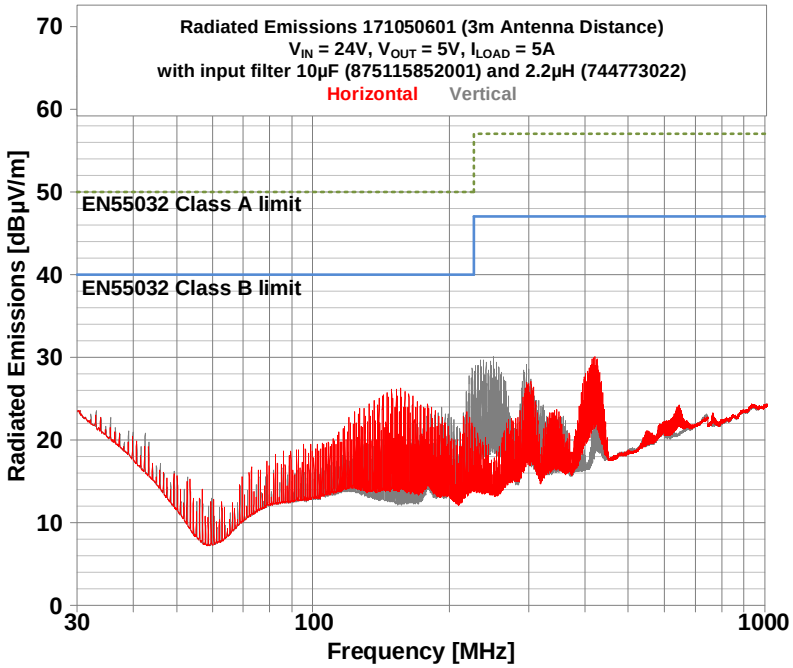
Load connected with 1m wire length



Load directly connected to the board



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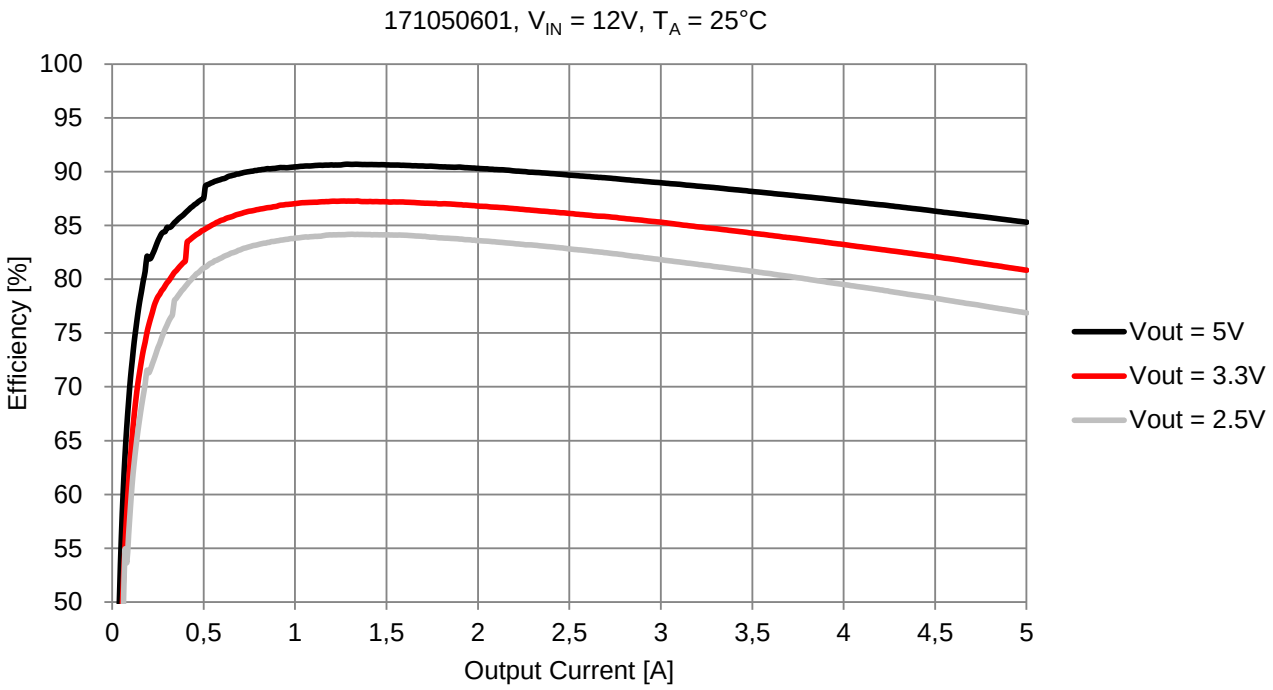
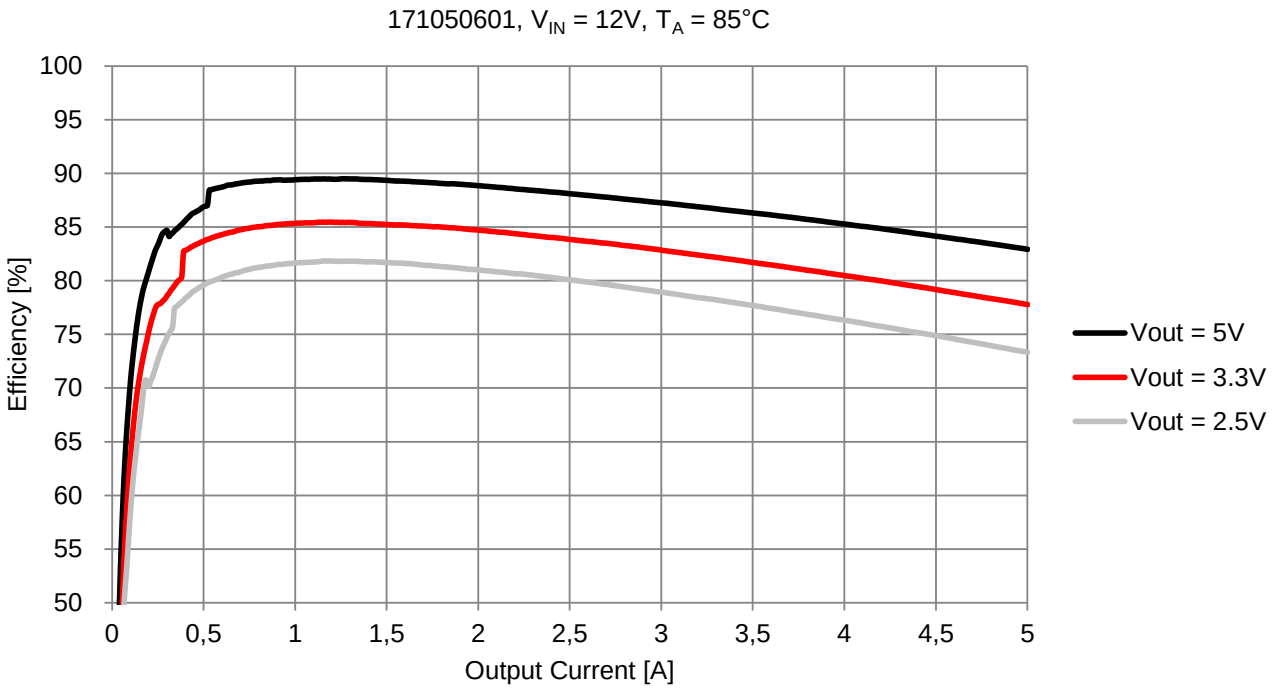
EFFICIENCY





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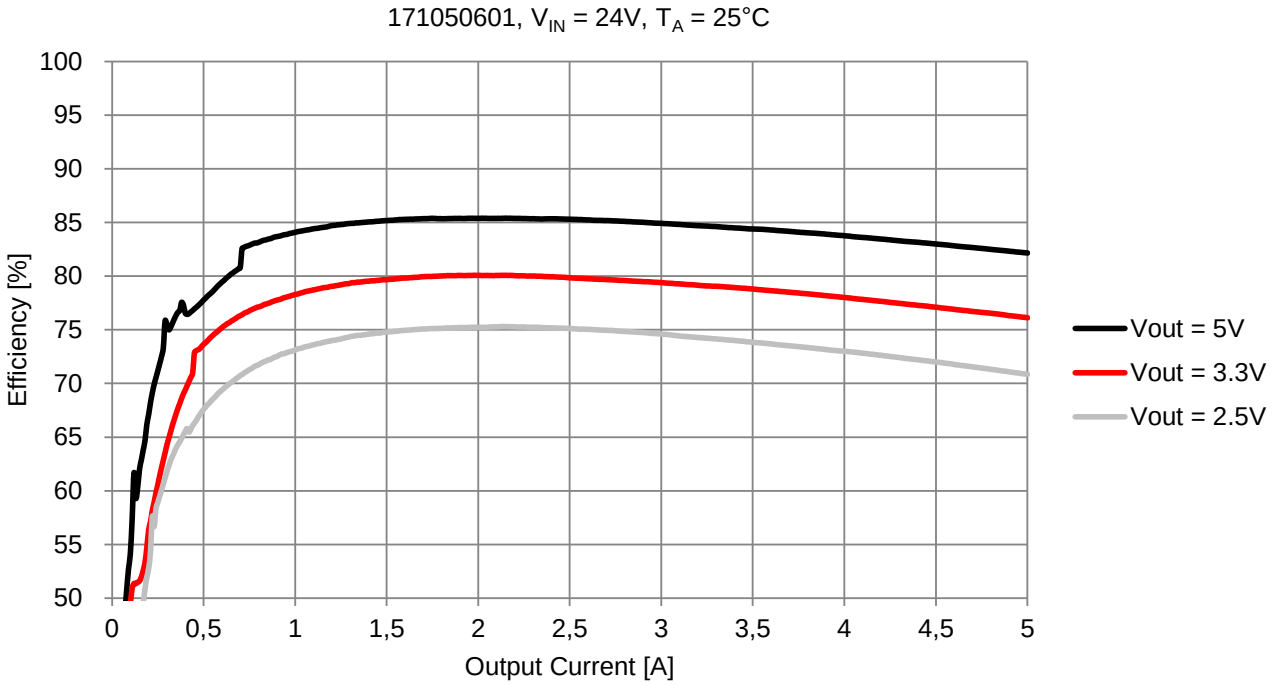
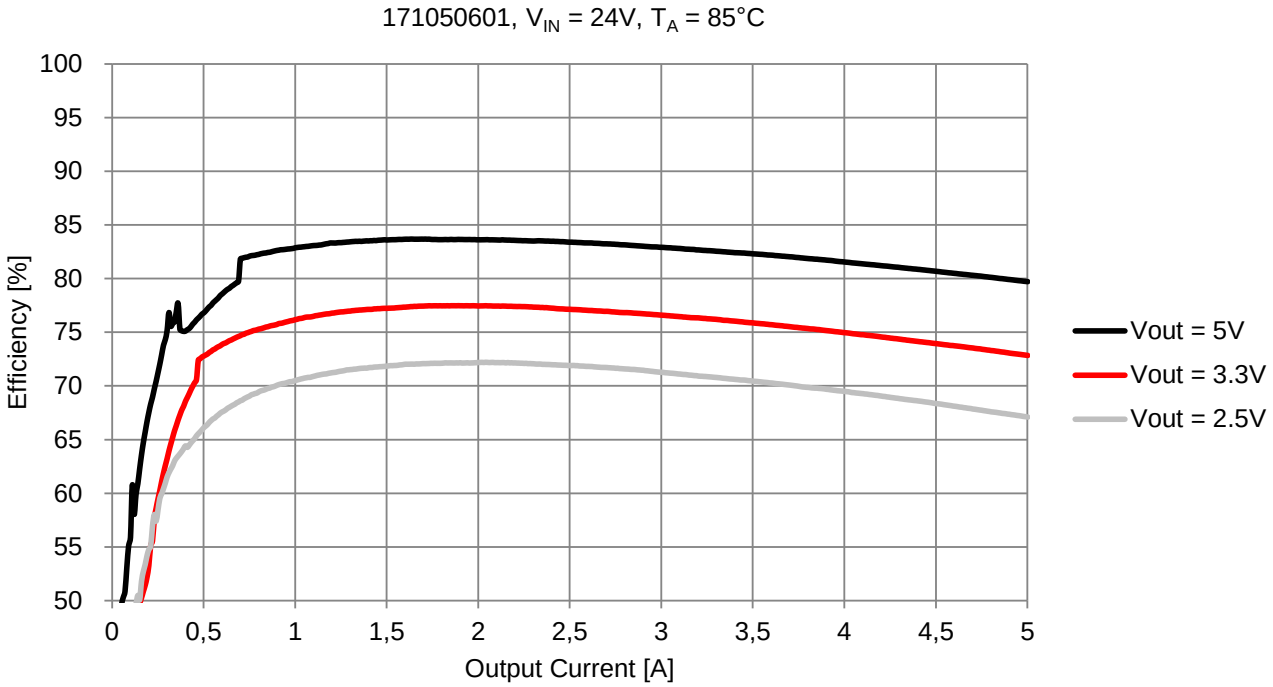
EFFICIENCY





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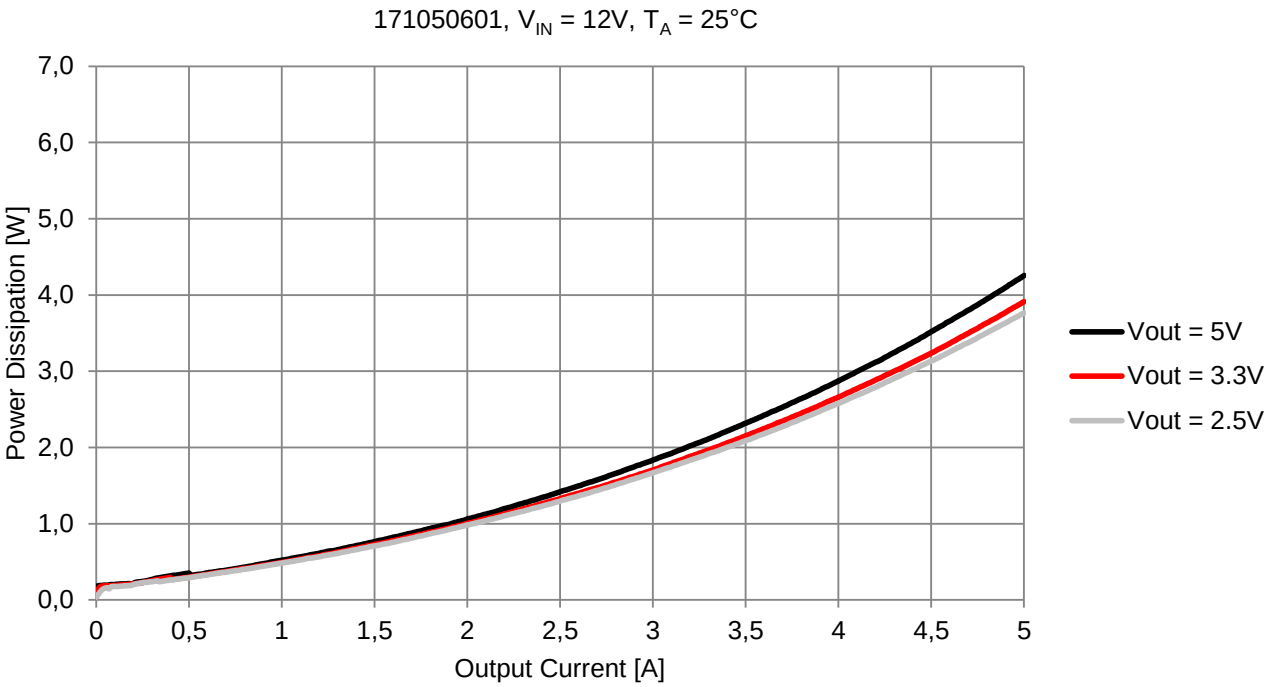
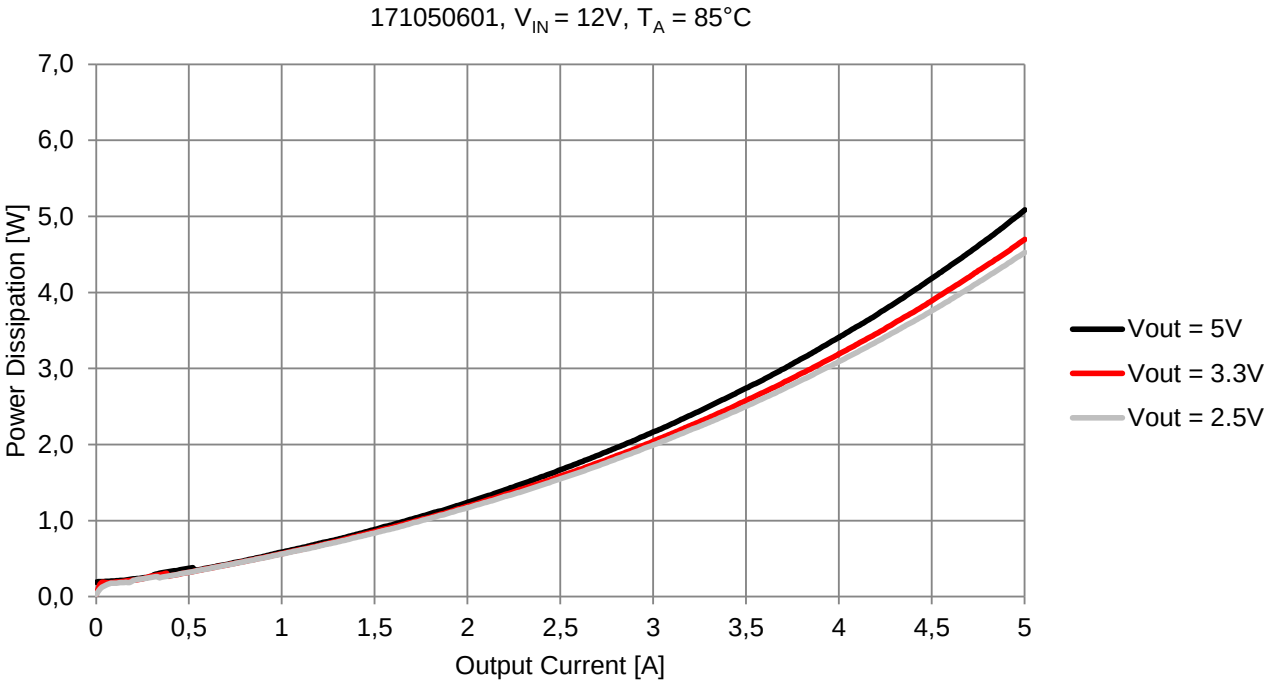
POWER DISSIPATION





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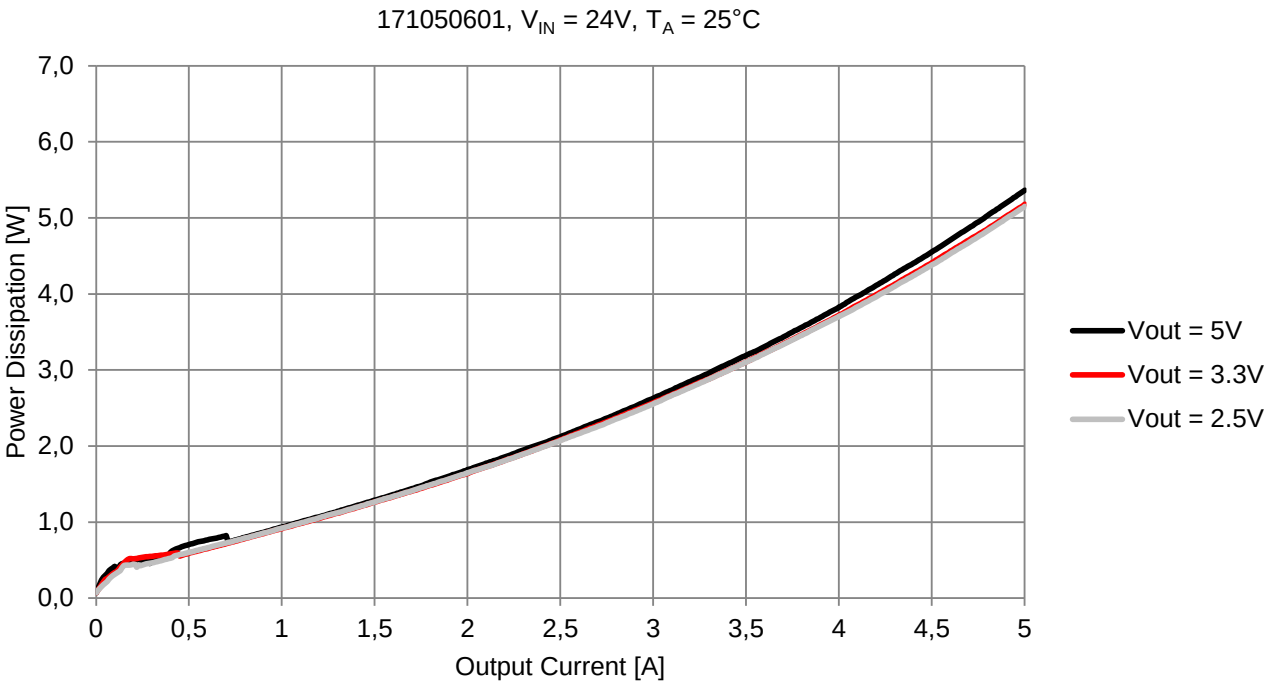
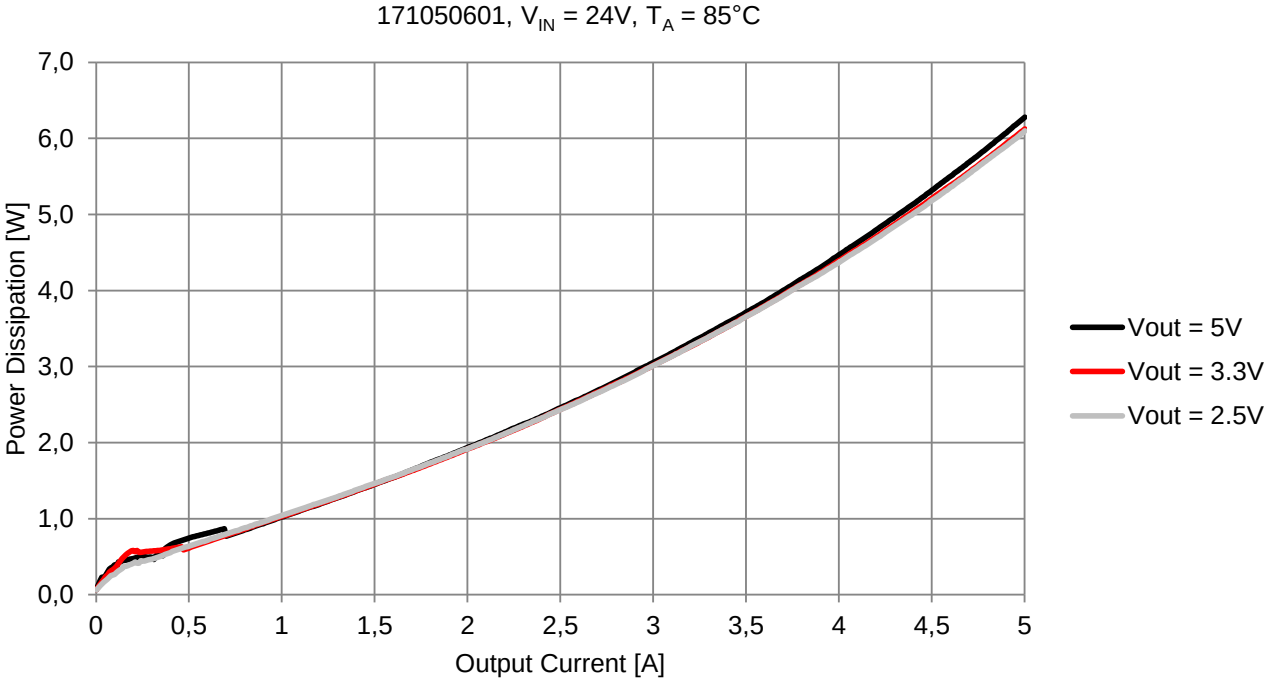
POWER DISSIPATION





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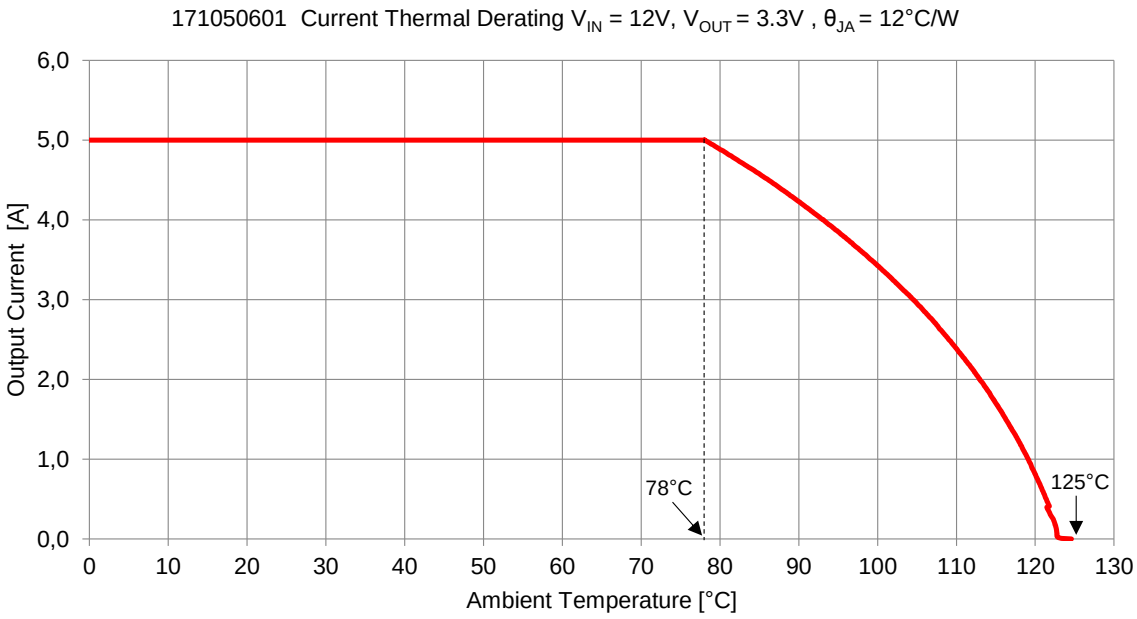
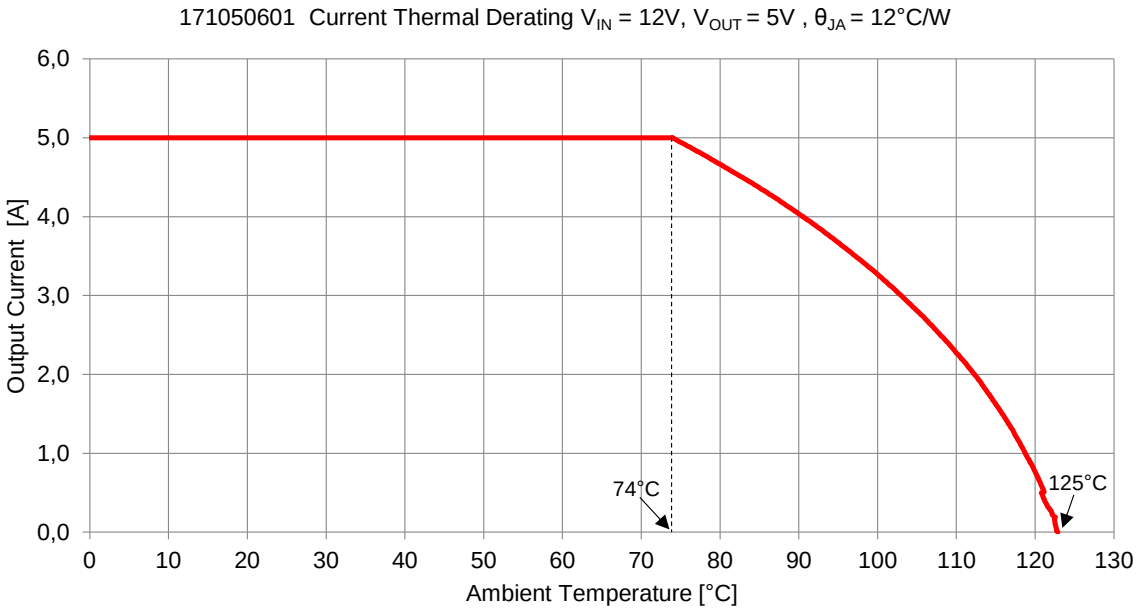
OUTPUT POWER DERATING





The ambient temperature and the power limits of the derating curve represent the operation at the max junction temperature specified in the "Operating Conditions" section on page 4.

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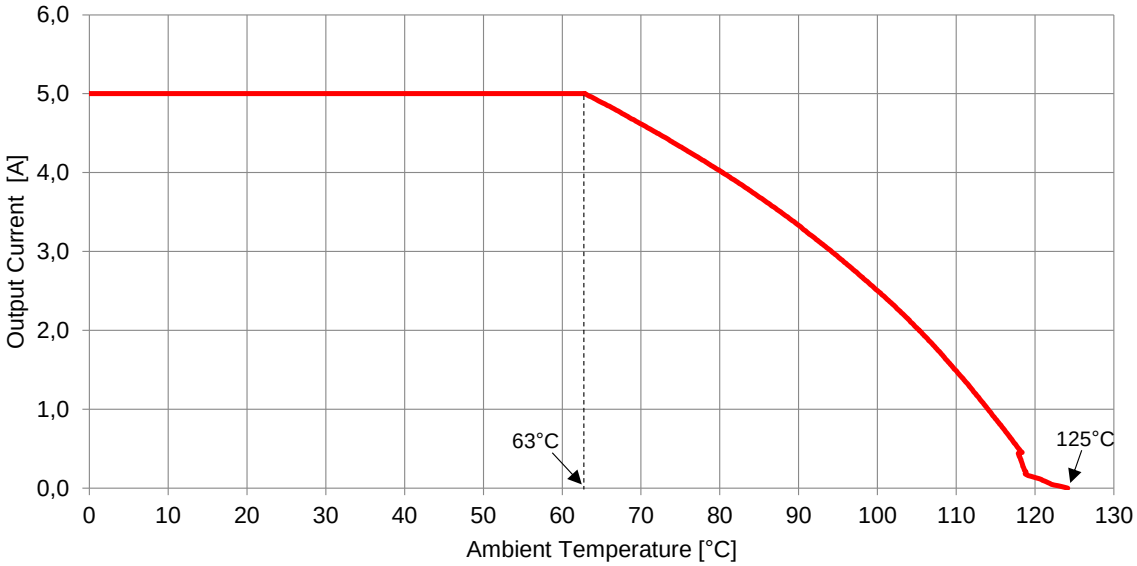
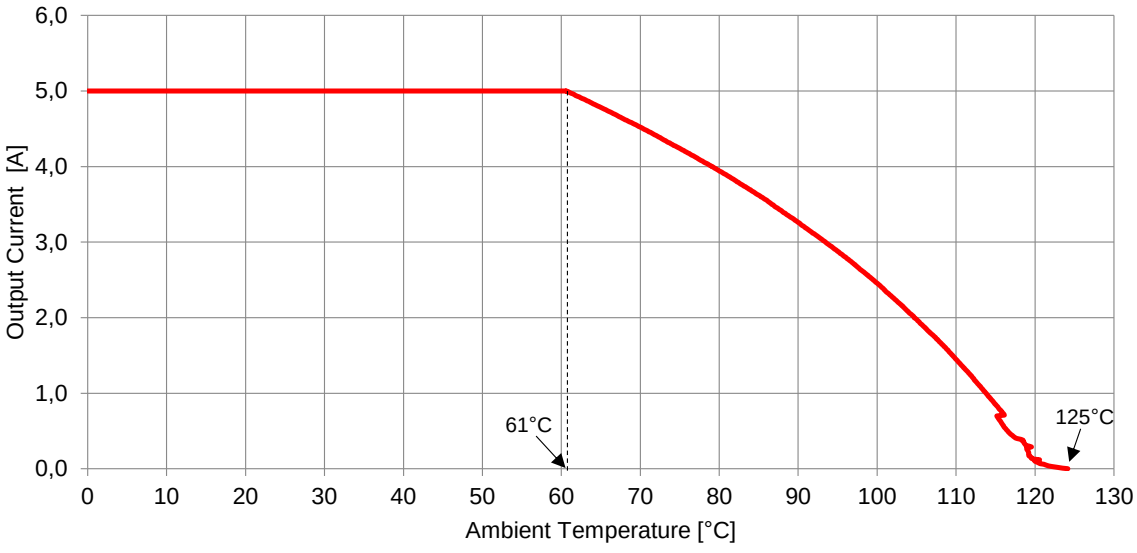
171050601 Current Thermal Derating V_{IN} = 24V, V_{OUT} = 3.3V , θ_{JA} = 12°C/W



171050601 Current Thermal Derating V_{IN} = 24V, V_{OUT} = 5V , θ_{JA} = 12°C/W



The ambient temperature and the power limits of the derating curve represent the operation at the max junction temperature specified in the "Operating Conditions" section on page 4.

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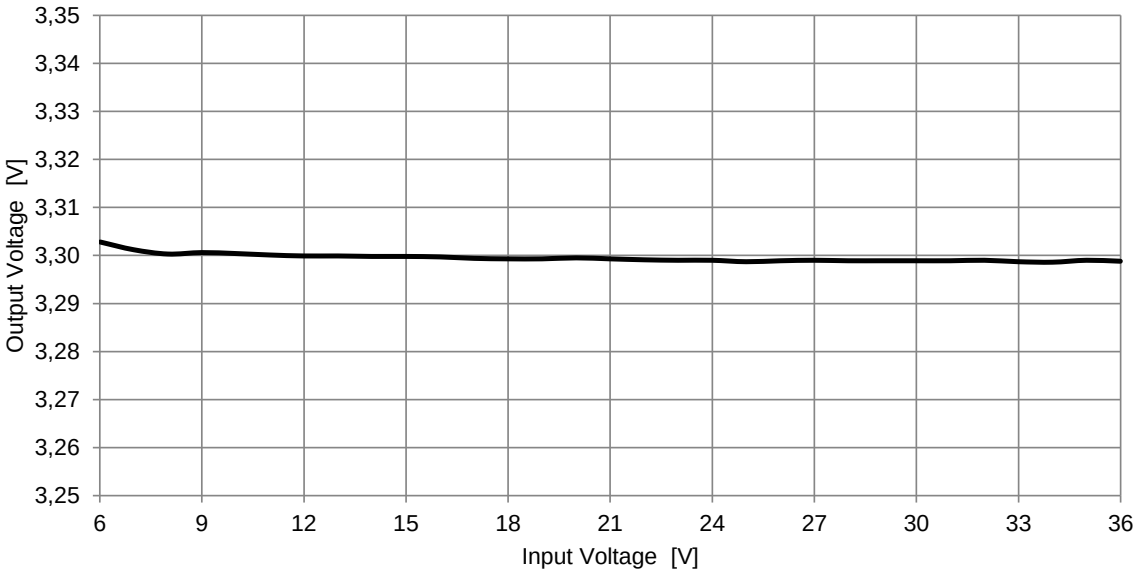
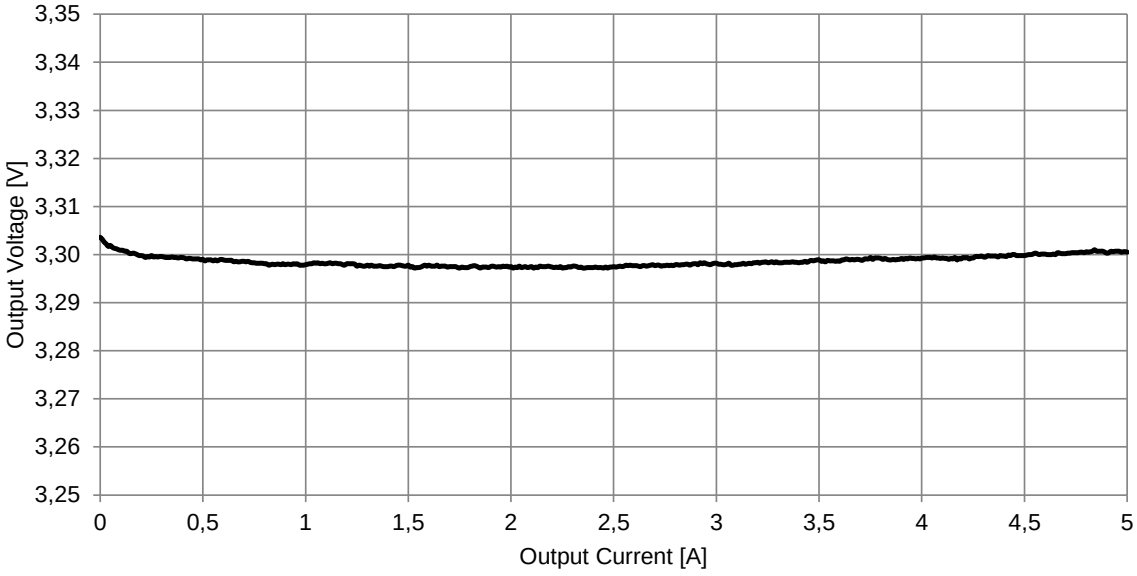
LINE AND LOAD REGULATION

171050601 Line Regulation V_{OUT} = 3.3V, I_{OUT} = 5A T_A = 25°C



171050601 Load Regulation V_{IN} = 24V, V_{OUT} = 3.3V, T_A = 25°C



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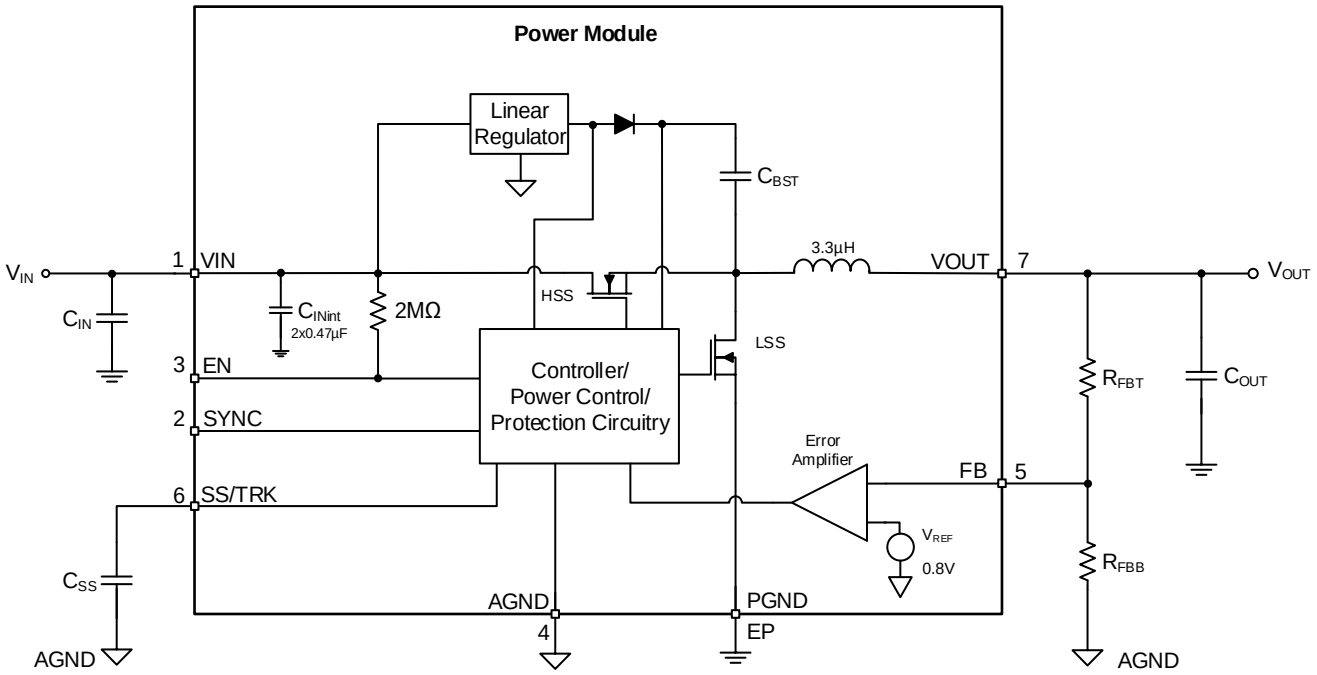
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module 171050601 consists of a synchronous step down regulator with integrated MOSFETs and a power inductor. The control scheme is based on a Current Mode (CM) regulation loop.

The V_{OUT} of the regulator is divided with the feedback resistor network R_{FBT} and R_{FBB} and fed into the FB pin. The error amplifier compares this signal with the internal 0.796V reference. The error signal is amplified and controls the on-time of a fixed frequency pulse width generator. This signal drives the power MOSFETs.

The Current Mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output voltage ripple values (< 10mV) are achieved.

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DESIGN FLOW

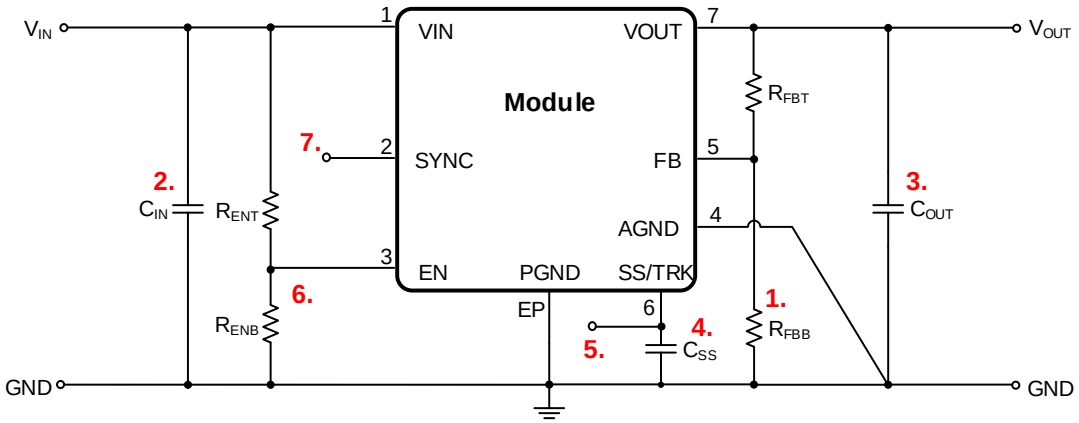
The next 7 simple steps will show how to select the external components to design your power application.

Essential Steps

1. Set the output voltage
2. Select the input capacitor
3. Select the output capacitor
4. Select the soft-start capacitor

Optional Steps

5. Voltage tracking
6. Select the under voltage lockout divider
7. Synchronization to an external clock



Step 1 Set the output voltage (V_{OUT})

The output voltage is determined by a divider of two resistors connected between V_{OUT} and ground. The midpoint of the divider is connected to the FB input. The ratio of the feedback resistors for a desired output voltage is:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{V_{OUT}}{V_{FB}}\right) - 1 \qquad (1)$$

Where V_{FB} = 0.796V (see “Electrical Specifications” on page 5). These resistors should be chosen from values in the range of 1kΩ to 20kΩ.
For V_{OUT} = 0.8V the FB pin can be connected to the output directly and R_{FBB} can be set to 8.06kΩ to provide minimum output load (for V_{OUT} < 2.5V). A table of values for R_{FBT} and R_{FBB}, is included in the “Typical Schematic” section (page 39).

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Step 2 Select the input capacitor (C_{IN})

The MagI³C power module internally contains two ceramic capacitors of 0.47µF each. The module requires additional, external input capacitance to handle the input current ripple. This input capacitance should be located as close as possible to the MagI³C power module. Input capacitor selection is generally based on different requirements. The first criterion is the input current ripple. Worst case input current ripple rating is dictated by the equation:

$$I_{C_{INRMS}} \approx \frac{1}{2} \cdot I_{OUT} \cdot \sqrt{\frac{D}{1-D}} \qquad (2) \qquad \text{where} \quad D \approx \frac{V_{OUT}}{V_{IN}}$$

As a point of reference, the worst case current ripple will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_{OUT}$.

Recommended minimum input capacitance is 22µF (including derating) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is strongly recommended to pay attention to the voltage and temperature deratings of the capacitor selected. It should be noted that current ripple rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

The second criterion is the input voltage ripple.
If the system design requires a certain minimum value of peak-to-peak input voltage ripple ($V_{IN\ ripple}$) then the following equation may be used:

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1 - D)}{f_{SW(CCM)} \cdot (V_{IN\ ripple} - ESR \cdot I_{OUT} \cdot D)} \qquad (3)$$

The duty cycle is theoretically defined as the ratio between the output and the input voltage. In reality, the efficiency should also be taken into consideration when calculating the duty cycle, as shown by the following formula:

$$D = \frac{V_{OUT}}{V_{IN} \cdot \eta} \qquad (4)$$

where η represents the efficiency and its value under the specified conditions can be found in the "Efficiency" section on page 10.

As example, if $\Delta V_{IN} \leq 100mV$ for a 12V input to 5V output application, $I_{OUT} = 5A$, reading the efficiency from the diagram on page 10 (85%) and assuming ESR = 5mΩ, this leads to:

$$C_{IN} \geq \frac{5A \cdot \frac{5V}{12V \cdot 0.85} \cdot (1 - \frac{5V}{12V \cdot 0.85})}{812000Hz \cdot 0.1V}$$

$$C_{IN} \geq 17.5\mu F$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects between the input capacitance and parasitic inductance of the incoming supply lines.

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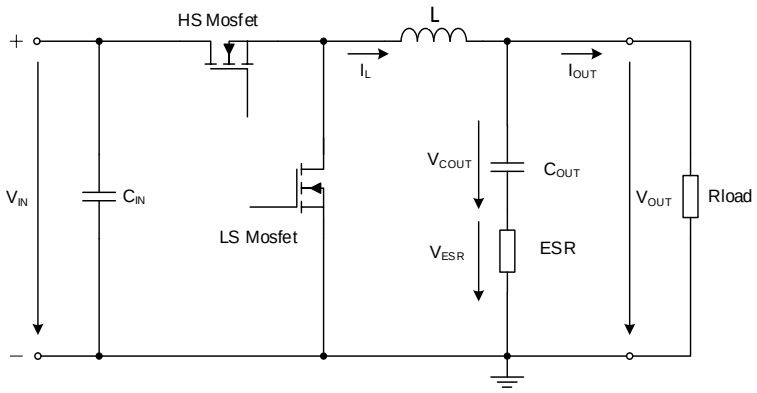
Step 3 Select the output capacitor (C_{OUT})



None of the required output capacitors are integrated within the module. A general recommendation in order to guarantee a stable behavior is to place at least 200µF at the output.The output capacitor must meet the worst case RMS current rating of $0.5 \cdot \Delta I_L$, as calculated by equation (5).

$$I_{C_{OUTRMS}} = \frac{\Delta I_L}{\sqrt{12}} \quad (5)$$

where ΔIL is the inductor current ripple calculated with the equation (6):

$$\Delta I_L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{f_{SW} \cdot L \cdot V_{IN}} \quad (6)$$

Selection by output voltage ripple requirements

The capacitor should be selected in order to minimize the output voltage ripple and provide a stable voltage at the output. Under steady state conditions, the voltage ripple observed at the output can be defined as:

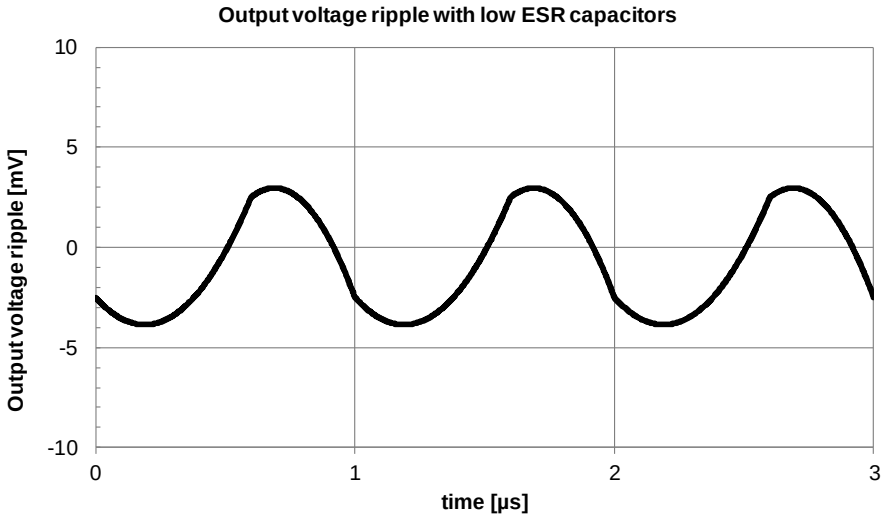
$$V_{OUT\ ripple} = \Delta I_L \cdot ESR + \Delta I_L \cdot \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \quad (7)$$

Very low ESR capacitors, like ceramic and polymer electrolytic, are recommended. If a low ESR capacitor is selected, equation (7) can be simplified and a first condition for the minimum capacitance value can be derived:

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot V_{OUT\ ripple} \cdot f_{SW}} \quad (8)$$

Beyond that, additional capacitance will reduce output ripple as long as the ESR is low enough to permit it. Please consider the derating of the nominal capacitance value due to temperature, aging and applied DC voltage (only for MLCC, e.g. X7R up to -50%).

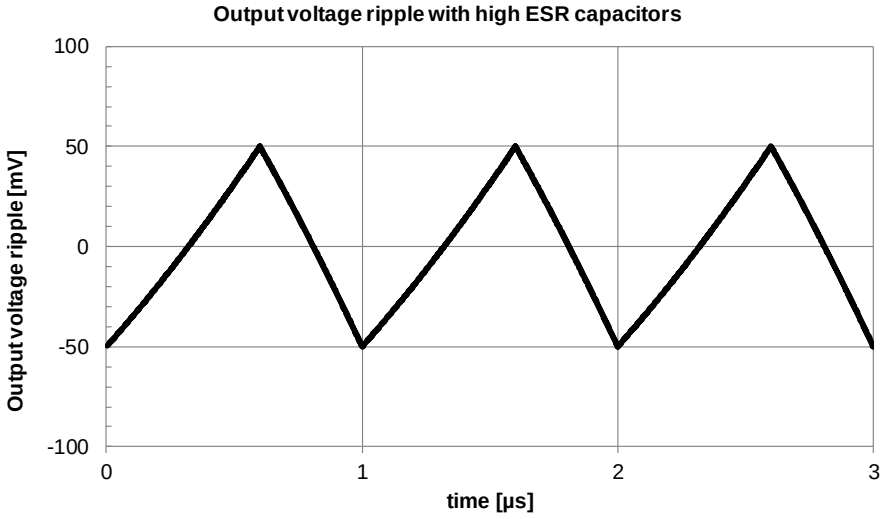
The use of very low ESR capacitors leads to an output voltage ripple as shown below:



When capacitors with slightly higher ESR are utilized, the dominant parameter which influences the output voltage ripple is just the ESR:

$$ESR \leq \frac{V_{OUT\ ripple}}{\Delta I_L} \quad (9)$$

Consequently, the shape of the output voltage ripple changes, as shown below:



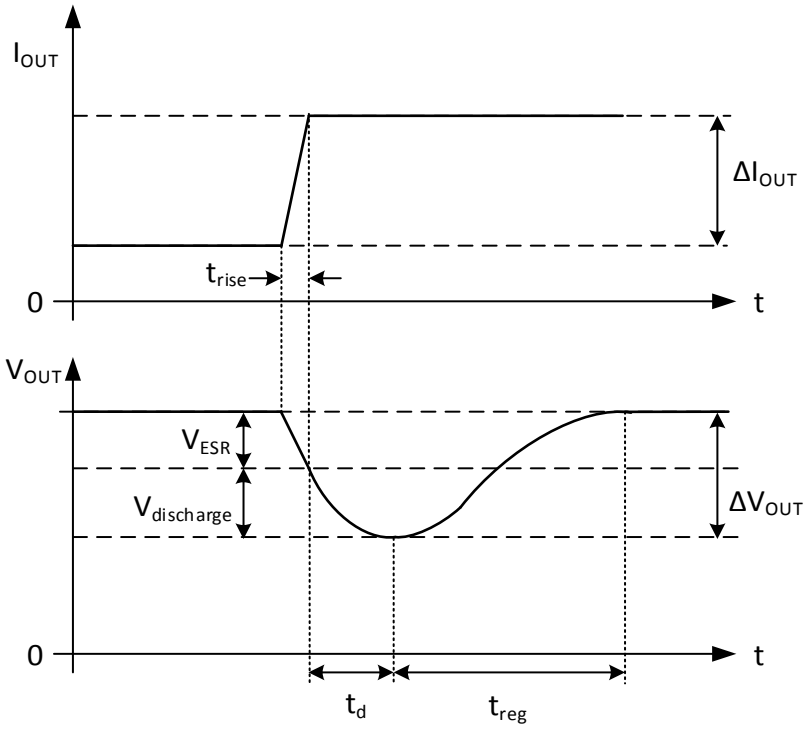
Selection by load step requirements

The output voltage is also affected by load transients (see picture below).

When the output current transitions from a low to a high value, the voltage at the output capacitor (V_{OUT}) drops. This involves two contributing factors. One is caused by the voltage drop across the ESR (V_{ESR}) and depends on the slope of the rising edge of the current step (t_{rise}). For low ESR values and small load currents, this is often negligible. It can be calculated as follows:

$$V_{ESR}=ESR\cdot\Delta I_{OUT} \quad (10)$$

where ΔI_{OUT} is the load step, as shown in the picture below (simplified: no voltage ripple is shown).



The second contributing factor is the voltage drop due to discharge of the output capacitor, which can be estimated as:

$$V_{discharge}=\frac{\Delta I_{OUT}\cdot t_d}{2\cdot C_{OUT}} \quad (11)$$

In a current mode architecture the t_d is strictly related to the bandwidth of the regulation loop and influenced by the C_{OUT} (if C_{OUT} increases, the t_d increases as well).

For this power module a minimum value of 200µF is recommended to keep the loop stable.

In order to choose the value of the output capacitor, the following steps should be utilized:

1. Start with the minimum C_{OUT} recommended (200µF), essential for a stable operation.
2. Measure t_d.
3. Calculate the appropriate value of C_{OUT} for the maximum voltage drop $V_{discharge}$ allowed at a defined load step, using the following equation (12), derived from equation (11):

$$C_{OUT} \geq \frac{\Delta I_{OUT} \cdot t_d}{2 \cdot V_{discharge}} \quad (12)$$

4. As mentioned above, changing C_{OUT} affects also t_d. Therefore, step 2 and step 3 should be repeated to find the best performance.

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Example
The following application conditions are used as an example to show how to calculate a suitable C_{OUT} value:

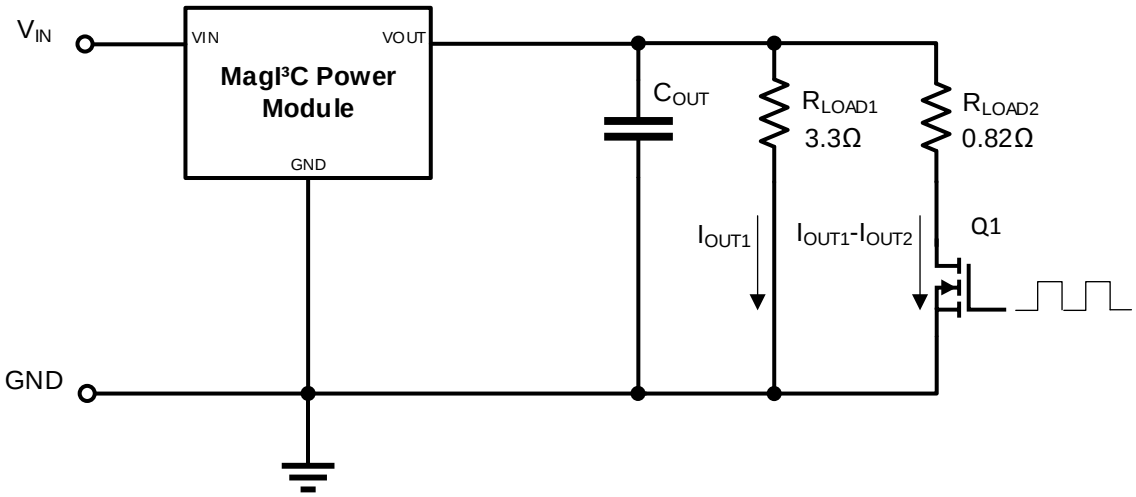
- V_{IN} = 12V
- V_{OUT} = 3.3V
- load transient from 1A to 5A and vice versa (ΔI_{OUT} = 4A)
- max allowed undershoot or overshoot ΔV_{OUT} = 100mV

C_{OUT} can be calculated using equation (12) on page 23. This equation provides two possible values depending on whether t_d is calculated for a positive load transient (generating a V_{OUT} drop) or for a negative load transient (resulting in a V_{OUT} overshoot).
A combination of two 22µF MLCC (Würth Elektronik, part number 885012108018) together with a 220µF aluminum polymer capacitor (Würth Elektronik, part number 875115350002) are selected. Some margin from the calculated C_{OUT} value is recommended in order to take into account:

- Approximations within the equations to estimate t_d and C_{OUT} itself;
- Tolerances and variations of some components and parameters involved in those equations (e.g. R_{ON}, $t_{OFF-MIN}$, L, k, etc.)
- Derating of the capacitors with DC applied voltage and temperature

The use of two MLCCs in parallel contributes to the further reduction of the total ESR. The selected combination of output capacitors allows for stable operation and provides a phase margin around 65°.

The load transients with the selected C_{OUT} can be tested using the setup depicted below. The resistor R_{LOAD1} sets the lower current value of the transient (I_{OUT1}). In order to reach the higher current value (I_{OUT2}) the resistor R_{LOAD2} is switched through a N-Channel MOSFET. A square waveform applied to the gate of this MOSFET generates continuously load transients between I_{OUT1} and I_{OUT2} and conversely.



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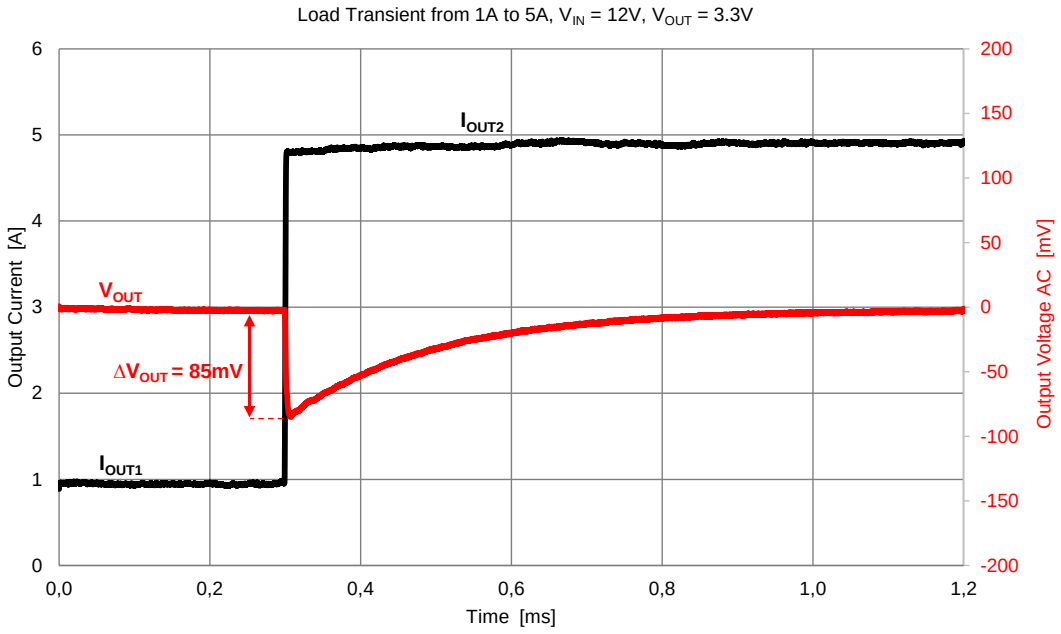
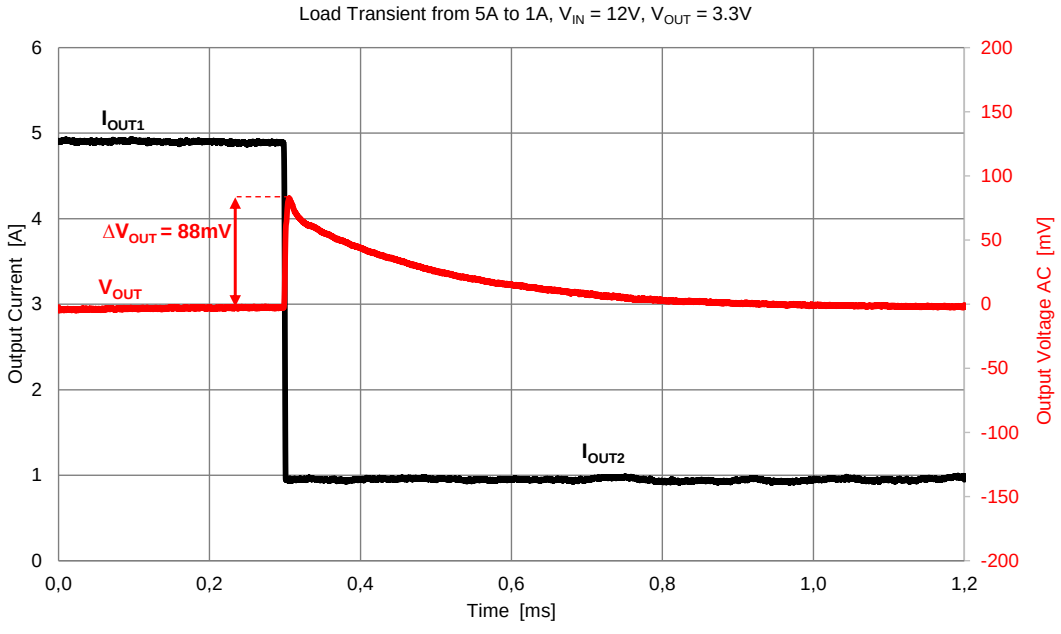
The results of the load transient tests with the selected C_{OUT} are shown below:





In both the positive and the negative transition, the ΔV_{OUT} is below the target (100mV). The explanation of the strong reduction of the ΔV_{OUT} lies in the use of a capacitance value higher than the one calculated.

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Step 4 Select the soft-start capacitor (C_{SS})

Adujstable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise time to prevent overshoot.

Upon turn-on, after all UVLO conditions have been passed, an internal 1.6ms circuit slowly ramps the SS/TRK input to implement internal soft start. If the preset soft-start time is enough for the application, the SS/TRK can be left floating. Longer soft-start periods are achieved by adding an external capacitor to this pin.

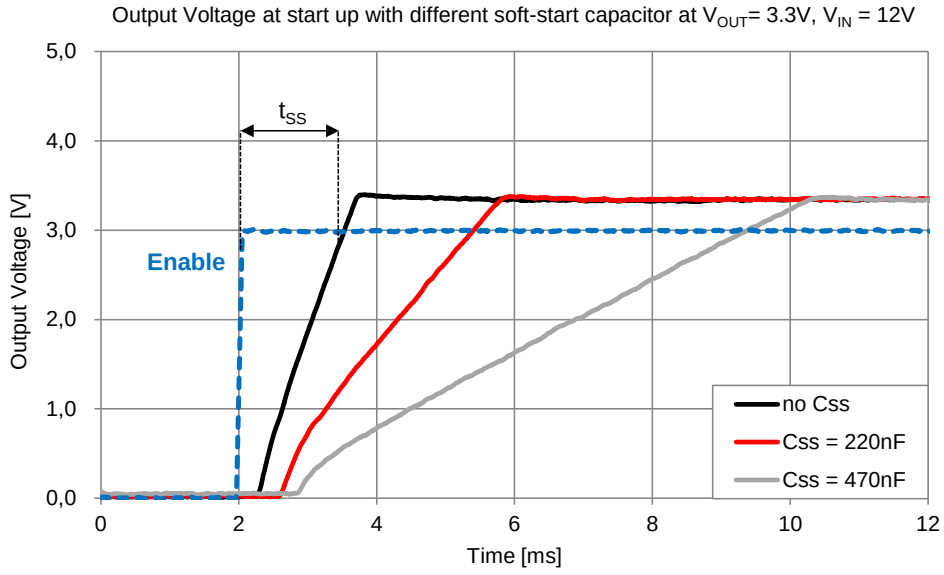
Soft-start duration is given by the formula:

$$C_{SS} = t_{SS} \cdot \frac{I_{SS}}{V_{FB}} \qquad (13)$$

where t_{SS} corresponds to the soft-start time in milliseconds, I_{SS} (50µA) is the current flowing out of the SS/TRK during start-up and V_{FB} = 0.796.
Using a 220nF capacitor results in 3.5ms typical soft-start duration; and 470nF results in 7.5ms typical. 470nF is a recommended initial value. As the soft-start input exceeds 0.796V the output of the power stage will be in regulation and the 50µA current is deactivated. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The enable input being “pulled low”
- Thermal shutdown condition
- Internal V_{CC} UVLO (Approx 4.3V input to V_{IN})

The output voltage rising waveforms with different soft-start capacitors are shown in the diagram below.



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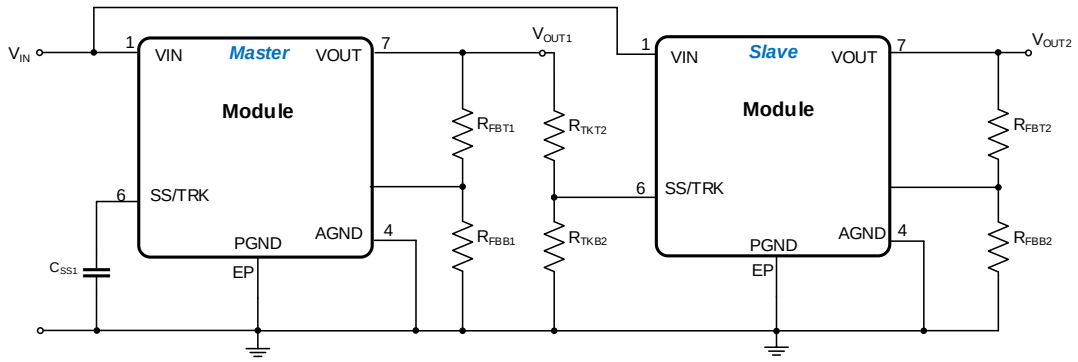
Step 5 Optional: Voltage tracking

The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3V system rail) where the slave module output voltage is lower than that of the master. The schematic below illustrates the general idea of connecting two power modules in a master-slave configuration.



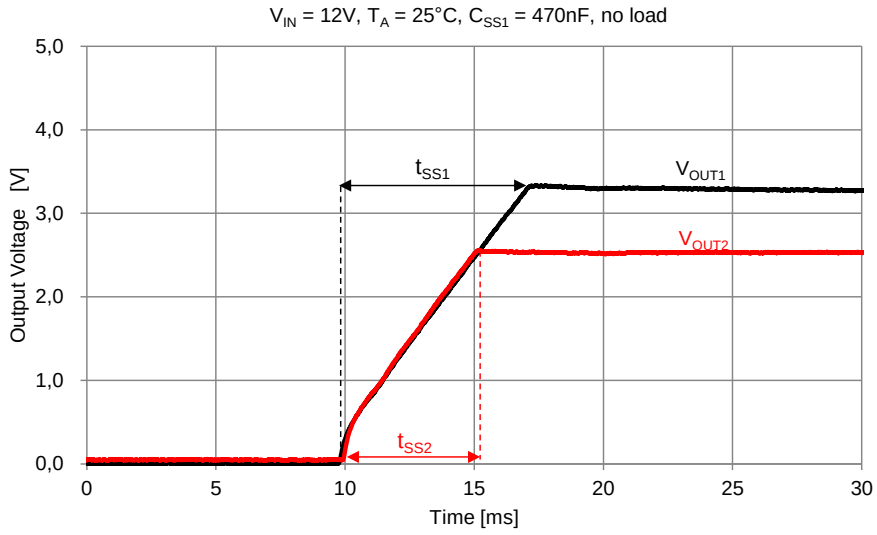
Proper configuration of the tracking resistor divider (R_{TKT2} and R_{TKB2}) at the slave module allows for implementing simultaneous or ratiometric output tracking. The tracking function is only supported during the power up interval of the master supply.

Simultaneous tracking

Simultaneous output tracking allows the slave rail to power up coincidental with the master (voltage difference between the rails during ramp-up is very small, <0.15V). The condition to implement a simultaneous tracking is:

$$\frac{R_{TKT2}}{R_{TKB2}} = \frac{R_{FBT2}}{R_{FBB2}} \qquad (14)$$

The values for the tracking resistive divider should be selected small enough to minimize the effect of the internal 50uA current source. The curve below shows the simultaneous tracking with R_{TKT2} = 1kΩ, R_{TKB2}=464Ω (for the feedback resistor divider the values of the evaluation board are used, see “Bill of Material” on page 48).



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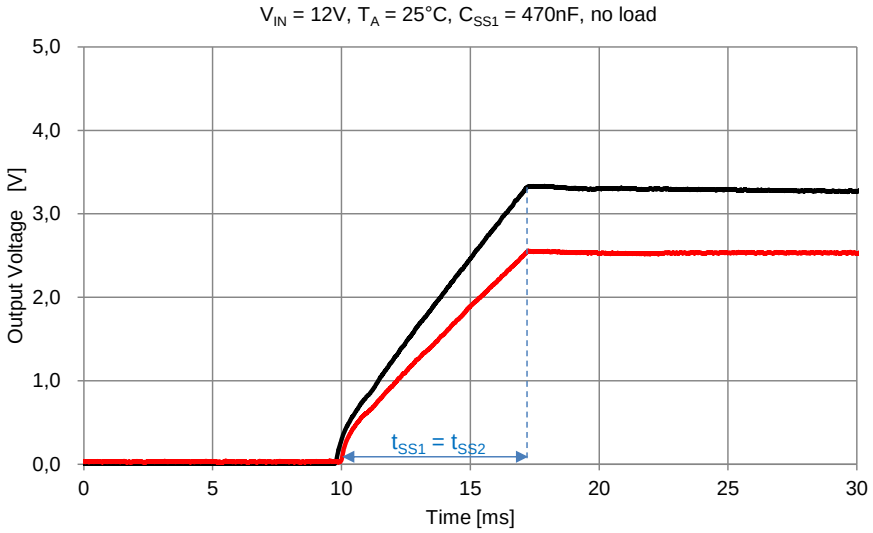
Ratiometric tracking

Ratiometric output tracking indicates that the output voltages of both the master and the slave reach their preset value at the same time. This means also that the soft-start duration is the same for both modules. The condition to implement a ratiometric tracking is:

$$\frac{R_{TKT2}}{R_{TKB2}} = \frac{R_{FBT1}}{R_{FBB1}} \quad (15)$$

The values for the tracking resistive divider should be selected small enough to minimize the effect of the internal 50uA current source. The curve below shows the ratiometric tracking with R_{TKT2} = 1kΩ, R_{TKB2}=316Ω (for the feedback resistor divider the values of the evaluation board are used, see “Bill of Material” on page 48).



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Step 6 Optional: Select the under voltage lockout divider

For applications not requiring precision under voltage lockout (UVLO), the EN input may be left open. An internal 2MΩ pull-up resistor (R_{ENint}) is connected from EN pin to VIN. It will always enable the module. In such case, the internal UVLO occurs typically at 4.3V ($V_{IN\ rising}$). In applications with separate supervisory circuits, the EN pin can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail. Enable provides a precise 1.279V threshold to allow for direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN} (see figure below, left). Additionally there is switched offset current (I_{EN}, 21µA typ.) allowing programmable hysteresis.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable UVLO. The two resistors should be chosen based on the following ratio:

$$\frac{R_{ENT}}{R_{ENB}} = \left(\frac{V_{UVLO}}{V_{EN}}\right) - 1 \qquad (16)$$

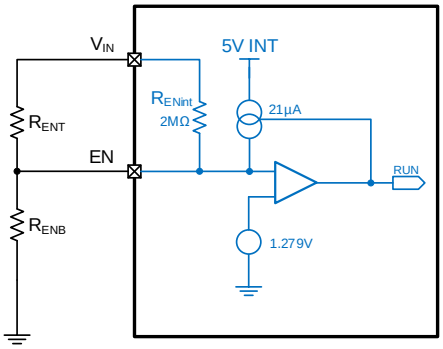
where V_{EN} is the EN threshold trip point (1.279V, see “Electrical specifications” on page 5). Equation (16) neglects the internal pull-up resistor but it is nevertheless a good approximation.
The rising threshold of the UVLO at the input voltage can be calculated as follows:

$$V_{IN(rising)} = V_{EN} \cdot \left(1 + \frac{(R_{ENT} \| R_{ENint})}{R_{ENB}}\right) \qquad (17)$$

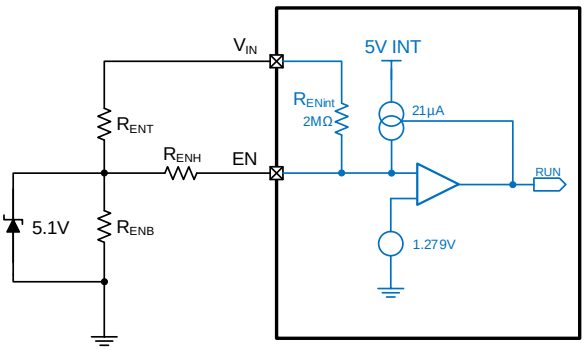
An additional hysteresis can be introduced by connecting the resistor R_{ENH} (see picture below, right). The falling threshold is therefore defined as:

$$V_{IN(falling)} = V_{IN(rising)} - I_{EN} \cdot [R_{ENT} \| R_{ENint} \| (R_{ENH} + R_{ENB})] \qquad (18)$$

A zener clamp diode might be required in order to prevent the EN input voltage from exceeding its maximum absolute rating value (6V, see “Absolute maximum ratings” on page 4).
For example, selecting R_{ENB} = 12.7kΩ and R_{ENT} = 42.2kΩ would result in a rising UVLO threshold of 5.46V. This divider however presents 8.33V to the input when the input voltage reaches its maximum value (36V), exceeding the 6V mentioned above. A midpoint 5.1V zener clamp should be used in this case to allow the application to cover the full 6V to 36V range of operation (see figure below, right).



Basic external UVLO divider



External UVLO circuit with programmable hysteresis and EN pin voltage clamp

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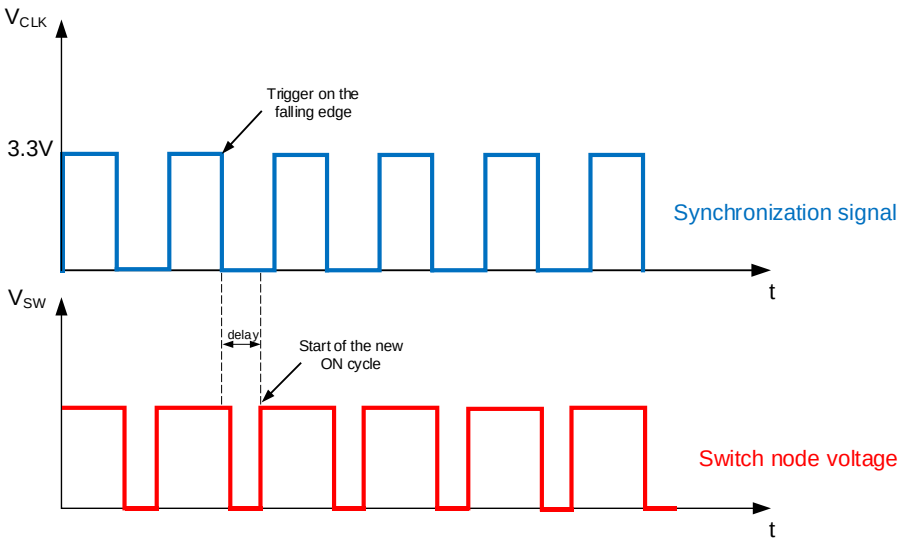
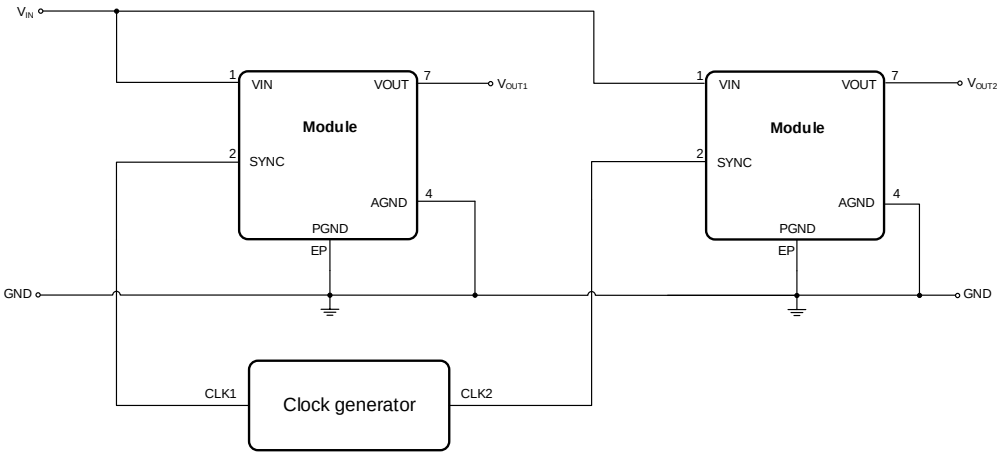
Step 7 Optional: Synchronization to an external clock

The PWM switching frequency can be synchronized to an external frequency source through the SYNC pin (see picture below). This feature helps avoiding undesired beat frequencies due to slight deviations of the default switching frequency in case more modules are present in the same system. In addition, when phase shift is implemented by using two clocks (CLK1 and CLK2), the input RMS current, and consequently input voltage ripple and input capacitance, can be reduced.
The recommended synchronization frequency range is 650kHz to 950 kHz. The typical input threshold is 1.4V transition level. Ideally, the input clock should overdrive the threshold by a factor of 2, such as direct drive from 3.3V logic source. The duty cycle of the synchronization signal should be in the range of 15% and 85%, as indicated in the "Electrical Specifications" on page 5. The module is synchronized by the falling edge of the synchronization signal after a small delay (see figure below). If this feature is not used, connect this input either directly to ground, or connect to ground through a resistor (R_{SYNC}, see "Typical schematic" section on page 39) of 1.5kΩ or less.



Note that applying a sustained "logic 1" corresponds to 0Hz PWM frequency and will cause the module to stop switching. The figure below shows how two (in this case) or more power modules can be synchronized by a clock generator.



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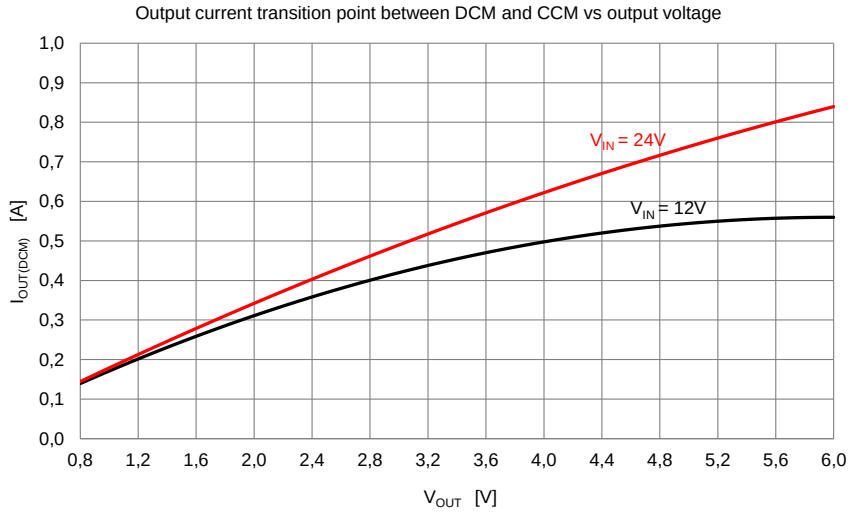
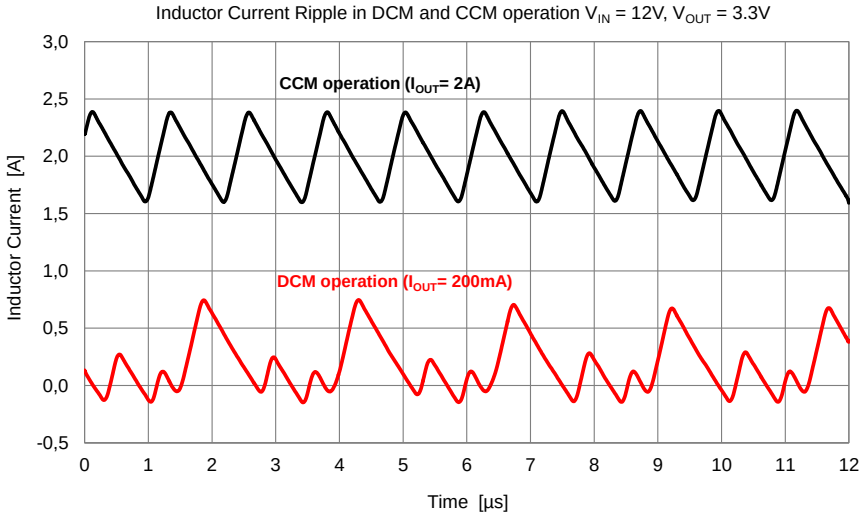
LIGHT LOAD OPERATION

Under light load operation, the device switches from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM). The load current where the transition between DCM and CCM takes place can be estimated using the following formula and illustrated by the diagram below:

$$I_{OUT(DCM)} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \cdot f_{SW} \cdot L} \quad (19)$$



In CCM, current flows through the inductor over the entire switching cycle and never falls to zero during the OFF-time (see figure below, black curve). Once the inductor current reaches zero during the OFF-time, the module starts to operate in DCM (see figure below, red curve). The output voltage ripple during this mode is typically higher than in CCM. In case of no load or load of few milliamps some switching cycle might be skipped.



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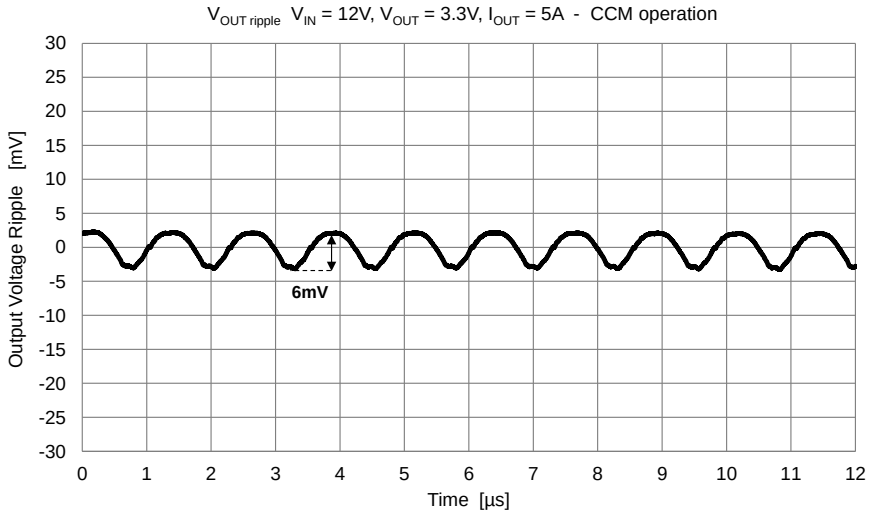
OUTPUT VOLTAGE RIPPLE

The output voltage ripple depends on several parameters, as already shown in DESIGN FLOW – Step3 on page 20. The figure below shows the V_{OUT} ripple at full load and using the output capacitors indicated in the "Bill of material" on page 48. An output voltage ripple of around 6mV is measured under the conditions indicated.



The operating mode (CCM or DCM) further influences the output voltage ripple. Normally at light load a higher output voltage ripple is expected.

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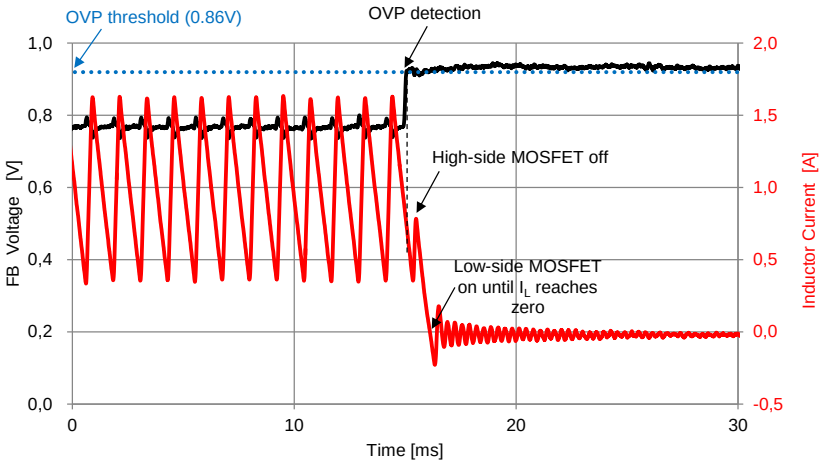
PROTECTING FEATURES

Output Over-voltage protection (OVP)

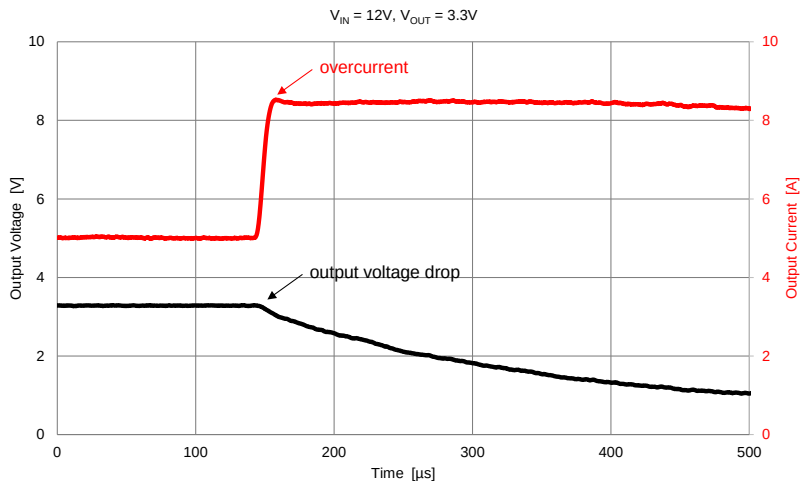
The voltage at FB is compared to a 0.86V internal reference (see “Electrical specifications” on page 5). If FB rises above 0.86V the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). Once OVP is activated, the high-side MOSFET on-time will be inhibited until the condition clears. Additionally, the low-side MOSFET will remain on until the inductor current falls to zero. Then both high-side and low-side MOSFETs are turned off as long as the overvoltage condition is not removed (see figure below).



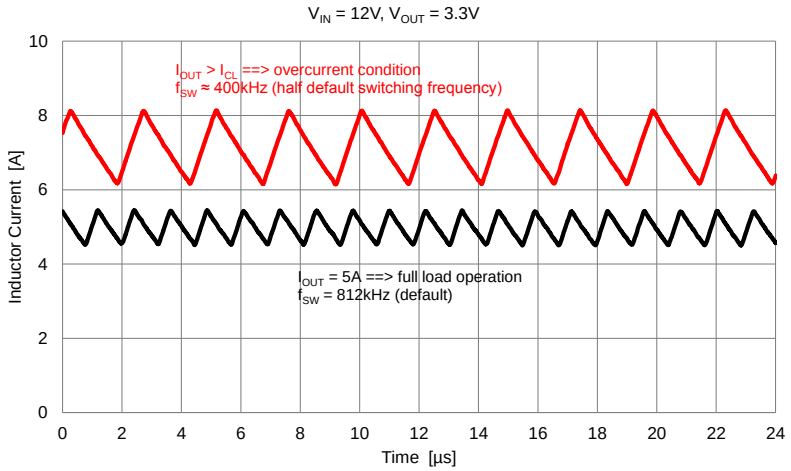
Over current protection (OCP)

The over current protection in this module is carried out by implementing both a peak current protection (high-side MOSFET) and a valley-current protection (low side MOSFET).

The peak current protection (I_{CL_HS}, 7A typical, see “Electrical Specifications” on page 5) is detected on the high side MOSFET during the on-time. When the peak current protection is triggered, the high-side MOSFET is immediately turned-off and the low side is kept on until the current falls below valley current limit threshold (I_{CL_LS}, 5.4A typical, see “Electrical Specifications” on page 5). If necessary some cycles are also skipped and this causes the output voltage to drop (see figure below).

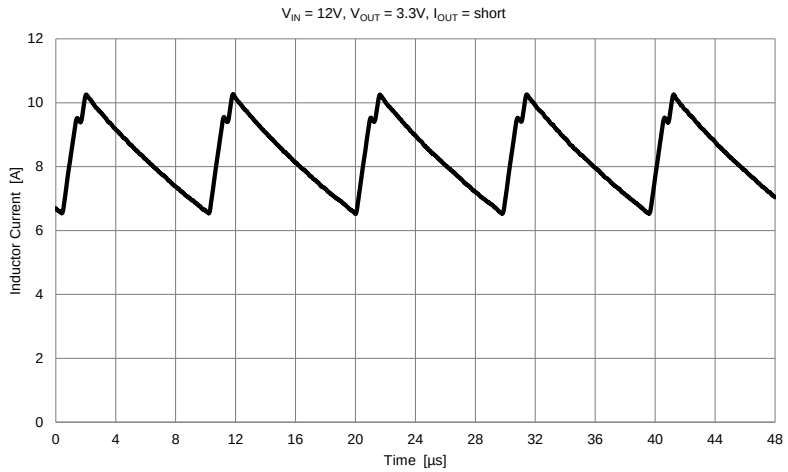


When the high-side MOSFET is turned off, the inductor current flows through the load, the PGND pin and the low-side MOSFET. If this current exceeds the valley current limit (I_{CL_LS}, 5.4A typical, see “Electrical Specifications” on page 5) the start of the next on-time period is prevented. This results in a reduced switching frequency, as shown by the figure below.



Short circuit protection

The combination of the peak and valley current limit above described offers an effective protection in case of a short circuit event. The device stops switching when the peak current limit is exceeded and starts again switching when the current falls below the valley current limit, as shown by the figure below.



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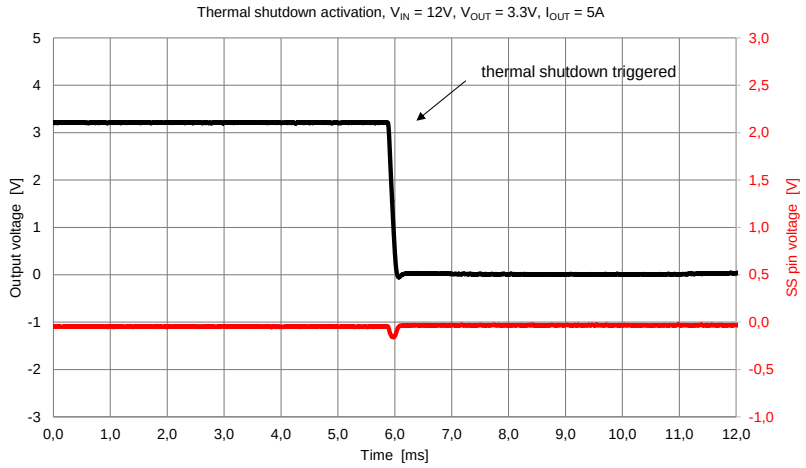
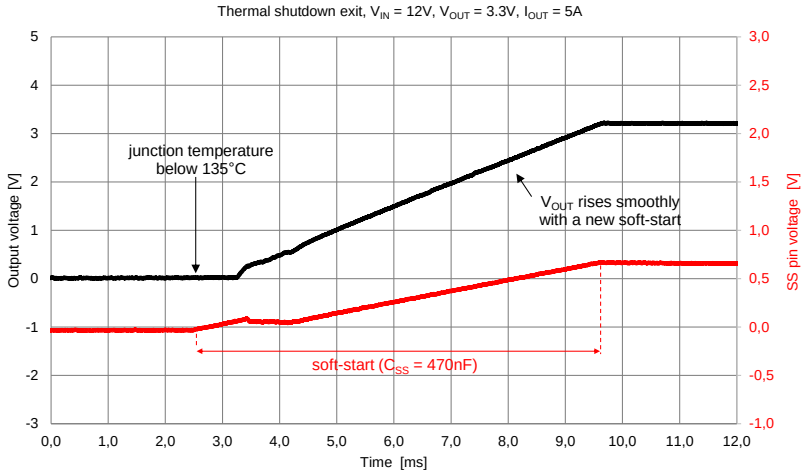
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

Over temperature protection (OTP)

The junction temperature of the MagI³C power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 165°C (typ) causing the device to enter a low power standby state. In this state the high-side MOSFET remains off causing V_{OUT} to fall (see figure below).



Thermal protection helps prevent catastrophic failures caused by device overheating. When the junction temperature falls back below 150°C (typ. hysteresis = 15°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes (see figure below).



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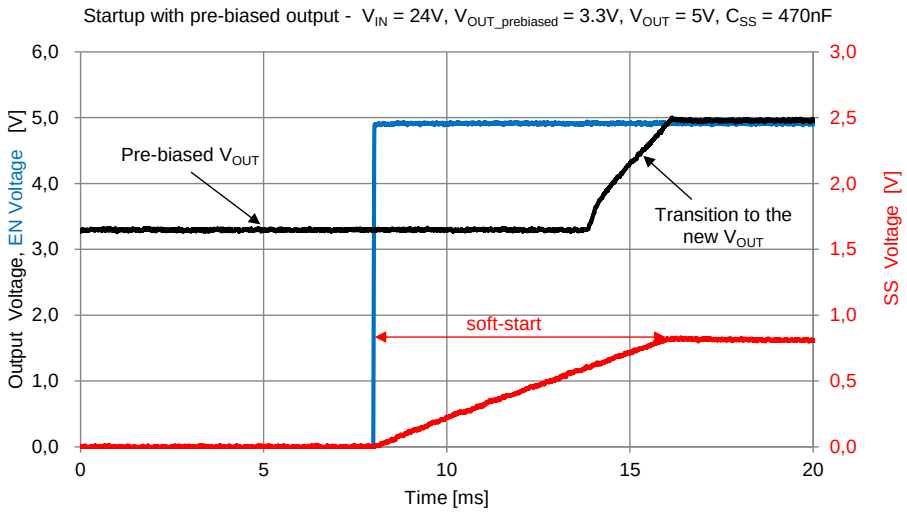
Zero coil current detection (ZCCT)

The current of the low-side MOSFET is monitored by a zero coil current detection circuit that inhibits the low-side MOSFET when its current reaches zero until the next on-time. This circuit prevents a negative inductor current and enables the DCM operating mode (see “Light load operation” on page 31). In this way the efficiency at light loads is improved, also because the output capacitor is not discharged by the negative current.

Start up into pre-biased load

The MagI³C power module will properly start up into a pre-biased output (see example in the figure below). This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high side MOSFET body diode.
The figure below shows an example of start up with a pre-biased output voltage (3.3V, black curve). When the EN pin voltage goes up (blue curve), the soft-start takes place (red curve) and the output voltage moves from 3.3V to the final value of 5V.



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DETERMINE POWER LOSSES AND THERMAL REQUIREMENTS OF THE BOARD

This section provides an example of calculation of power losses and thermal design of the board.
As a starting point the following application conditions can be considered:

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 5A, $T_{A(MAX)}$ = 60°C and $T_{J(MAX)}$ = 125°C

where T_A is the maximum air temperature surrounding the module and $T_{J(MAX)}$ is the maximum value of the junction temperature according to the limits in the "OPERATING CONDITIONS" section on page 4.
The goal of the calculation is to determine the characteristics of the required heat sink. In the case of a surface mounted module this would be the PCB (number of layers, copper area and thickness). These characteristics are reflected in the value of the case to ambient thermal resistance (θ_{JA}).
The basic formula for calculating the operating junction temperature T_J of a semiconductor device is as follows:

$$T_J = P_{LOSS} \cdot \theta_{JA} + T_A \quad (20)$$

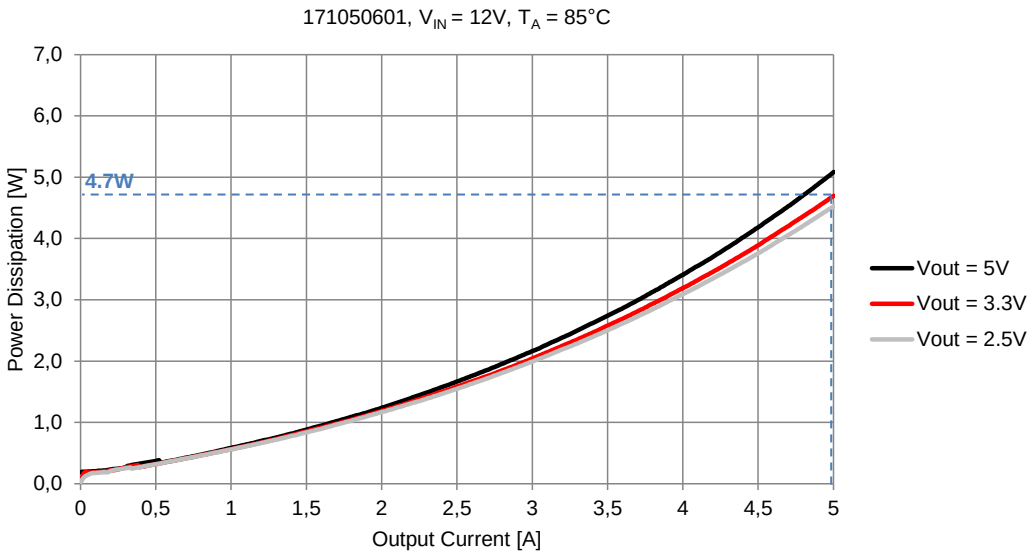
P_{LOSS} is the total power loss within the module and is related to the operating conditions (e.g. V_{IN}, V_{OUT}, I_{OUT}, f_{SW}).
Θ_{JA} is the junction to ambient thermal resistance and calculated as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (21)$$

Θ_{JC} is the junction to case thermal resistance.
Combining equations (20) and (21) results in the maximum case-to-ambient thermal resistance:

$$\theta_{CA(MAX)} < \frac{T_{J(MAX)} - T_{A(MAX)}}{P_{LOSS}} - \theta_{JC} \quad (22)$$

From section "THERMAL SPECIFICATIONS" (page 4) the typical thermal resistance from junction to case (θ_{JC}) is defined as 1.9 °C/W. Using the 85°C (60°C not available, however 85°C is the worst case condition) power dissipation curves in the "TYPICAL PERFORMANCE CURVES" section (page 12) the power losses P_{LOSS} can be estimated.



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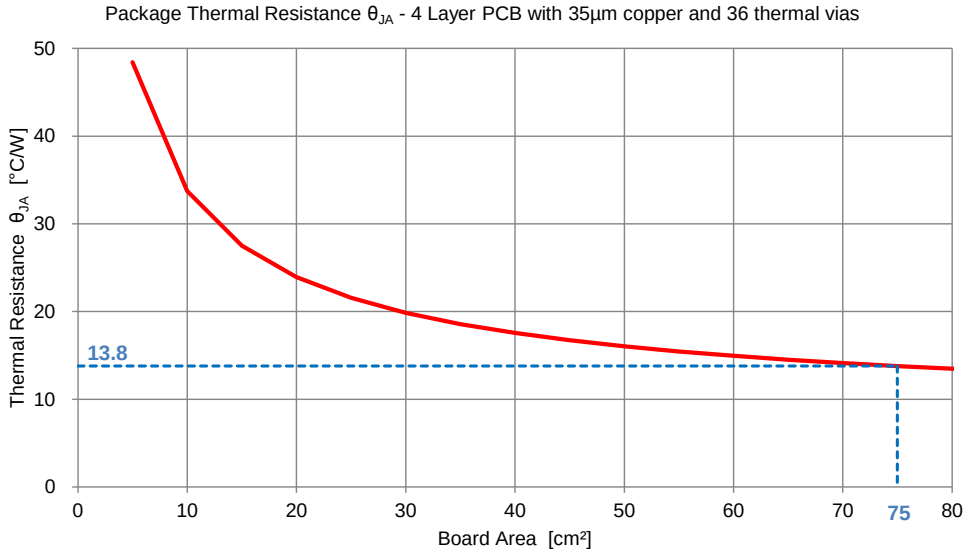
From the graph a loss of 4.7W is read. Entering the values in formula (22) results in:

$$\theta_{CA(MAX)} < \frac{125°C\text{-}60°C}{4.7W} - 1.9°C/W = 11.9°C/W$$

$$\theta_{JA(MAX)} = \theta_{JC} + \theta_{CA(MAX)} = 1.9°C/W + 11.9°C/W = 13.8°C/W$$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area the following package thermal resistance graph can be considered.



For θ_{JA} < 13.8°C/W and only natural convection (LFM=0, where LFM stands for Linear Feet per Minute, i.e. no air flow), the minimum PCB area should be 75cm². This corresponds to a square board with about 8.7cm x 8.7cm copper area, 4 layers, and 35µm copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

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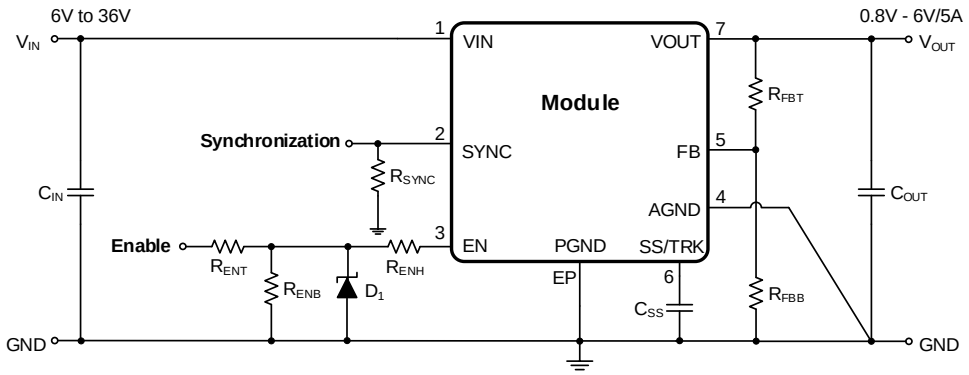
VDRM – Variable Step Down Regulator Module

TYPICAL SCHEMATIC



Quick setup guide

Conditions: I_{OUT} = 5A

Recommended component values

V_{OUT}	6V	5V	3.3V	2.5V	1.8V	1.2V
R_{FBT}	10kΩ	10kΩ	10kΩ	10kΩ	10kΩ	10kΩ
R_{FBB}	1.54kΩ	1.91kΩ	3.16kΩ	4.64kΩ	7.87kΩ	19.6kΩ
R_{SYNC}	1.5kΩ	61.9kΩ	47.5kΩ	32.4kΩ	28.0kΩ	22.6kΩ
R_{ENT}	12.7kΩ (V_{UVLO} = 5.46V)					
R_{ENB}	42.2 kΩ (V_{UVLO} = 5.46V)					
R_{ENH}	To be calculated for additional hysteresis					
D1	Zener Diode 5.1V					
C_{IN}	3x10µF					
C_{OUT}	220µF					
C_{SS}	470nF					
V_{IN}	9-36V	7.5-36V	6-36V			

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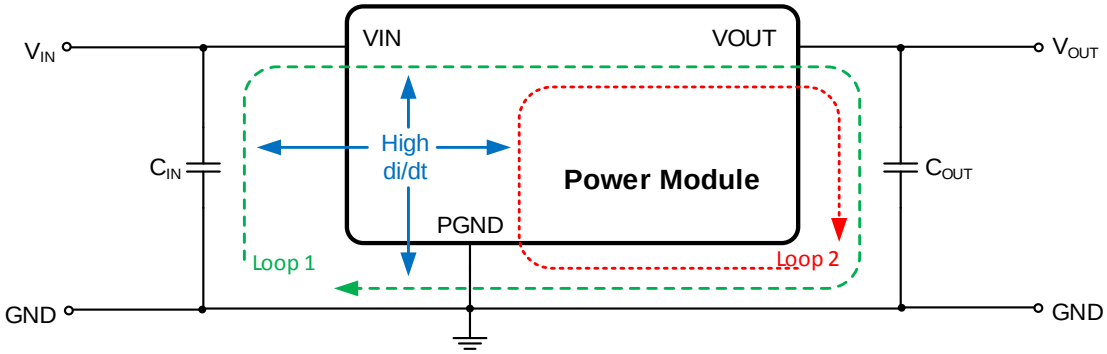
VDRM – Variable Step Down Regulator Module

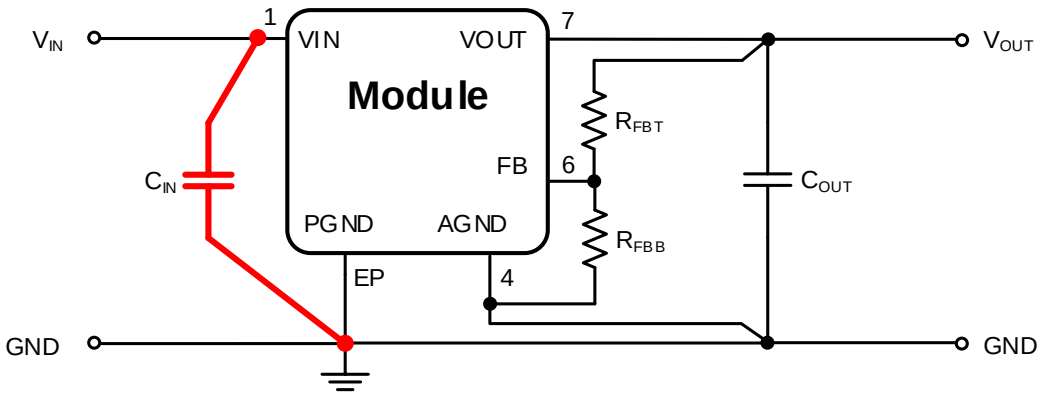
LAYOUT RECOMMENDATION

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. A good layout can be implemented by following simple design rules.

1: Minimize the area of switched current loops.



The target is to identify the paths in the system that have discontinuous current flow. They are the most critical ones because they act as an antenna and cause observable high frequency noise (EMI). The easiest approach to find the critical paths is to draw the high current loops during both switching cycles and identify the sections which do not overlap. They are the ones where no continuous current flows and high di/dt is observed. Loop1 is the current path during the ON-time of the high-side MOSFET. Loop2 is the current path during the OFF-time of the high-side MOSFET.



Based on those considerations, the path of the input capacitor C_{IN} is the most critical one to generate high frequency noise on V_{IN}. Therefore, place C_{IN} as close as possible to the MagI³C power module V_{IN} and PGND exposed pad EP. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad.

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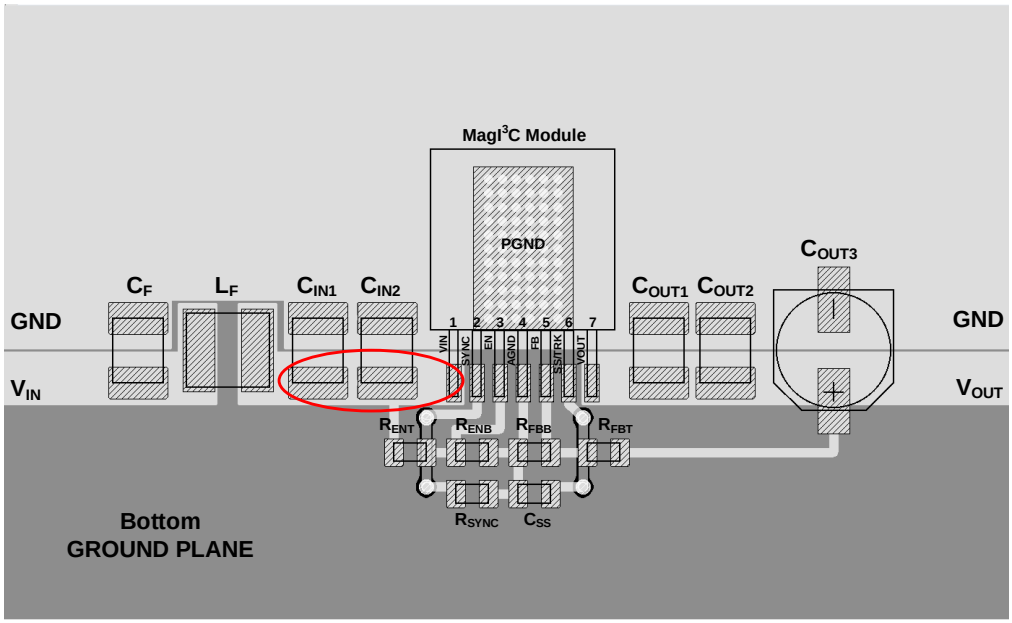
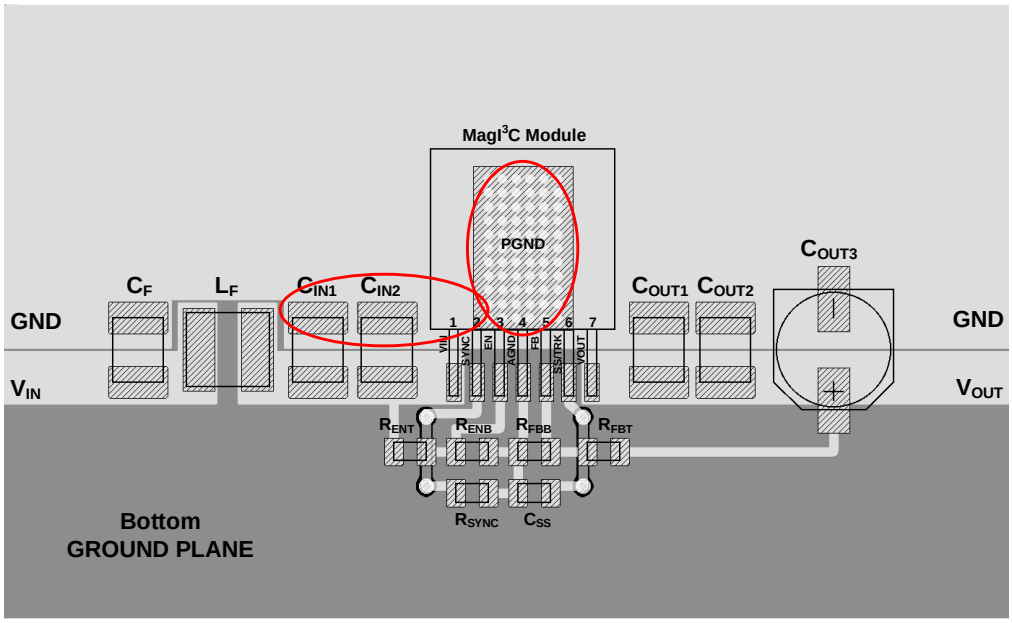
VDRM – Variable Step Down Regulator Module

The placement of the input capacitors is highlighted in the following picture.



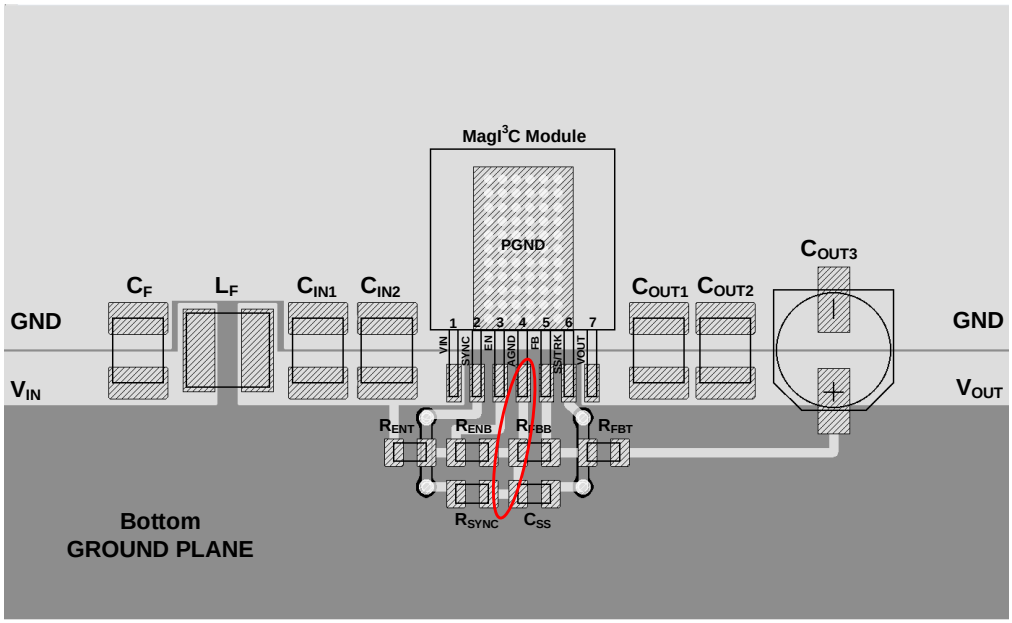
PCB color coding: Top layer Bottom layer

The positive terminal of C_{IN1} and C_{IN2} need to be very close to the VIN pin of the power module.



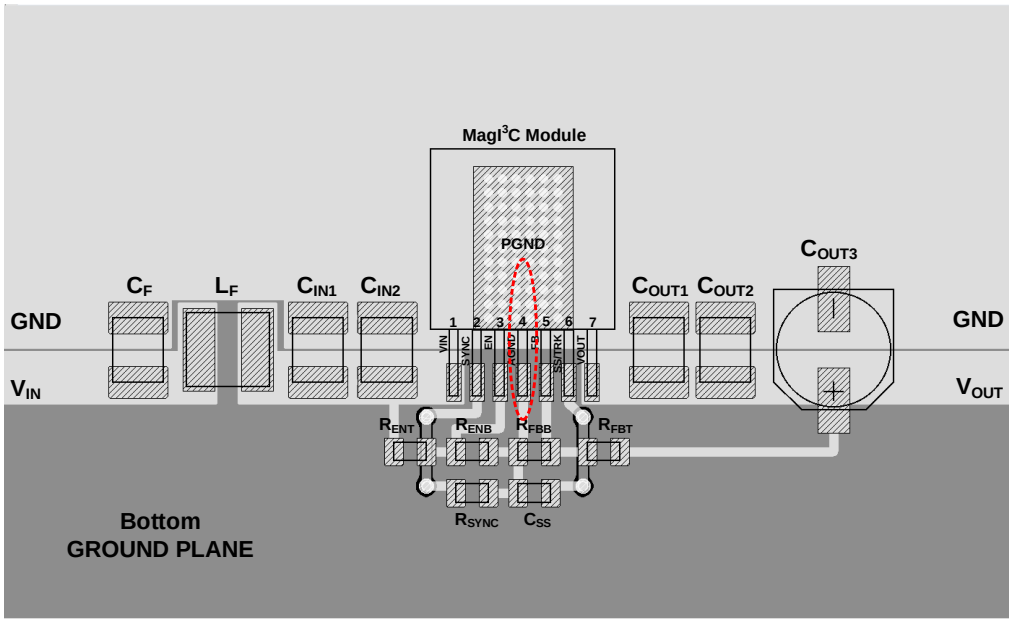
The ground connection of C_{IN1} and C_{IN2} needs to be very close to the PGND pad of the power module.

2: Analog Ground (AGND) connections



The ground connections for the soft-start capacitor (C_{SS}), the output voltage lower resistor divider (R_{FBB}), the enable components (when used) and R_{SYNC} should be routed to the AGND pin of the device. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Place C_{SS}, R_{FBT} and R_{FBB} close to their respective pins.

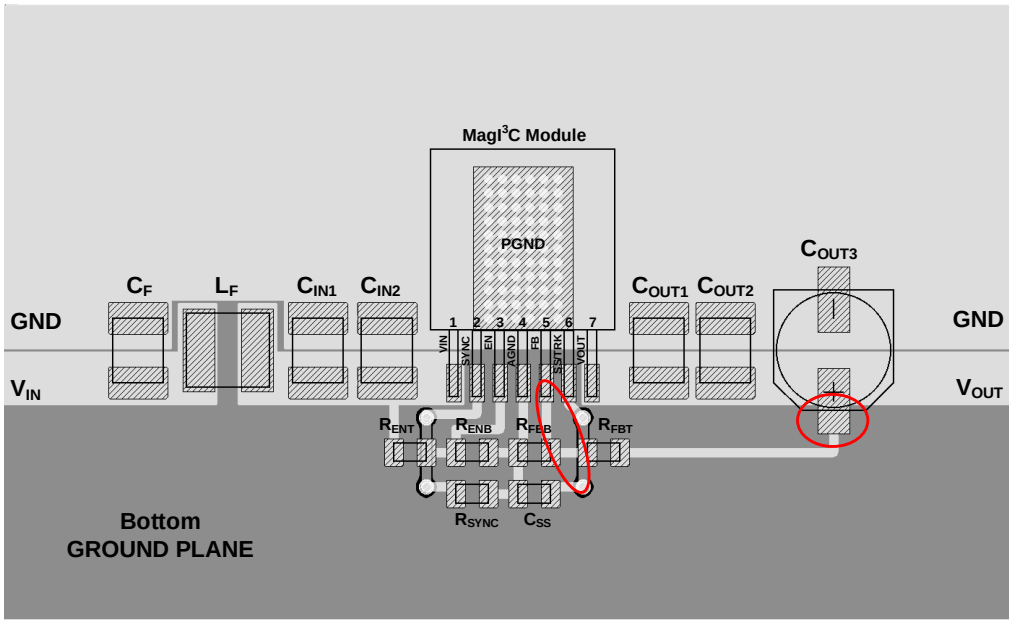
3: Analog Ground (AGND) to Power Ground (PGND) connections



Module internal connection:

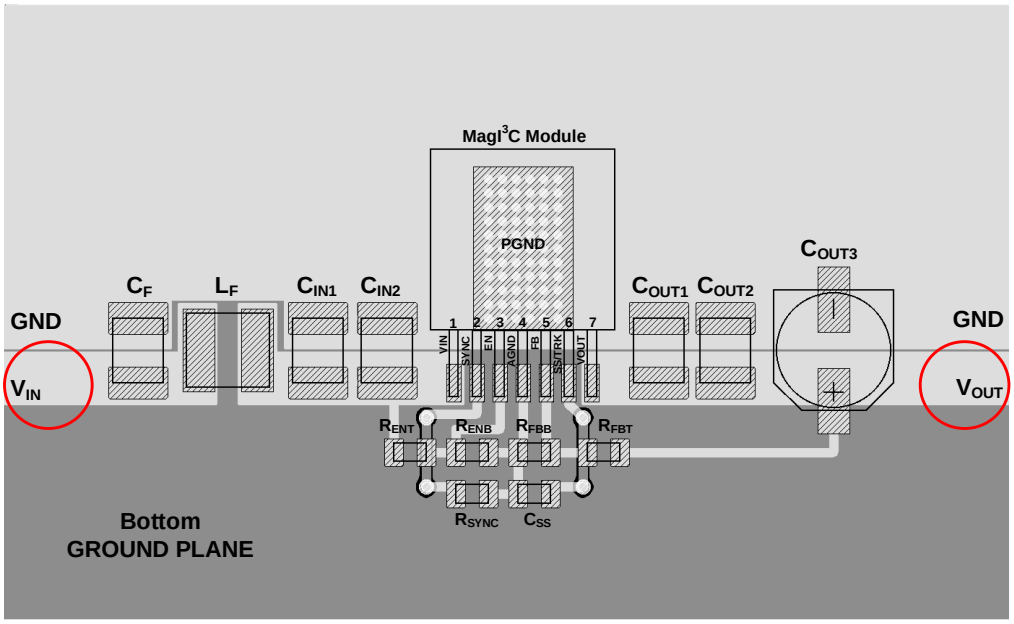
The AGND is **internally connected** to PGND at a low noise node. The output current is flowing from the PGND pad through the ground plane through the ground terminal of the first output capacitor. Due to its very low ripple it will not inject noise in the ground plane.

4: Feedback layout



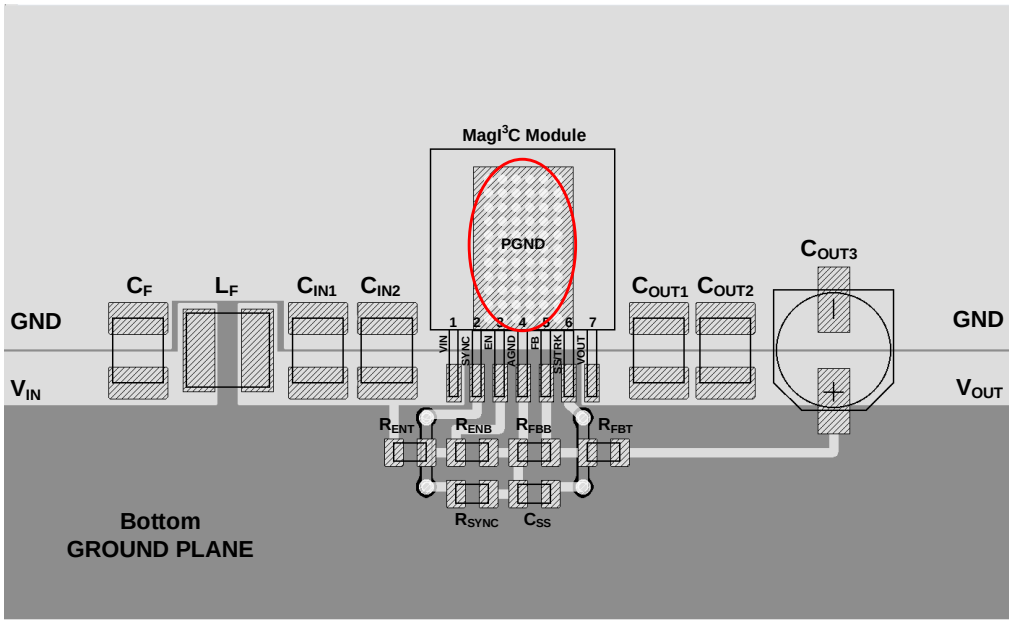
The resistor divider (R_{FBT} and R_{FBB}) should be located close to the FB pin. Since the FB node is high impedance, the trace thickness should be kept small. The traces from the FB pin to the middle point of the resistor divider should be as short as possible. The upper terminal of the output resistor divider (where the V_{OUT} is normally applied) should be connected to the output connection of the last output capacitor (C_{OUT3}), because this is the node with the lowest noise. The traces from R_{FBT} and R_{FBB} should be routed away from the body of the MagI³C Power Module to minimize noise pickup.

5: Make input and output bus connections as wide as possible

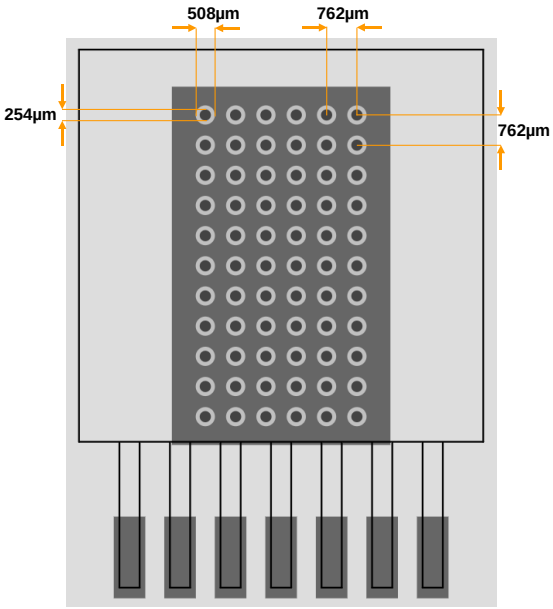


This reduces any voltage drops on the input or output of the converter and maximizes efficiency.

6: Provide adequate device heat-sinking



Place a dedicated PGND copper area beneath the MagI³C Power Module.
Use an array of heat-sinking vias to connect the PGND pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be used to make a connection to the heat-spreading ground planes located on inner layers.



For best result, use a thermal via array as proposed in the picture above with drill of 254µm, spaced 762µm apart. Ensure enough copper area is used for heat-sinking, to keep the junction temperature below 125°C.

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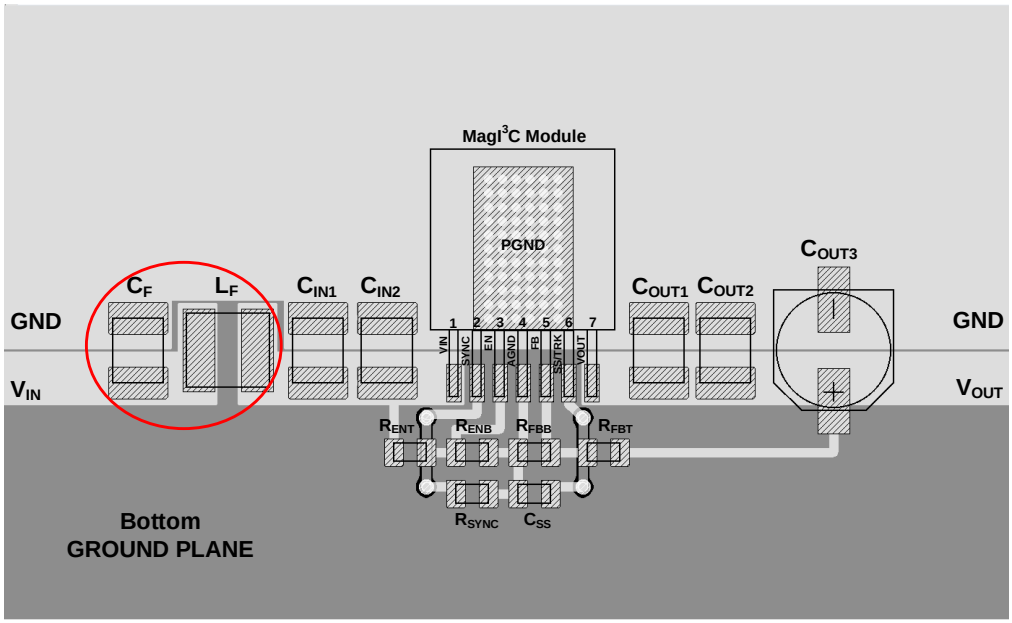
MagI³C Power Module

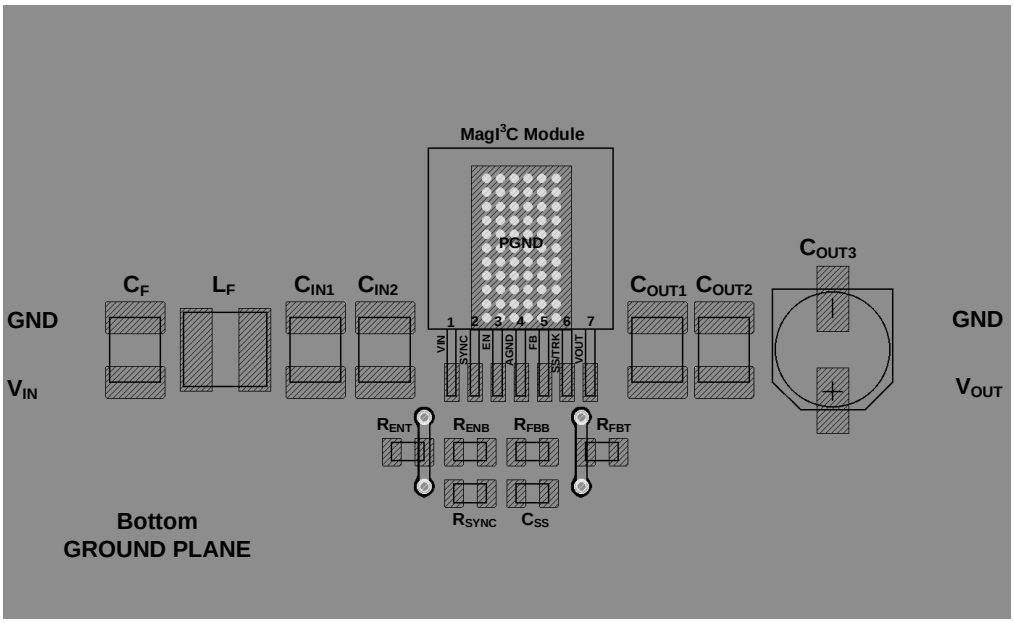
VDRM – Variable Step Down Regulator Module

7: Input filter section



The filter network, if used, should be placed as close as possible to the input of the power module to avoid undesired radiation over long traces. Short connections from the power supply lines to the filter capacitor are also recommended to reduce the additional series inductance.

8: Isolate high noise areas



Place a dedicated solid GND copper area beneath the MagI³C Power Module. The recommended copper thickness is at least 70µm.

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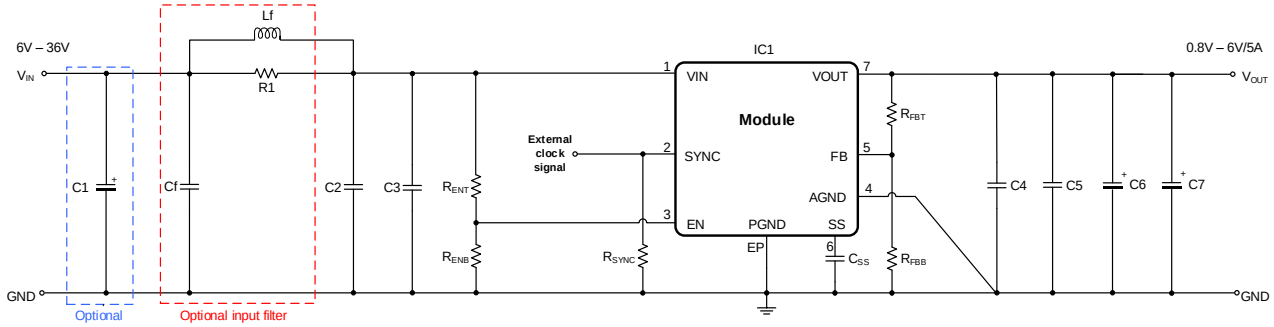
VDRM – Variable Step Down Regulator Module

EVALUATION BOARD SCHEMATIC (178050601 v3.1)

The evaluation board schematic has been developed to be suitable for all input and output voltage conditions supported by the module, switching frequencies and load currents as well as to achieve optimum load transient response.



The two multi-layer ceramic capacitors (MLCCs) C2 and C3 at the input handle the switching current ripple and support fast load transients preventing the voltage at the VIN pin from dropping, potentially below the UVLO threshold. Two MLCCs in parallel help to reduce the ESR. The additional aluminum electrolytic capacitor C1 is only for the purpose of protecting the evaluation board. It is mounted as a termination of the supply line and provides a slight damping of possible oscillations of the series resonance circuit represented by the inductance of the supply line and the input capacitance.
The additional MLCC C_f is part of the input filter and is mounted on the board. The inductor L_f is not mounted and replaced by a zero ohm resistor R1 on the evaluation board. In the event an input filter is to be placed on the board, R1 must be removed and an appropriate L_f mounted.
The output capacitors should provide a low ESR, in order to reduce the output voltage ripple. The requirement of high output capacitance for good transient response performance is fulfilled by mounting an additional aluminum polymer capacitor C6 (220µF, 875115350002) in parallel to the MLCC output capacitors (22µF, 885012108018). The use of two MLCCs in parallel leads to a very low total ESR. Furthermore, the use of more MLCCs in parallel at the input and at the output increases the reliability of the system (in case one capacitor fails, there is still another one remaining). An aluminum electrolytic through-hole capacitor can be placed at the output as well (C7, not mounted) as an alternative to C6.
R_{SYNC} is a pull-down resistor that connects the SYNC pin to ground if no synchronization signal is applied. This pull-down resistor ensures that the device is enabled (see page 30).

Operational Requirements

At high duty cycles (V_{IN} very close to V_{OUT}) the input current will be very similar to the output current. Make sure that your supply for the module is capable of delivering high enough currents (check the current limit setting of your power supply). In case your module output voltage V_{OUT} is set to very low values (for example 0.8V) electronic loads might not be able to work correctly. Use discrete high power resistors instead as a load. Use thick and short leads to the input of the module and to the load. High currents result in additional voltage drops across the cables, which decrease the voltage at the load. Measure the input and output voltage directly at the ceramic capacitors at the input and output (test points).

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Bill of Material

Designator	Description		Quantity	Order Code	Manufacturer
IC1	MagI³C Power Module		1	171050601	Würth Elektronik
C1	Aluminum electrolytic capacitor 100µF/50V, ATG8 family		1	860010674014	Würth Elektronik
C2,C3	Ceramic chip capacitor 10µF/50V X5R, 1210		2		
C4,C5	Ceramic chip capacitor 22µF/16V X5R, 1206, CSGP family		2	885012108018	Würth Elektronik
C6	Aluminum polymer capacitor 220µF/10V, PSHP family		1	875115350002	Würth Elektronik
C7	Aluminum electrolytic capacitor (not mounted)				
C_f	Aluminum polymer capacitor 10µF/63V (not mouned)			875115852001	Würth Elektronik
C_{SS}	Ceramic chip capacitor, 0805 (not mounted)				
L_f	Not mounted, see recommended value in the "Filter suggestion for conducted EMI" section on the next page				
R_{ENT}, R_{ENB}	Not mounted				
R_{SYNC}	Chip resistor 1.5kΩ, 1%, 0805		1		
R1	SMD bridge 0Ω resistance (remove when L_f is mounted)		1		
R_{FBT}	10kΩ		1		
R_{FBB}	Set by jumper	1.54 kΩ for V_{OUT} = 6V	1		
		1.91 kΩ for V_{OUT} = 5V	1		
		3.16 kΩ for V_{OUT} = 3.3V	1		
		4.64 kΩ for V_{OUT} = 2.5V	1		
		7.87 kΩ for V_{OUT} = 1.8V	1		
		19.6 kΩ for V_{OUT} = 1.2V	1		
		For adjustable V_{OUT}: $R_{FBB}=\frac{R_{FBT}\cdot 0.8V}{V_{OUT}-0.8V}$ (see DESIGN FLOW – Step1 on page 18)			

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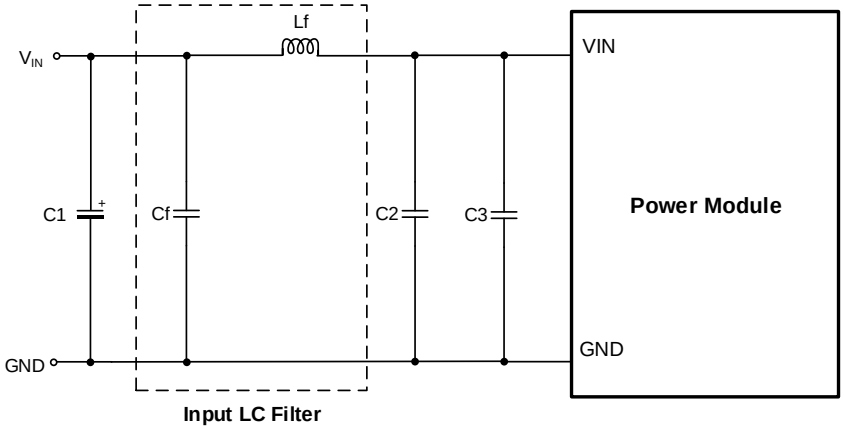
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

Filter suggestion for conducted EMI

The input filter shown in the schematic below is recommended to achieve conducted compliance according to EN55032 CISPR32 Class B (see results on page 8).
For radiated EMI the input filter is not necessary. It is only used to comply with the setup recommended in the norms.



Input LC Filter

Bill of Material of the Input LC Filter (V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 5A)

Designator	Description	Order Code	Manufacturer
C_f	Filter aluminum polymer capacitor 10µF/63V, ESR = 45mΩ	875115852001	Würth Elektronik
Lf	Filter inductor, 2.2µH, PD2 family, I_{SAT} = 3.38A , I_R = 2.5A	744773022	Würth Elektronik

Bill of Material of the Input LC Filter (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A)

Designator	Description	Order Code	Manufacturer
C_f	Filter aluminum polymer capacitor 10µF/63V, ESR = 45mΩ	875115852001	Würth Elektronik
Lf	Filter inductor, 2.2µH, PD2 family, I_{SAT} = 8.2A , I_R = 4.6A	744774022	Würth Elektronik

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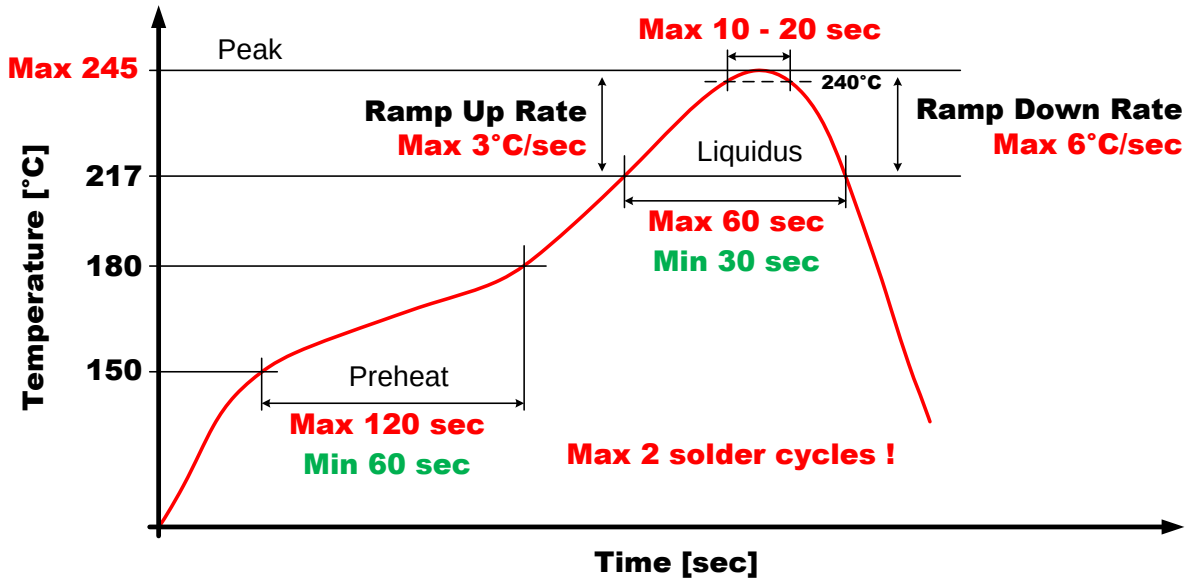
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

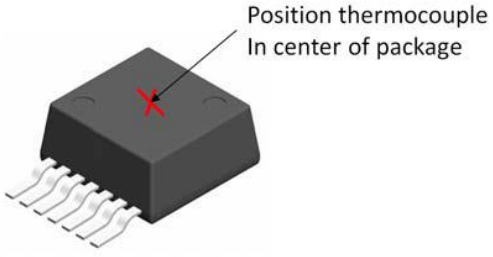
HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033).
2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
3. When opening the moisture barrier bag check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card .
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033 recommendation.

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C power module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 240°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 240°C ±5°C must not exceed 20 seconds.
5. Reflow time above liquidus (217°C) must not exceed 60 seconds.
6. Maximum ramp up is rate 3°C per second
7. Maximum ramp down rate is 6°C per second
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is two**.
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. Consider that the lead material is copper (Cu) and lead finish is tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk





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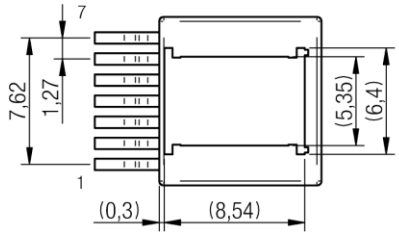
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

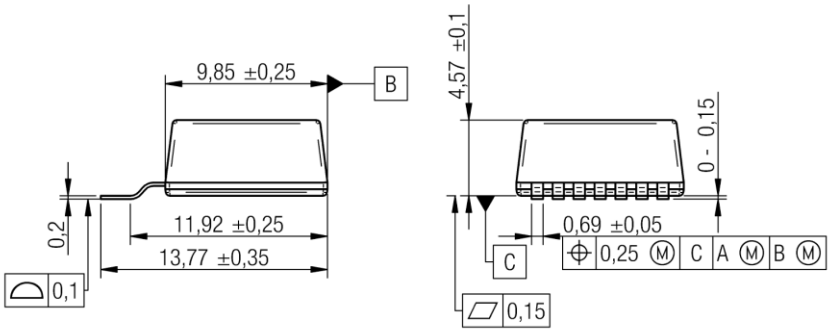
PHYSICAL DIMENSIONS

Package type: TO263-7

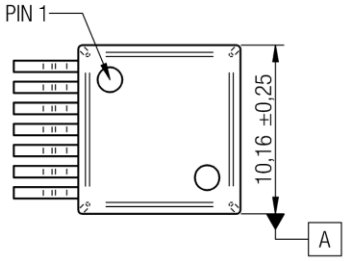
Bottom view

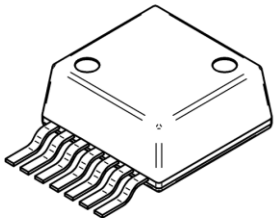


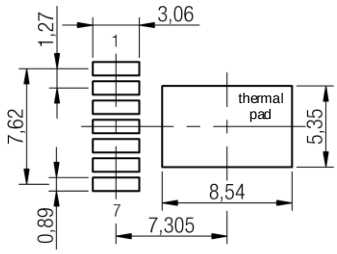
Side view



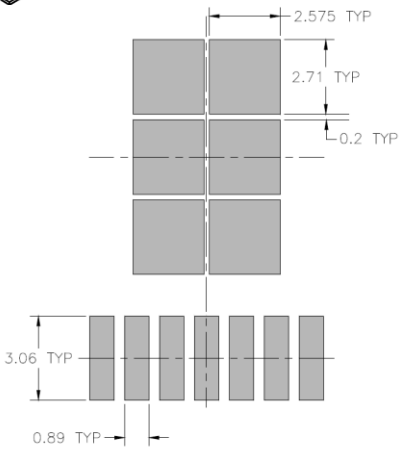
Top view







Recommended soldering pad



recommended stencil design

All dimensions in mm

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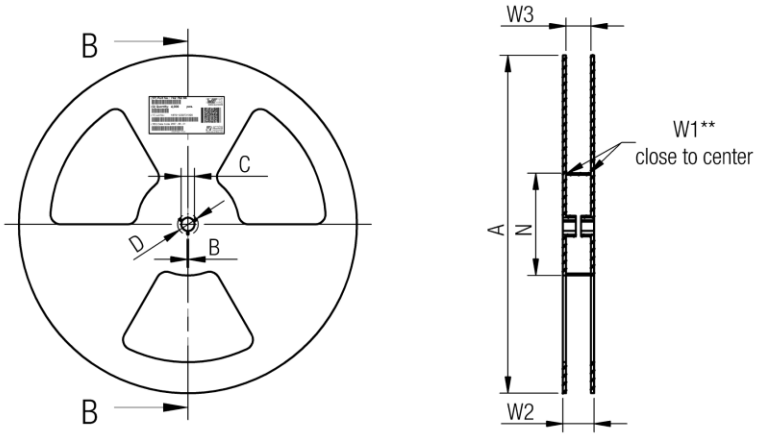
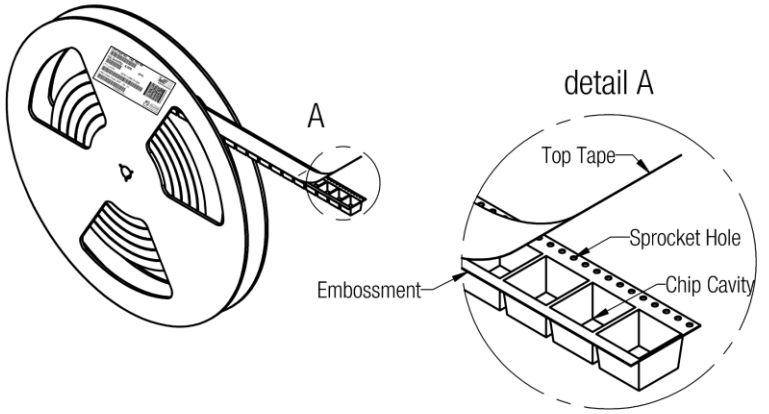
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

PACKAGING
Reel (mm)



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	± 2,0	+ 2	max.	min.	max.
Tape width	**24mm**	330,00	1,50	13,00	20,20	60,00	24,40	30,40	23,90	27,40



20P

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MagI³C Power Module
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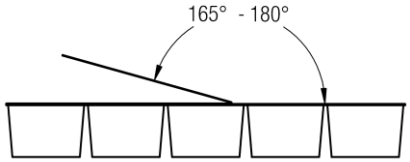
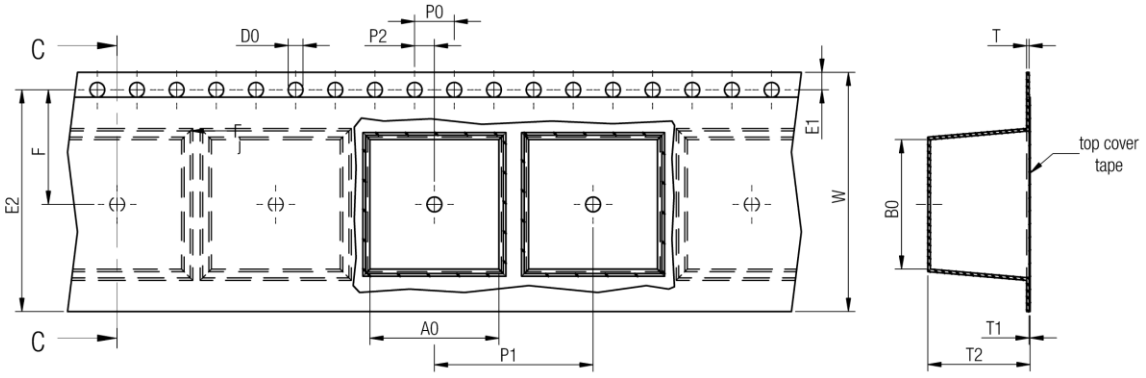
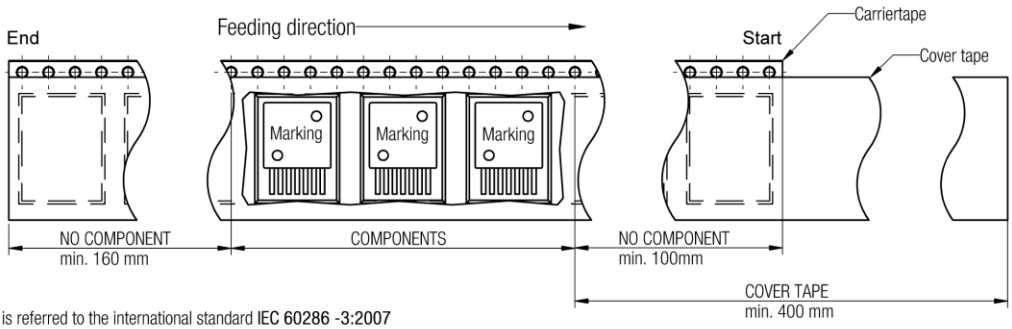
Tape (mm)



		Pull-of force
Tape width	**24 mm**	0,1 N - 1,3 N



		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,3 -0,1	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	**TO263-7EP**	10,60	14,22	24,00	16,00	0,50	0,10	5,00	1,50	1,75	22,25	11,50	4,00	2,00	Polystyrene	250



Packaging is referred to the international standard IEC 60286 -3:2007

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MagI³C Power Module

VDRM – Variable Step Down Regulator Module

DOCUMENT HISTORY

Revision	Date	Description	Comment
1.0	10.03.2015	Release of the final version	
2.0	July 2018	Updated version released	- No changes to the component have been applied. No changes to existing designs using the module are therefore required. - Additional information included

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the datasheet have to be complied with.

The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:
- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

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