

## General Description

The MC14094 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of MC14094 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading MC14094 devices when the clock has a slow rise time.

It operates over a recommended  $V_{DD}$  power supply range of 3V to 15V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

## Features

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5 V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from - 40° C to + 85° C
- Packaging information: SOP16

## Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
MC14094BDR2G	SOP-16	14094	Tape	2500Pcs/Reel

Block Diagram And Pin Description

Block Diagram

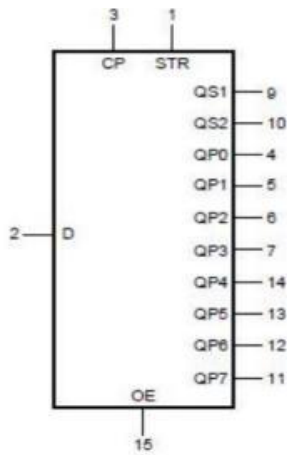


Figure 1. Logic symbol

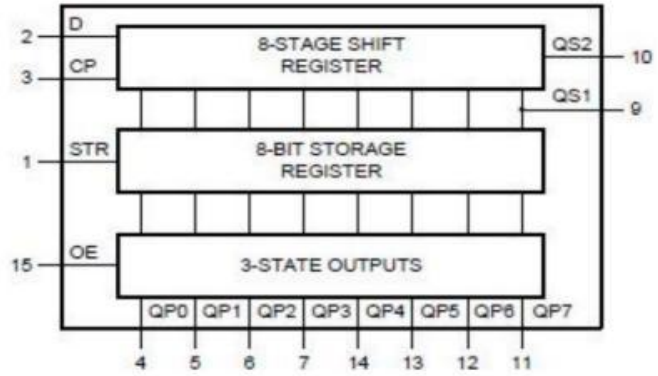


Figure 2. Functional diagram

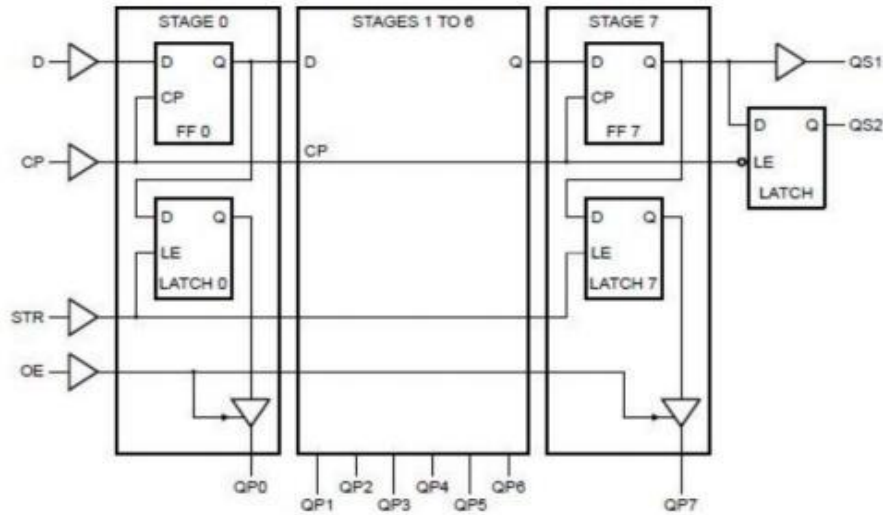


Figure 3. Logic diagram

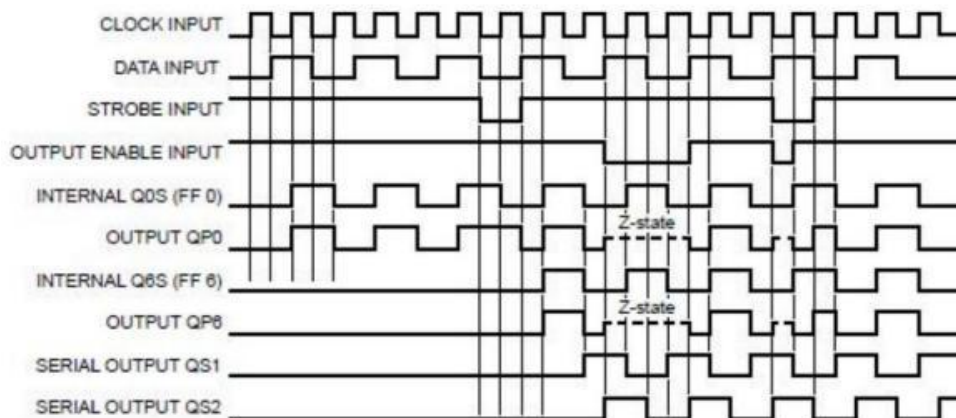
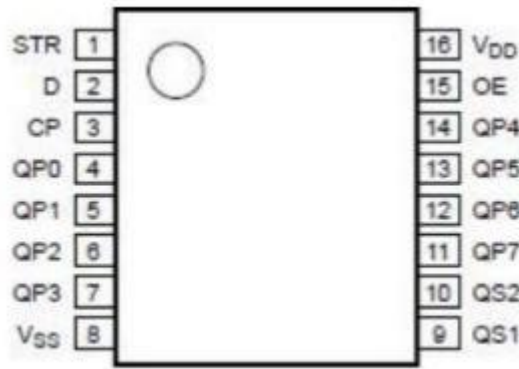


Figure 4. Timing diagram

**Pin Configurations**



**Pin Description**

Pin No.	Pin Name	Description
1	STR	strobe input
2	D	data input
3	CP	clock input
4	QP0	parallel output
5	QP1	parallel output
6	QP2	parallel output
7	QP3	parallel output
8	V <sub>SS</sub>	ground supply voltage
9	QS1	serial output
10	QS2	serial output
11	QS7	parallel output
12	QS6	parallel output
13	QS5	parallel output
14	QS4	parallel output
15	OE	output enable input
16	V <sub>DD</sub>	supply voltage

**Function Table**

Input				Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn-1	Q6S	NC
↑	H	H	H	H	QPn-1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=HIGH-impedance OFF-state; NC=no change; ↑=positive-going transition; ↓=negative-going transition;

Q6S=the data in register stage 6 before the LOW to HIGH clock transition; Q7S=the data in register stage 7 before the HIGH to LOW clock transition.

## Electrical Parameter

**Absolute Maximum Ratings** ( $T_{amb}=25^{\circ}\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Conditions		Min.	Max.	Unit
supply voltage	$V_{DD}$	-		-0.5	+18	V
DC input current	$I_{IK}$	any one input		-10	-	mA
input voltage	$V_I$	all inputs		-0.5	+18	V
storage temperature	$T_{stg}$	-		-65	+150	$^{\circ}\text{C}$
total power dissipation	$P_{tot}$	-		-	500	mW
device dissipation	P	Per output transistor		-	100	mW
soldering temperature	$T_L$	10s	DIP	245		$^{\circ}\text{C}$
			SOP/TSSOP	260		$^{\circ}\text{C}$

Note:

- [ 1 ] For DIP16 packages: above  $70^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 12mW/K.
- [ 2 ] For SOP16 packages: above  $70^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 8mW/K.
- [ 3 ] For (T)SSOP16 packages: above  $60^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 5.5mW/K.

### Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	$V_{DD}$	-	3	-	15	V
ambient temperature	$T_{amb}$	-	-40	-	+85	$^{\circ}\text{C}$
data setup time	$t_{SU}$	$V_{DD}=5\text{V}$	125	-	-	ns
		$V_{DD}=10\text{V}$	55	-	-	ns
		$V_{DD}=15\text{V}$	35	-	-	ns
clock pulse width	$t_w$	$V_{DD}=5\text{V}$	200	-	-	ns
		$V_{DD}=10\text{V}$	100	-	-	ns
		$V_{DD}=15\text{V}$	83	-	-	ns
clock input frequency	$f_{max}$	$V_{DD}=5\text{V}$	dc	-	1.25	MHz
		$V_{DD}=10\text{V}$		-	2.5	MHz
		$V_{DD}=15\text{V}$		-	3	MHz
clock rise and fall time	$t_{rCL}, t_{fCL}$	$V_{DD}=5\text{V}$	-	-	15	$\mu\text{s}$
		$V_{DD}=10\text{V}$	-	-	5	$\mu\text{s}$
		$V_{DD}=15\text{V}$	-	-	5	$\mu\text{s}$
strobe setup time	$t_w$	$V_{DD}=5\text{V}$	200	-	-	$\mu\text{s}$
		$V_{DD}=10\text{V}$	80	-	-	$\mu\text{s}$
		$V_{DD}=15\text{V}$	70	-	-	$\mu\text{s}$

## Electrical Characteristics

DC Characteristics 1 (T<sub>amb</sub>=25 °C, voltages are referenced to V<sub>SS</sub> (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions(V)			T <sub>amb</sub> =25°C			Unit
		V <sub>O</sub>	V <sub>IN</sub>	V <sub>DD</sub>	Min.	Typ.	Max.	
supply current	I <sub>DD</sub>	-	0, 5	5	-	0.04	5	μA
		-	0, 10	10	-	0.04	10	μA
		-	0, 15	15	-	0.04	20	μA
LOW-level output current	I <sub>OL</sub>	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I <sub>OH</sub>	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V <sub>OL</sub>	-	0, 5	5	-	-	0.05	V
		-	0, 10	10	-	-	0.05	V
		-	0, 15	15	-	-	0.05	V
HIGH-level output voltage	V <sub>OH</sub>	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V <sub>IL</sub>	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V <sub>IH</sub>	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I <sub>I</sub>	-	0, 15	15	-	±10 <sup>-5</sup>	±0.1	μA
OFF-state output current	I <sub>OZ</sub>	0, 15	0, 15	15	-	±10 <sup>-4</sup>	±0.4	μA

**DC Characteristics 2**

 (T<sub>amb</sub>=-40°C to +85°C, voltages are referenced to V<sub>SS</sub> (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions(V)			T <sub>amb</sub> =-40°C		T <sub>amb</sub> =+85°C		Unit
		V <sub>O</sub>	V <sub>IN</sub>	V <sub>DD</sub>	Min.	Max.	Min.	Max.	
supply current	I <sub>DD</sub>	-	0, 5	5	-	5	-	150	μA
		-	0, 10	10	-	10	-	300	μA
		-	0, 15	15	-	20	-	600	μA
LOW-level output current	I <sub>OL</sub>	0.4	0, 5	5	0.61	-	0.42	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	mA
		1.5	0, 15	15	4	-	2.8	-	mA
HIGH-level output current	I <sub>OH</sub>	4.6	0, 5	5	-0.61	-	-0.42	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	mA
LOW-level output voltage	V <sub>OL</sub>	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V <sub>OH</sub>	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V <sub>IL</sub>	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	V <sub>IH</sub>	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I <sub>I</sub>	-	0, 15	15	-	±0.1	-	±1	μA
OFF-state output current	I <sub>OZ</sub>	0, 15	0, 15	15	-	±0.4	-	±12	μA

**AC Characteristics** ( $T_{amb}=25^{\circ}\text{C}$ ,  $V_{SS}=0\text{V}$ ,  $t_r, t_f=20\text{ns}$ ,  $C_L=50\text{pF}$ ,  $R_L=200\text{K}\Omega$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay time	t <sub>PHL</sub> , t <sub>PLH</sub>	CP to QS1; see Figure 6	V <sub>DD</sub> =5V	-	300	600	ns
			V <sub>DD</sub> =10V	-	125	250	ns
			V <sub>DD</sub> =15V	-	95	190	ns
		CP to QS2; see Figure 6	V <sub>DD</sub> =5V	-	230	460	ns
			V <sub>DD</sub> =10V	-	110	220	ns
			V <sub>DD</sub> =15V	-	75	150	ns
		CP to QPn; see Figure 6	V <sub>DD</sub> =5V	-	420	840	ns
			V <sub>DD</sub> =10V	-	195	390	ns
			V <sub>DD</sub> =15V	-	135	270	ns
		STR to QPn; see Figure 7	V <sub>DD</sub> =5V	-	290	580	ns
			V <sub>DD</sub> =10V	-	145	290	ns
			V <sub>DD</sub> =15V	-	100	200	ns
HIGH to OFF-state/OFF-state to HIGH propagation delay	t <sub>PHZ</sub> , t <sub>PZH</sub>	OE to QPn; see Figure 8	V <sub>DD</sub> =5V	-	140	280	ns
			V <sub>DD</sub> =10V	-	60	120	ns
			V <sub>DD</sub> =15V	-	45	90	ns
LOW to OFF-state/OFF-state to LOW propagation delay	t <sub>PLZ</sub> , t <sub>PZL</sub>	OE to QPn; see Figure 8	V <sub>DD</sub> =5V	-	100	200	ns
			V <sub>DD</sub> =10V	-	50	100	ns
			V <sub>DD</sub> =15V	-	40	80	ns
pulse width	t <sub>w</sub>	minimum HIGH strobe pulse; see Figure 7	V <sub>DD</sub> =5V	-	100	200	ns
			V <sub>DD</sub> =10V	-	40	80	ns
			V <sub>DD</sub> =15V	-	35	70	ns
		minimum LOW clock pulse; see Figure 6	V <sub>DD</sub> =5V	-	100	200	ns
			V <sub>DD</sub> =10V	-	50	100	ns
			V <sub>DD</sub> =15V	-	40	83	ns
data setup time	t <sub>SU</sub>	D to CP; see Figure 9	V <sub>DD</sub> =5V	-	60	125	ns
			V <sub>DD</sub> =10V	-	30	55	ns
			V <sub>DD</sub> =15V	-	20	35	ns
transition time	t <sub>t</sub>	-	V <sub>DD</sub> =5V	-	100	200	ns
			V <sub>DD</sub> =10V	-	50	100	ns
			V <sub>DD</sub> =15V	-	40	80	ns
clock input rise and fall time	t <sub>rCL</sub> , t <sub>fCL</sub>	-	V <sub>DD</sub> =5V	15	-	-	us
			V <sub>DD</sub> =10V	5	-	-	us
			V <sub>DD</sub> =15V	5	-	-	us
Maximum clock frequency	f <sub>max</sub>	see Figure 6	V <sub>DD</sub> =5V	1.25	2.5	-	MHz
			V <sub>DD</sub> =10V	2.5	5	-	MHz
			V <sub>DD</sub> =15V	3	6	-	MHz
input	C <sub>I</sub>	any input		5	7.5	pF	

 Note: t<sub>t</sub> is the same as t<sub>TLH</sub> and t<sub>THL</sub>.

## Testing Circuit

### AC Testing Circuit

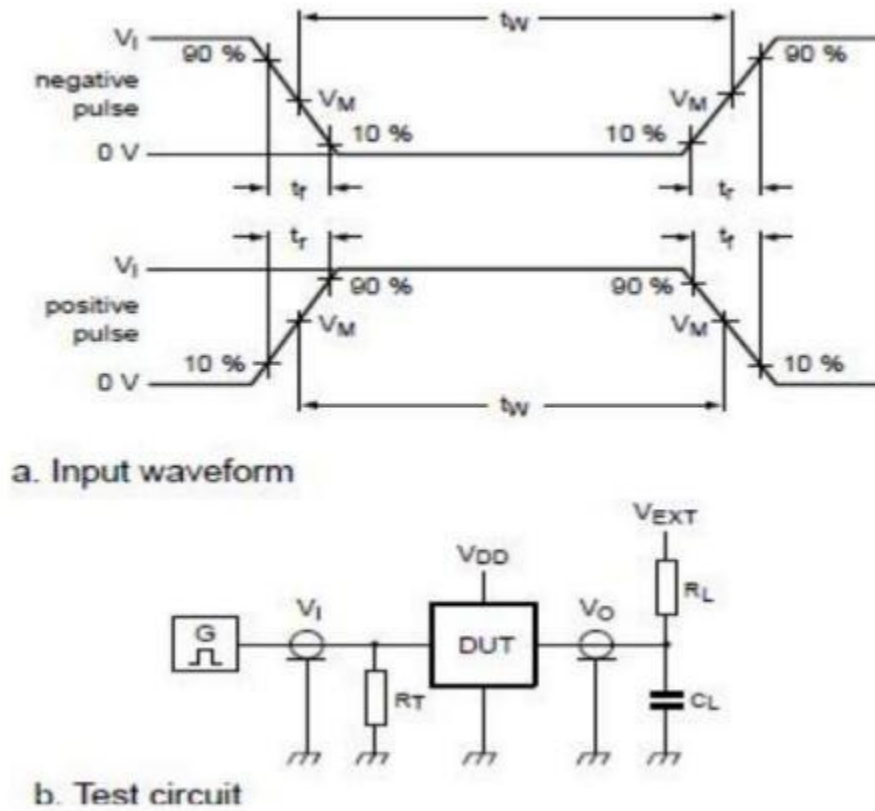


Figure 5. Test circuit for switching times

Definitions for test

circuit: DUT=Device

Under Test

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.  $R_L$ =Load resistance

$V_{EXT}$ =External voltage for measuring switching times

### AC Testing Waveforms



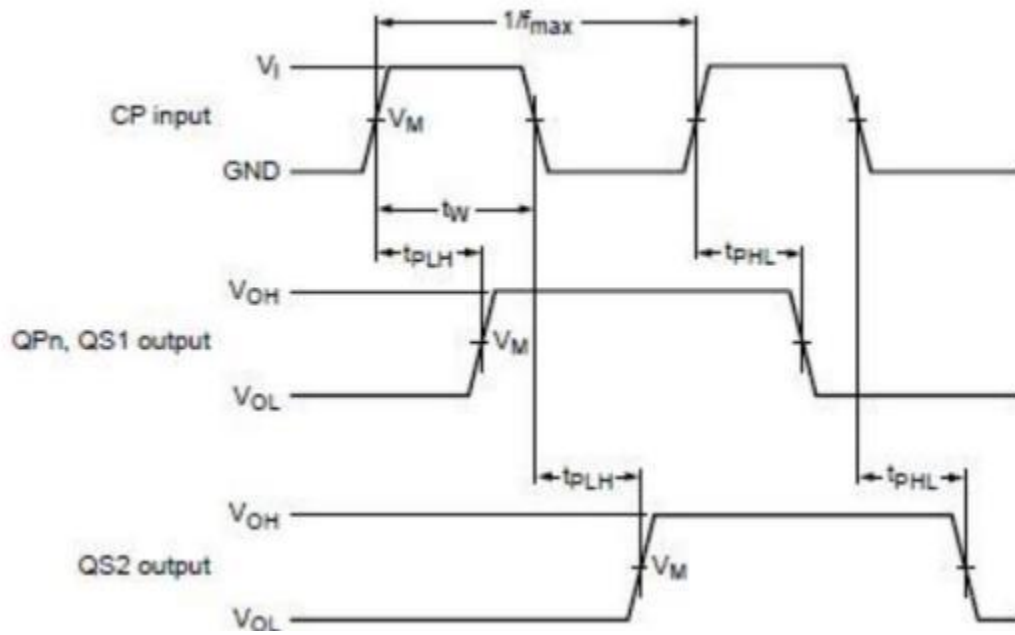


Figure 6. Clock to outputs propagation delays, and clock pulse width and maximum frequency

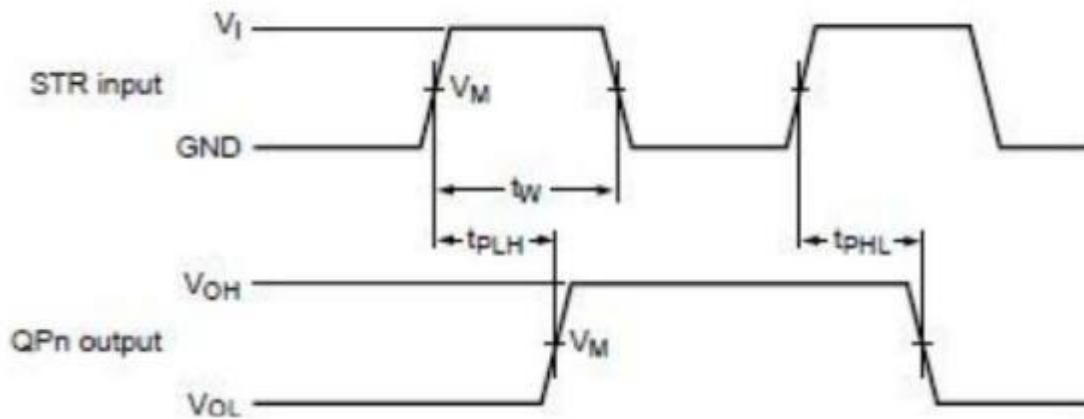


Figure 7. Strobe to output propagation delays, and strobe pulse width, set up and hold times

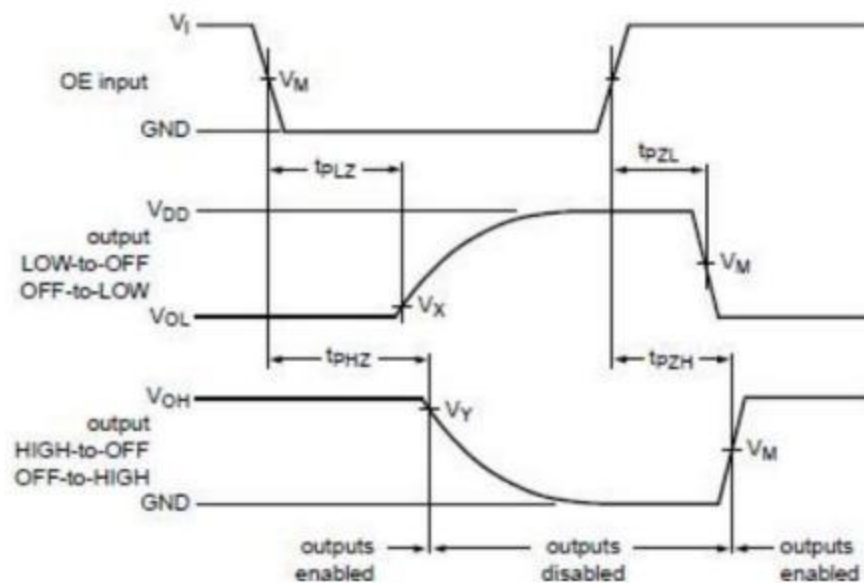


Figure 8. 3-state output enable and disable times for OE input

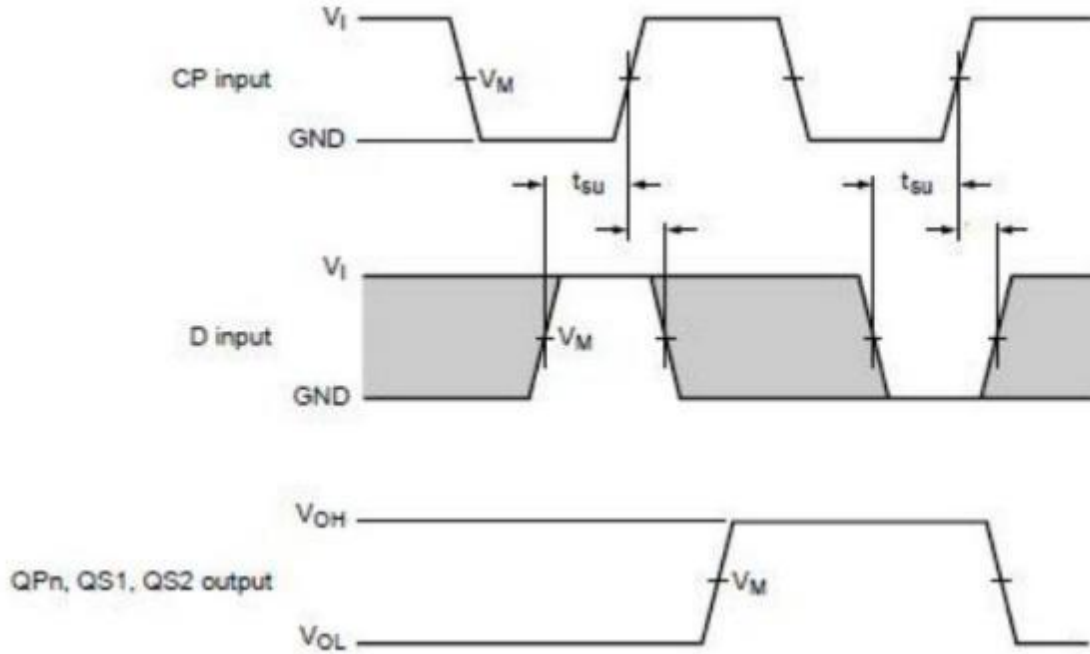


Figure 9. Data input data set up and hold times

**Measurement Points**

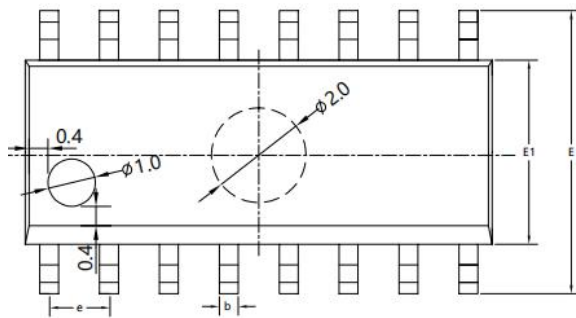
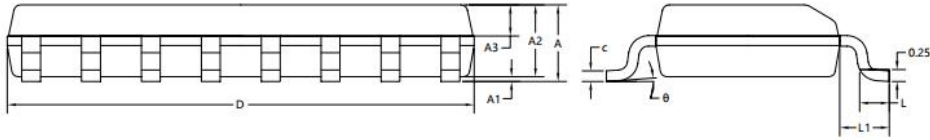
Supply voltage	Input	Output		
$V_{DD}$	$V_M$	$V_M$	$V_X$	$V_Y$
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

**Test Data**

Supply voltage	Input		Load		Load		
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$
5V to 15V	$V_{SS}$ or $V_{DD}$	$\leq 20ns$	50pF	1KΩ	open	$V_{SS}$	$V_{DD}$

**Package Information**

SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

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