

Product Specification

XBLW SG3526

Performance pulse width modulator integrated circuit

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General Description

The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

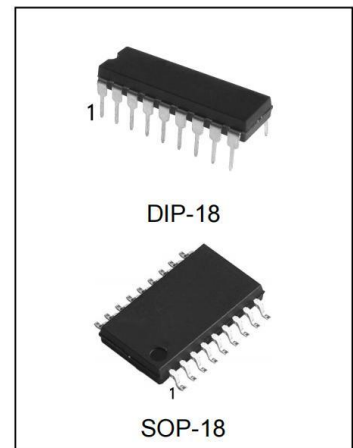
Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering.

All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility.

The versatility of this device enables implementation or transformer coupled

Features

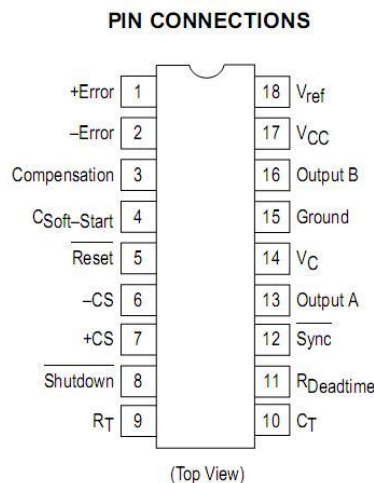
- 8.0V to 35V Operation
- 5.0V \pm 1% Trimmed Reference
- 1.0Hz to 400KHz Oscillator Range Dual Source/Sink Current Outputs: \pm 100mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage-Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode
- Range Guaranteed 6 Unit Synchronization



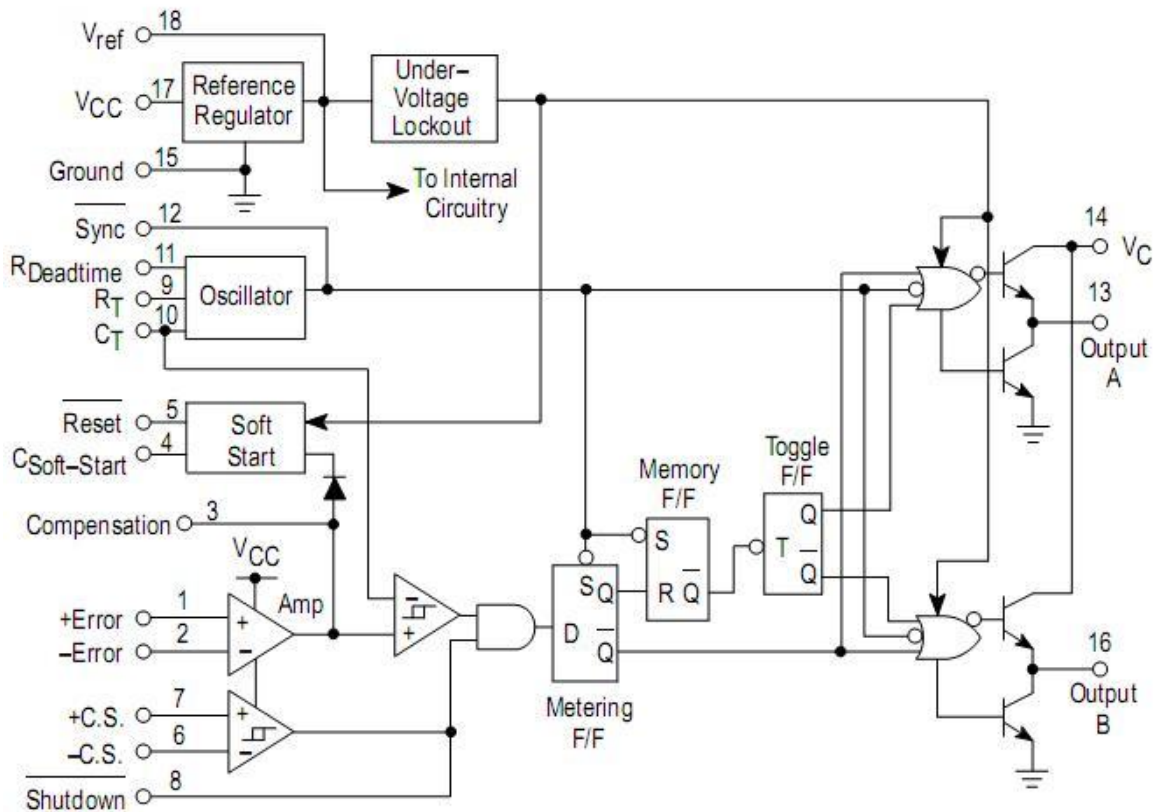
Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SG3526N	DIP-18	SG3526N	Tube	1000/Box
XBLW SG3526DTR	SOP-18	SG3526	Tape	2000/Reel

Block Diagram And Pin Description



Representative Block Diagram



Maximum Ratings (Note1)

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	+40	Vdc
Collector Supply Voltage	Vc	+40	Vdc
Logic Inputs		-0.3 to + 5.5	V
Analog Inputs		-0.3 to +5.5	V
Output Current,Source or Sink	Io	±200	mA
Reference Load Current(Vcc=40V Note2)	Iref	50	mA
Logic Sink Current		15	mA
Power Dissipation Ta=+25°C (note3)	Pd	1000	mW
Operating Temperature Range	Ta	0~70	°C
Storage Temperature Range	Tstg	-65 to +150	°C
Lead Temperature(Soldering, 10Seconds)	Tsolder	±300	°C

NOTES:

Values beyond which damage may occur.
Maximum junction temperature must be observed.
Derate at 10 mW/°C for ambient temperatures above +50°C.

Recommended Operating Conditions

Characteristics		Symbol	Min	Max	Unit	
Supply Voltage		Vcc	8.0	35	Vdc	
Collector Supply Voltage		Vc	4.5	35	Vdc	
Output Sink/Source Current(Each Output)		Io	0	±100	mA	
Reference Load Current		Iref	0	20	mA	
Oscillator Frequency Range		Fosc	0.001	400	Khz	
Oscillator Timing Resistor		Rt	2.0	150	KΩ	
Oscillator Timing Capacitor		Ct	0.001	20	uF	
Available Deadtme Range(40Khz)			3.0	50	%	
Operating Junction Range	Temperature	Tj	0	+125	°C	
Minimum Frequency (Rt=150Kohm,Ct=20uF)	Fmin		0.5		Hz	
Maximum Frequency (Rt=2.0Kohm,Ct=0.001uF)	Fmax	400	-	-	KHz	
Sawtooth Peak Voltage(Vcc=35V)	Vosc(p)	-	3.0	3.5	V	
Sawtooth Valley Voltage(Vcc=8.0V)	Vosc(V)	0.45	0.8	-	V	
Error Amplifier Section (note6)						
Input Offset Voltage		Vio		2.0	10	mV
Input Bias Current		Iib		-350	-2000	nA
Input Offset Current		Iio		35	200	nA
Characteristics		Symbol	Min	Typ	Max	Unit
DC Open Loop Gain(RI≥10Mohm)		Av	60	72		dB
High Output Voltage (Vpin1-Vpin2≥+150mV, Isource=100uA)		Voh	3.6	4.2		V
Low Output Voltage (Vpin2-Vpin1≥+150mV, Isink=100uA)		Vol		0.2	0.4	V
Common Mode Rejection Ratio(Rs≤2.0Kohm)		CMRR	70	94		dB
Power Supply Rejection Ration(+12V≤Vcc≤+18V)		PSRR	66	80		dB
PWM Comparator Section(Note5)						
Minimum Duty Cycle (Vcompensation = +0.4V)		Dcmin			0	%
Maximum Duty Cycle (Vcompensation = +3.6V)		Dcmax	45	49		%
Digital Ports(SYNC, SHUTDOWN,RESET)						

Output Voltage (High Logic Level) (I _{source} =40uA) (Low Logic Level) (I _{sink} =3.6mA)	V _{oh} V _{ol}	2.4	4.0 0.2	0.4	V
Input Current-High Logic Level (High Logic Level) (V _{ih} =+2.4V) (Low Logic Level) (V _{il} = +0.4V)	I _{ih} I _{il}		-125 -225	-200 -360	uA
Current Limit Comparator Section(note7)					
Sense Voltage(R _s ≤50 Ω)	V _{sense}	80	100	120	mA
Input Bias Current	I _{ib}		-3.0	-10	uA
Soft-Start Section					
Error Clamp Voltage(Reset=+0.4V)			0.1	0.4	V
Csoft-Start Charging Current(Reset=+2.4V)	I _{cs}	50	100	150	uA
Output Drivers(each output, V_c=+15Vdc)Unless otherwise noted.					
Output High Level I _{source} = 20mA I _{source} = 100mA	V _{oh}	12. 5 12	13. 5 13		V
Output Low Level I _{sink} = 20 mA I _{sink} = 100mA	V _{ol}		0.2 1. 2	0.3 2.0	V
Collector Leakage,V _c =+40V	I _{c(Leak)}	-	50	150	uA
Rise Time(CL=1000pF)	T _r		0.3	0.6	uS
Fall Time(CL=1000pF)	T _f		0.1	0.2	uS
Supply Current (Shutdown = +0.4V, V _{cc} =+35V, R _t =4.12K Ω)	I _{cc}	-	18	30	mA

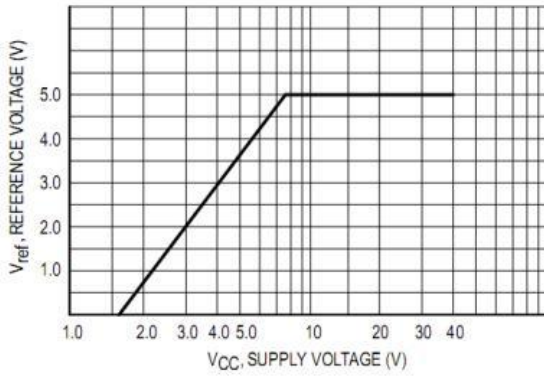
Notes:

 T_{low} = 0 °C T_{high} = +125°C

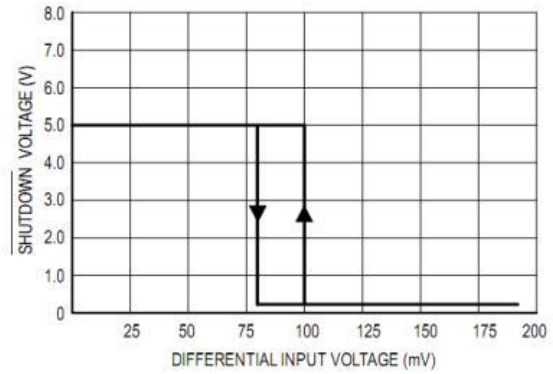
 f_{osc}=40KHz(R_t=4.12k Ω±1%,C_T=0.01uF±1%, R_D=0 Ω)

 0V ≤ V_{CM} ≤ +5.2V

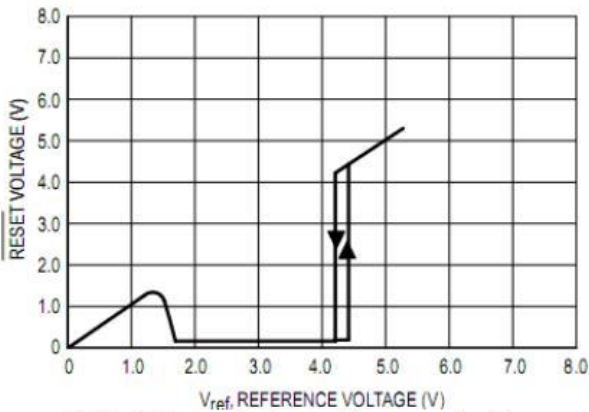
 0V ≤ V_{CM} ≤ +12V



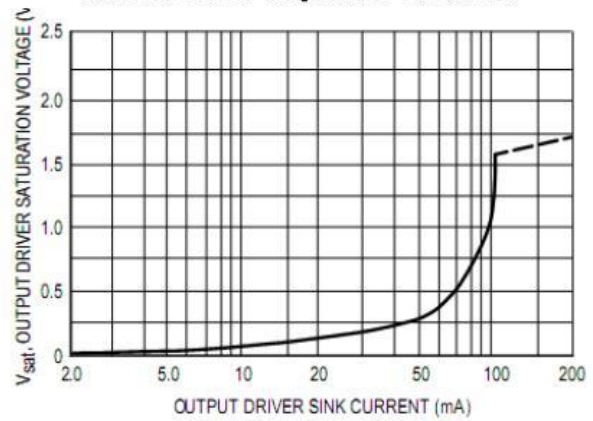
Reference Voltage as a Function Supply Votage



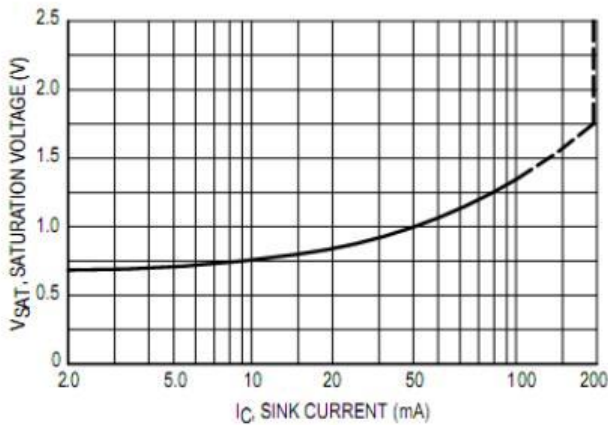
Current Limit Comparator Threshold



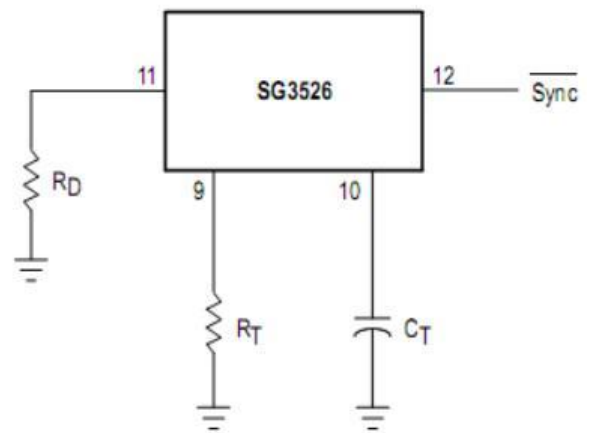
UnderVoltage Lockout Characteristic



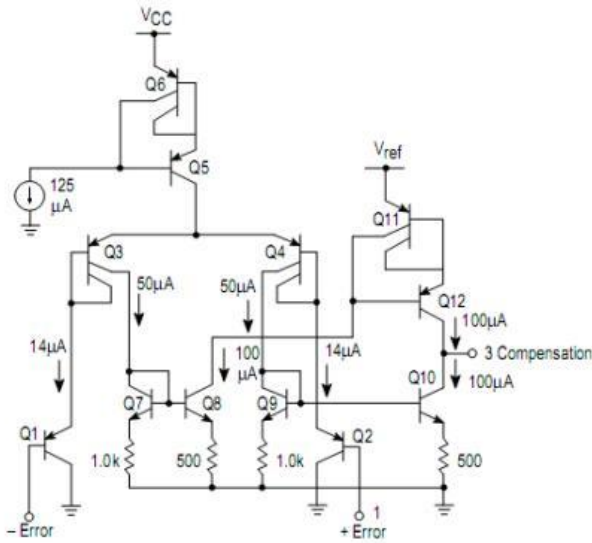
Output Driver Saturation Voltage as a Function of Sink Current



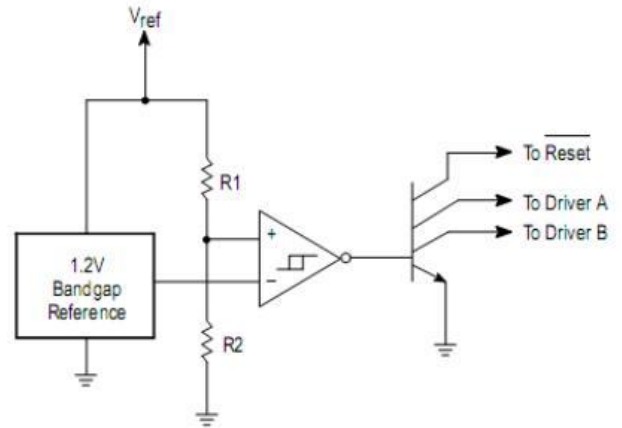
Vc Saturation Voltage as a Function of Sink Current



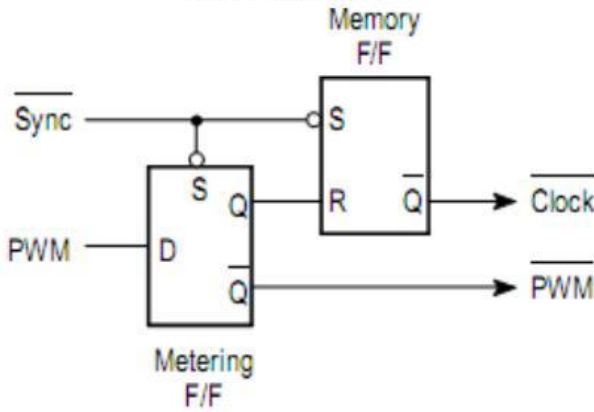
Oscillator Connections



Error Amplifier



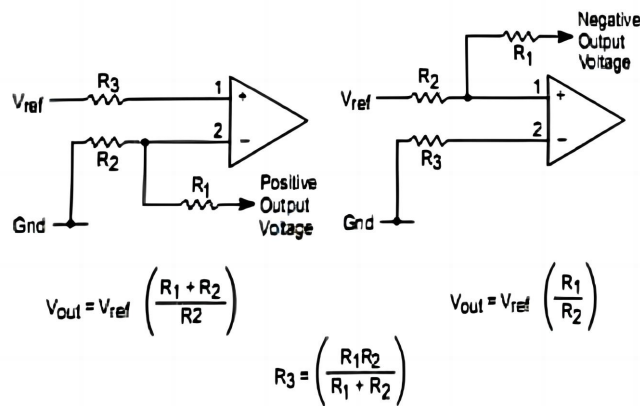
Undervoltage Lockout



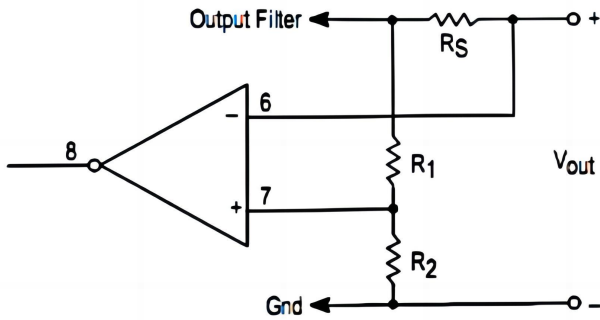
The metering Flip-Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip-Flop prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

Pulse Processing Logic



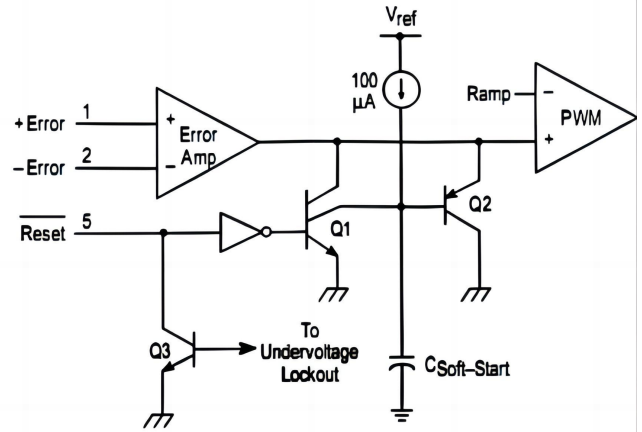
Error Amplifier Connects



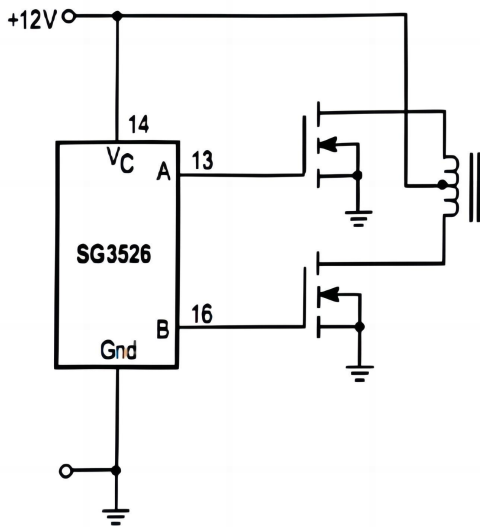
$$I_{(max)} = \frac{\left(0.1V + \frac{V_{out} R_1}{R_1 + R_2}\right)}{R_S}$$

$$I_{SC} = \left(\frac{0.1V}{R_S}\right)$$

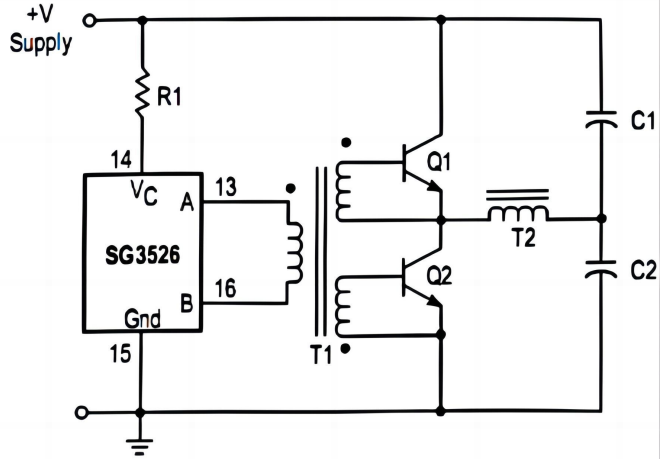
Foldback Current Limiting



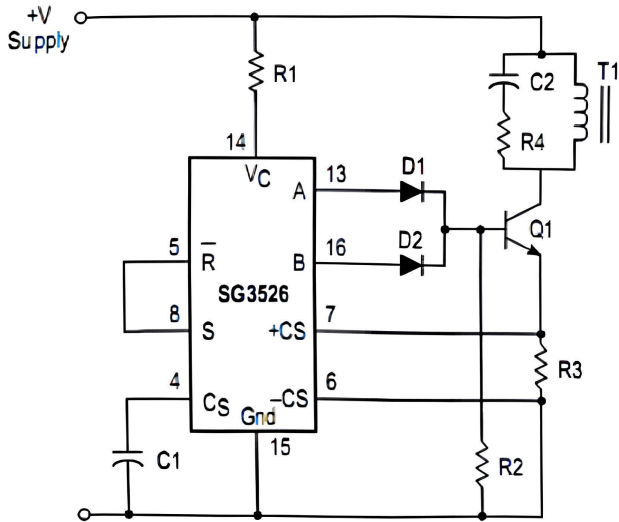
Soft-Start Circuitry



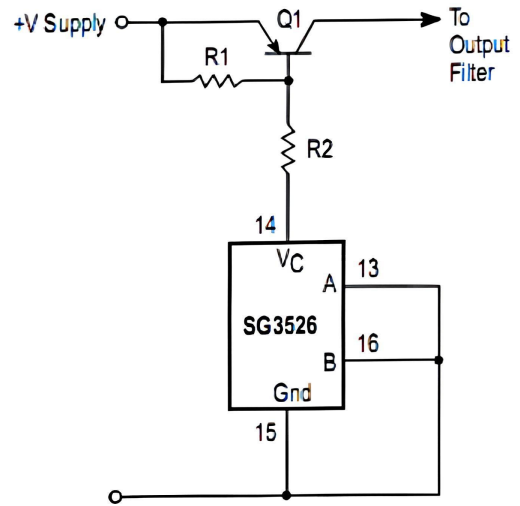
Driving VMOS Power FETs



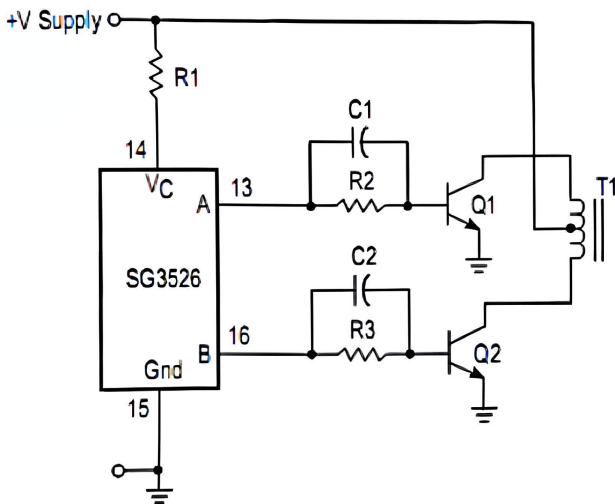
Half-Bridge Configuration



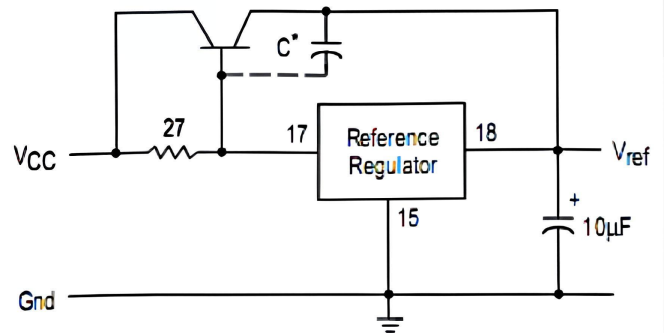
Flyback Converter with Current Limiting



Single-Ended Configuration



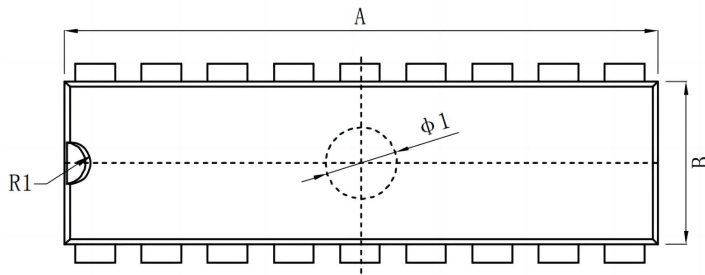
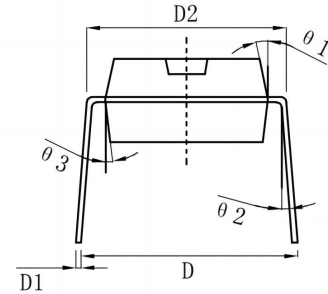
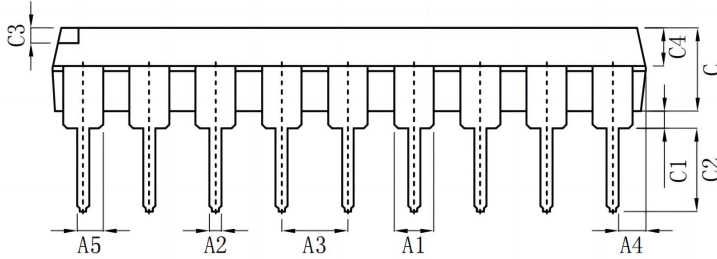
Push-Pull Configuration



Extending Reference Output Current Capability

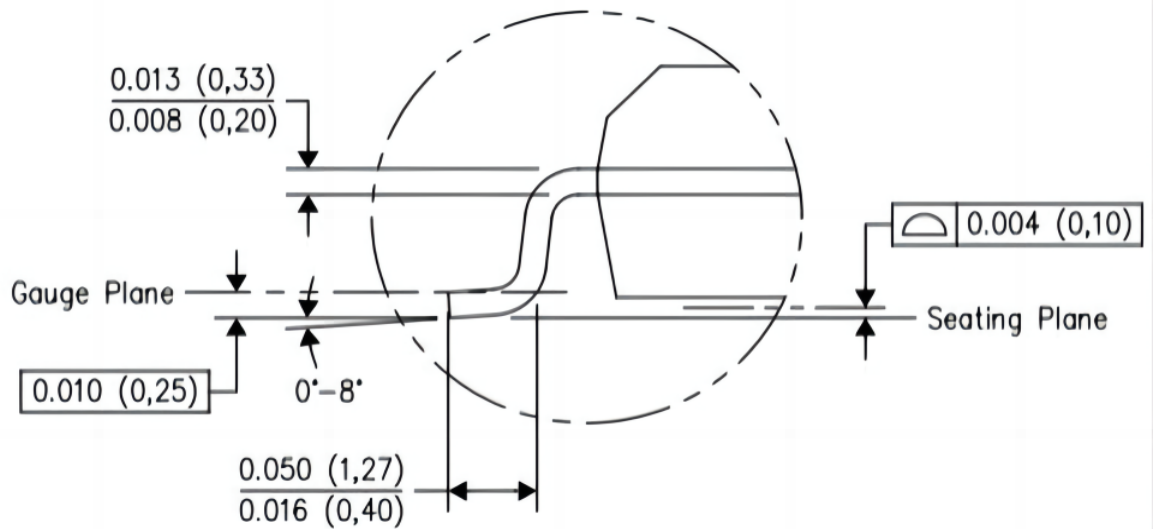
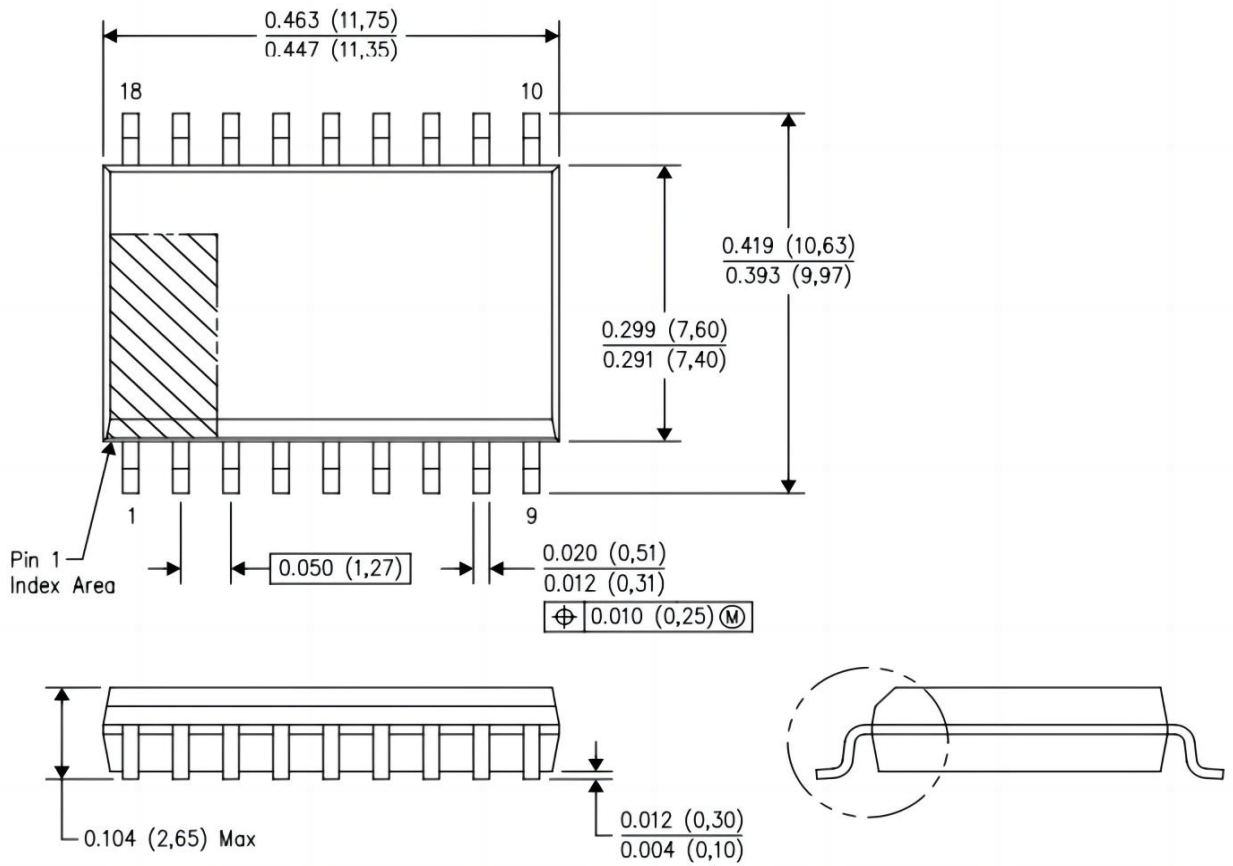
Package Information

DIP-18



Size Symbol	MIN(mm)	MAX(mm)	Size Symbol	MIN(mm)	MIN(mm)
A	22.76	22.96	C3	0.60	0.70
A1	1.524TYP		C4	1.47	1.57
A2	0.41	0.51	D	8.20	8.80
A3	2.54TYP		D1	0.20	0.35
A4	1.042TYP		D2	7.62	7.87
A5	0.991TYP		R1	0.80TYP	
B	6.25	6.45	$\theta 1$	12° TYP4	
C	3.20	3.40	$\theta 2$	5° TYP	
C1	0.65	0.85	$\theta 3$	7° TYP4	
C2	3.20	3.40	$\phi 1$	3.0*0.1TYP	

SOP-18



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