

Description

The TX15N10B is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

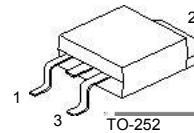
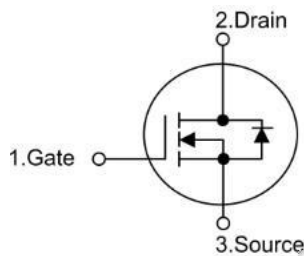
Features

V _{DS}	100V
R _{DS(on)Max.}	100mΩ
I _D	15A

- Super high density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability

Pin configuration

Order Number	Package
TX15N10B	TO-252



Maximum Ratings (T_c = 25°C unless otherwise noted*)

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V _{DSS}	100	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current	I _D	T _c =25°C	15
		T _c =70°C	14
Pulsed Drain Current	I _{DM}	59	A
Power Dissipation	P _D	T _c =25°C	34.7
		T _c =70°C	22.2
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55~+175	°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ.	R _{thCS}	0.5	°C/W
Thermal resistance junction to case.	R _{thJC}	3.6	°C/W
Thermal resistance junction to ambient.	R _{thJA}	110	°C/W

Electrical characteristics (TA =25°C Unless Otherwise Specified)

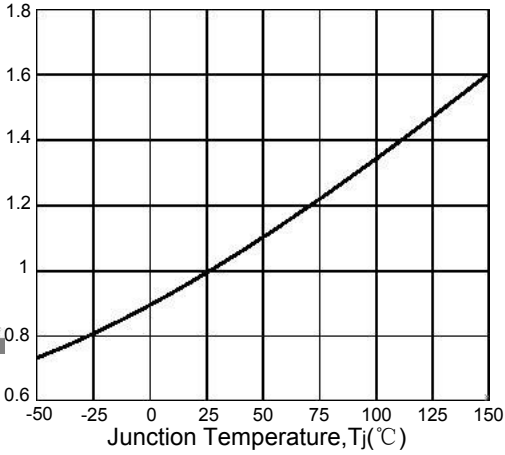
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250μA	100	—	—	V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	1	—	3	V
IGSS	Gate-Body Leakage	VDS=0V, VGS=±20V	—	—	±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=100V, VGS=0V	—	—	1	μA
RDS(ON)	Drain-Source On-Resistance	VGS=10V, ID=8A	—	80	100	mΩ
VSD	Diode Forward Voltage	IS=8A, VGS=0V	—	0.9	1.2	V
DYNAMIC						
Qg	Total Gate Charge	VDD=80V, VGS=10V, ID=10A		24		nC
Qg	Total Gate Charge	VDD=80V, VGS=4.5V, ID=10A	—	13	—	
Qgs	Gate-Source Charge		—	4.6	—	
Qgd	Gate-Drain Charge		—	7.6	—	
Rg	Gate Resistance	VDS=0V, VGS=0V, f=1MHz	—	0.9	—	Ω
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1MHz	—	890	—	pF
Coss	Output Capacitance		—	58	—	
Crss	Reverse Transfer Capacitance		—	23	—	
td(on)	Turn-On Delay Time	VDS =50V, RG=1Ω RL=5Ω, VGEN=10V,	—	14	—	ns
tr	Turn-On Rise Time		—	33	—	
td(off)	Turn-Off Delay Time		—	39	—	
tf	Turn-Off Fall Time		—	5	—	

Notes :a. Pulse test:pulse width 300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

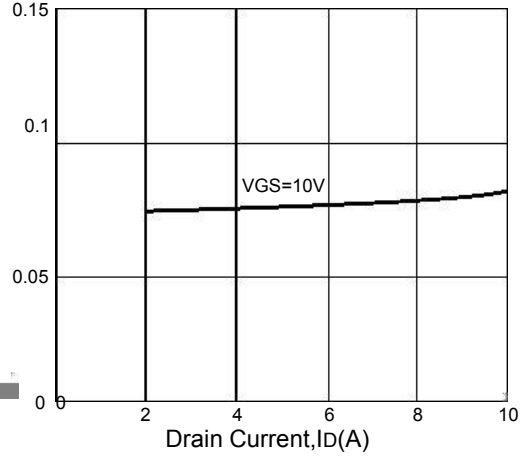
b. XDSSEMI reserves the right to improve product design,functions and reliability without notice.

Typical Characteristics (T_J =25°C Noted)

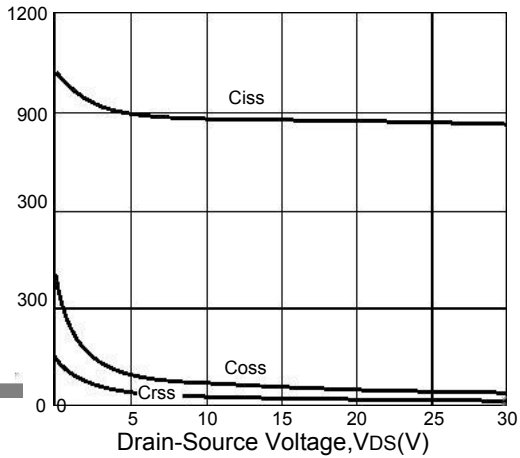
On Resistance vs. Junction Temperature



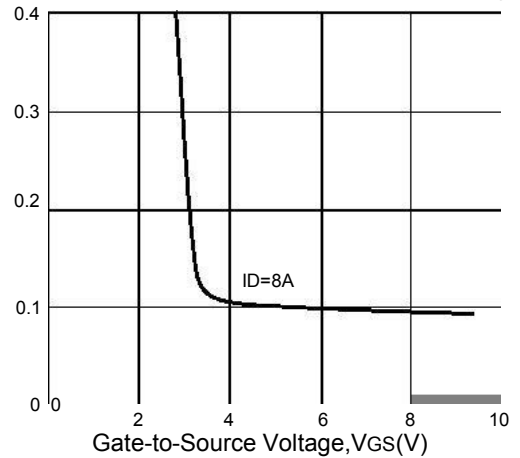
On Resistance vs. Drain Current



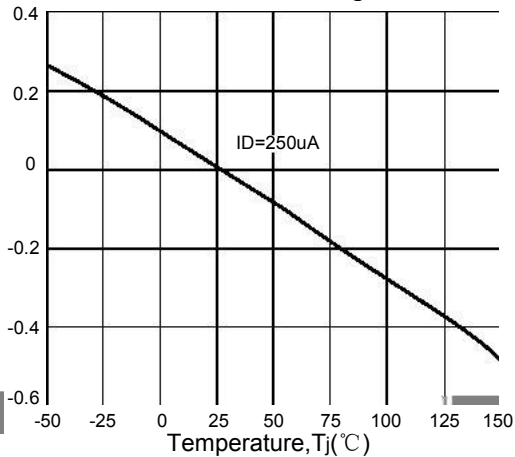
Capacitance



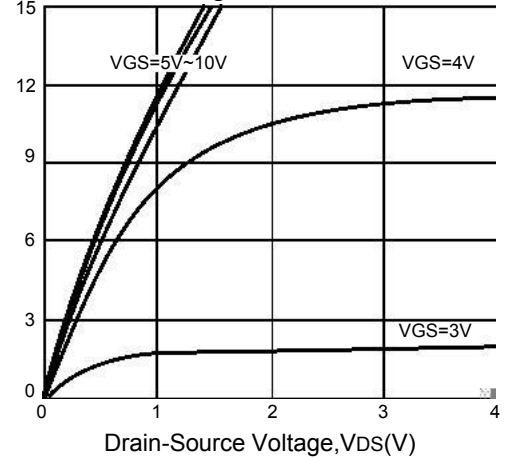
On Resistance vs. Gate-to-Source Voltage



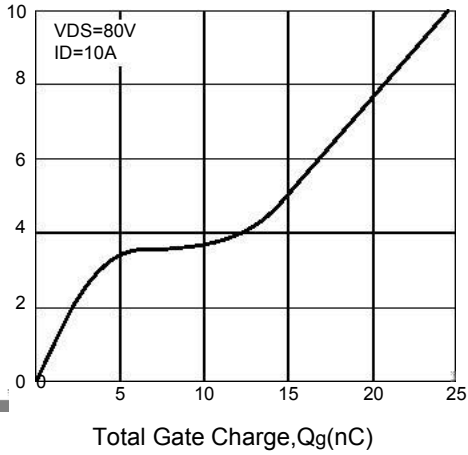
Threshold Voltage



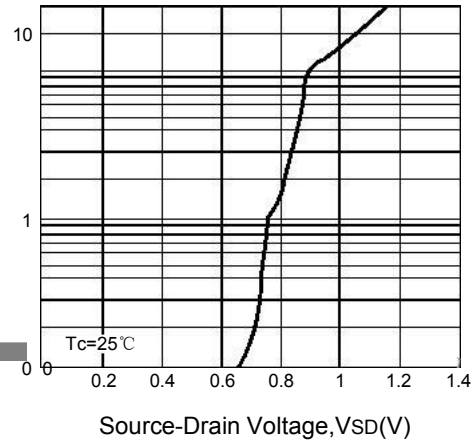
Gate Charge Characteristics



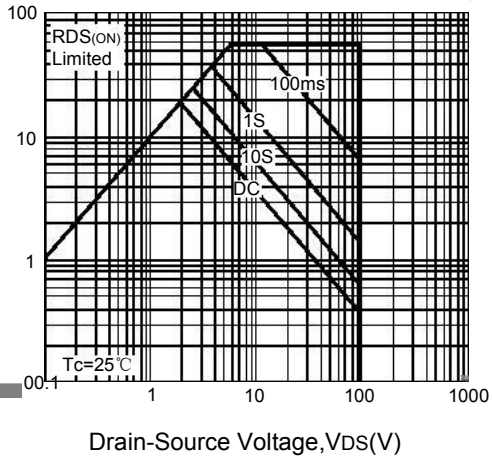
Typical Characteristics(T_J=25°C)



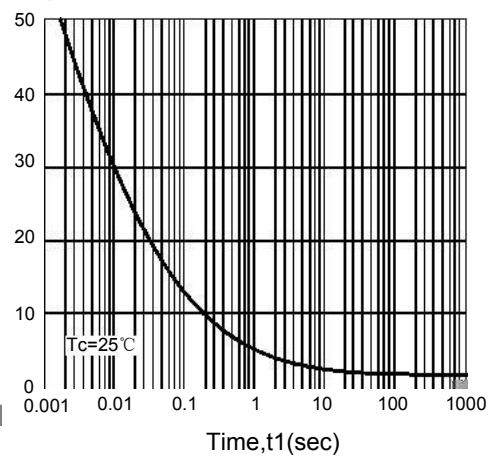
Body diode characteristics



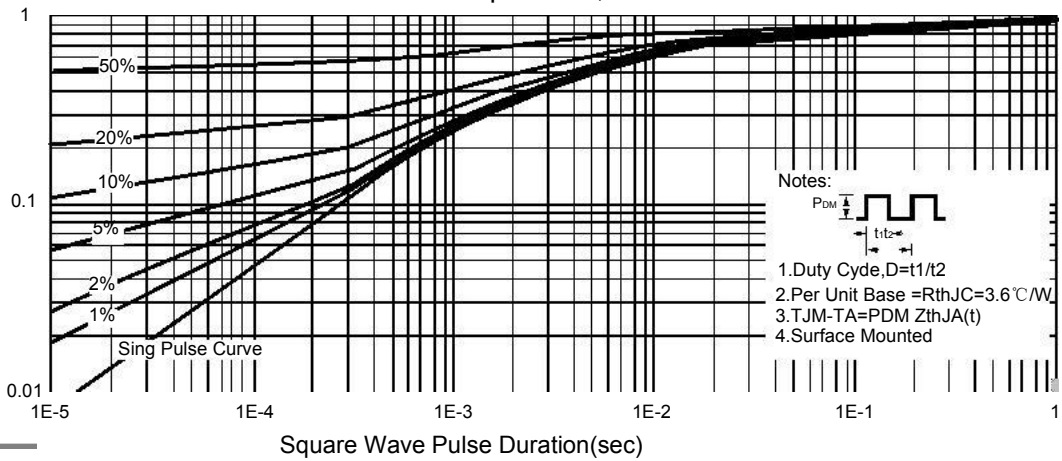
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation

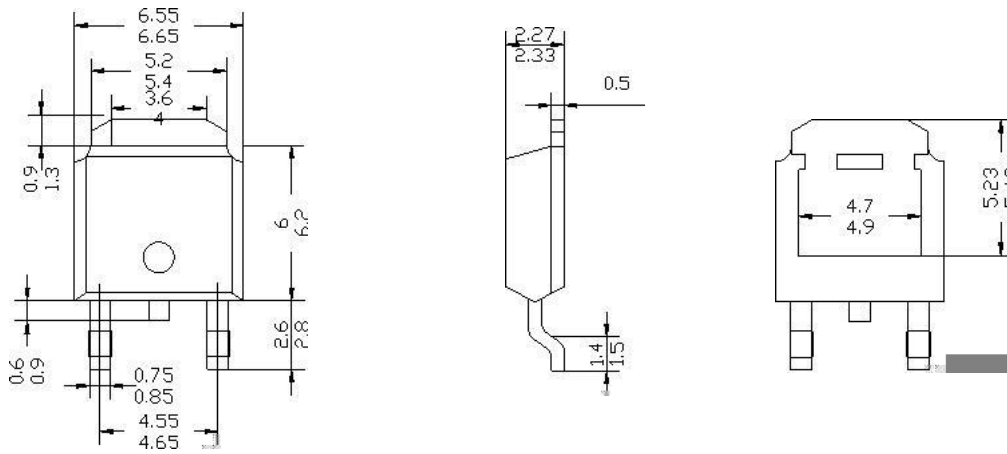


Normalized Thermal Transient Impedance, Junction to Ambient



SOT-89

Unit: mm



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