KCU1250 Board

User Guide

UG1057 (v1.0) December 19, 2014

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/19/2014	1.0	Initial Xilinx release.

Table of Contents

Appendix F: Regulatory and Compliance Information

Appendix F: Additional Resources and Legal Notices

Chapter 1

KCU1250 Board Features and Operation

Introduction

This user guide describes the components, features, and operation of the KCU1250 UltraScale™ FPGA GTH transceiver characterization board. The KCU1250 board provides the hardware environment for characterizing and evaluating the GTH transceivers on an UltraScale XCKU040-2FFVA1156E FPGA. The KCU1250 board schematic, bill-of-material (BOM), layout files, and reference designs are available at the Kintex® UltraScale FPGA KCU1250 Characterization Kit website.

FPGA Compatibility

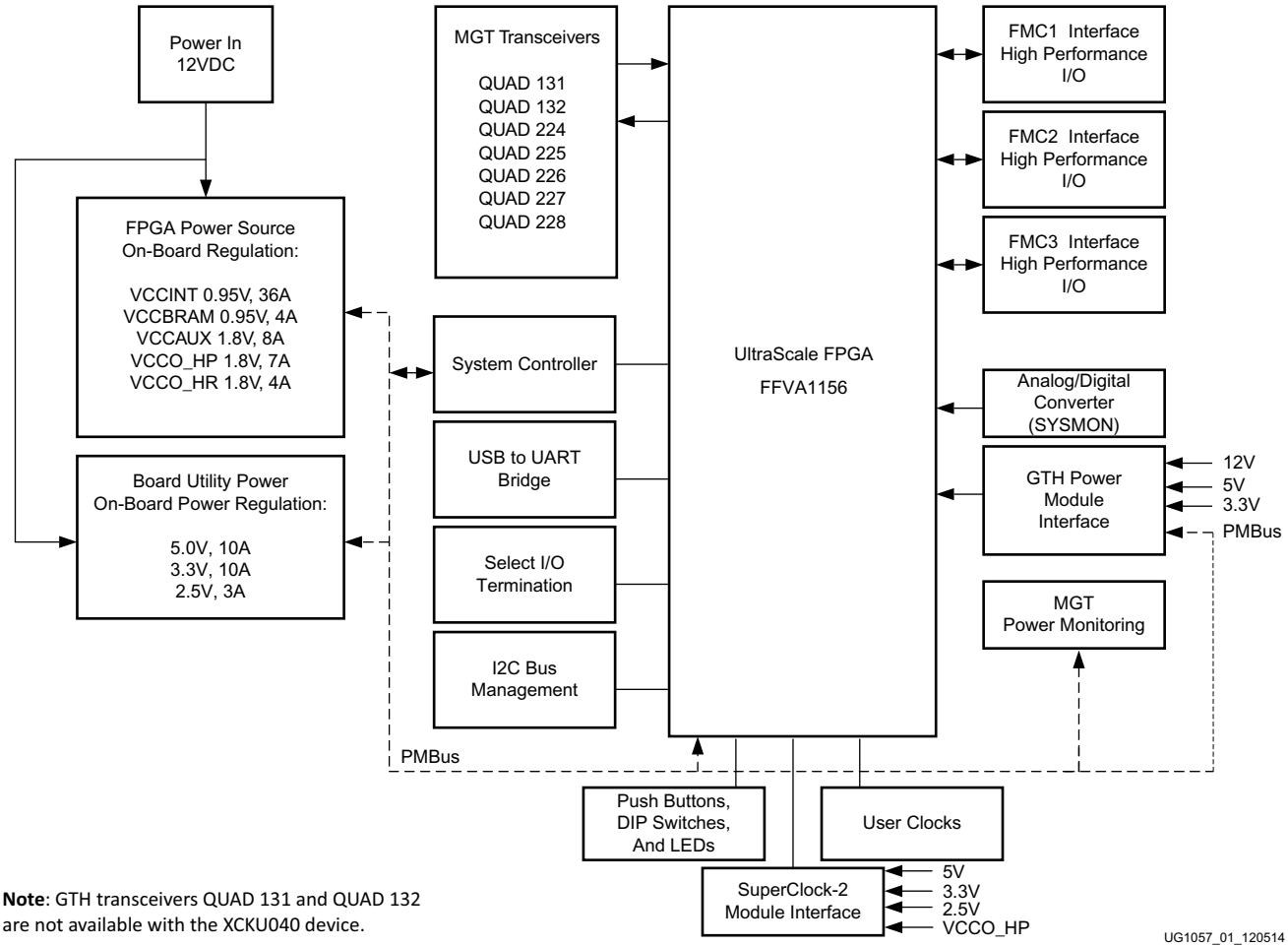
The KCU1250 board is shipped with the Kintex UltraScale XCKU040-2FFVA1156E FPGA. The board also supports other Kintex UltraScale device densities (XCKU035, XCKU060, and XCKU075) in the pin-compatible FFVA1156 package. However, certain GTH transceivers that are available in larger density devices are not available in the XCKU040 device (for example, GTH QUAD_131 and GTH QUAD_132).

KCU1250 Board Features

- UltraScale XCKU040-2FFVA1156E FPGA
- BullsEye cable access to all 20 GTH transceivers on the UltraScale XCKU040-2FFVA1156E FPGA
- Onboard power supplies for all necessary voltages
- Power connectors for optional use of external power supplies
- Digilent USB JTAG programming port
- System controller (Zynq-7000 AP SoC XC7Z010-CLG225)
- MGT power module supporting UltraScale FPGA GTH transceiver power requirements
- A fixed, 300 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting programmable clock outputs

- Samtec BullsEye connector pads for the FPGA GTH transceivers and reference clocks
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Three VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB to dual-UART bridge
- I2C bus
- PMBus connectivity to the boards digital power supplies
- Active cooling for the FPGA

The KCU1250 board block diagram is shown in Figure 1-1.



Note: GTH transceivers QUAD 131 and QUAD 132 are not available with the XCKU040 device.

Figure 1-1: **KCU1250 Board Block Diagram**

Detailed Description

Figure 1-2 shows the KCU1250 board. Each numbered feature referenced in Figure 1-2 is described in Table 1-1 and in subsequent sections.

CAUTION! *The KCU1250 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board*

CAUTION! *Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board*

IMPORTANT: *Figure 1-2 is for reference only and might not reflect the current revision of the board.*

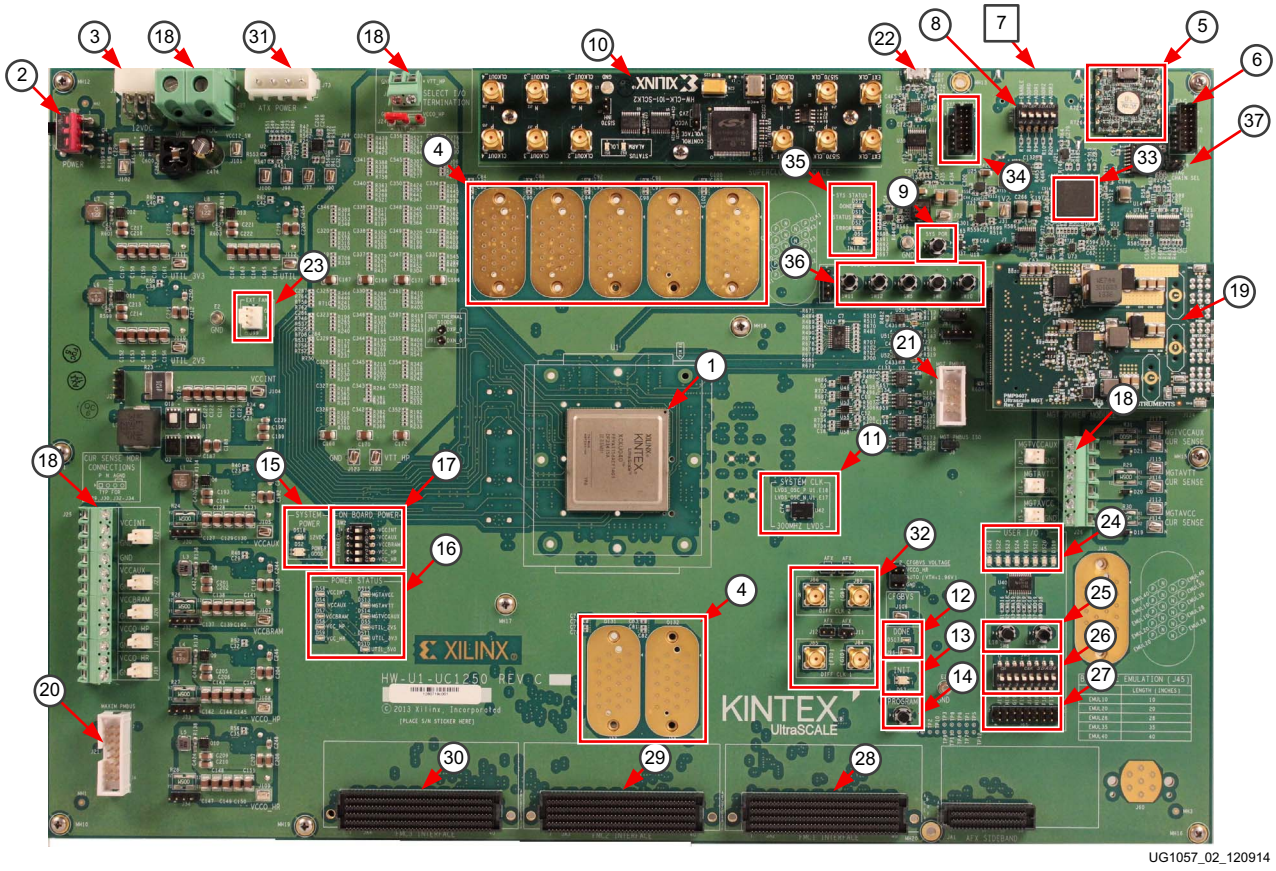


Figure 1-2: **KCU1250 Board Features**

Table 1-1 describes the callouts in Figure 1-2.

Table 1-1: **KCU1250 Board Features and Operation**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	UltraScale XCKU040-2FFVA1156E FPGA, page 18
2	SW1	Power switch, page 10
3	J28	12V mini-fit connector, page 9
4	J37, J38, J39, J40, J41, J42, J43	GTH transceiver connector pads Q224, Q225, Q226, Q227, Q228 page 28
5	U80	Digilent USB JTAG connector (micro-B receptacle), page 18
6	J2	Platform USB JTAG connector (alternate access for programming cables), page 18
7	J10	SD card connector (back-side of board), page 18
8	SW13	System controller configuration DIP switches, page 21
9	SW4	System controller power on reset (SYS_POR) button, page 20
10	J36	SuperClock-2 module, page 24
11	U42	300 MHz LVDS oscillator, page 23
12	DS17	FPGA DONE status LED, page 25
13	DS3	FPGA INIT status LED, page 25
14	SW7	FPGA PROGRAM pushbutton, page 27
15	DS18	12V system power status LED, page 14
16	DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS28, DS13, DS14, DS15	Status LEDS for FPGA logic, transceiver and utility power
17	SW2	Power regulation inhibitor switch for onboard regulators, page 13
18	J5, J25, J26, J27	External power supply connectors, page 13 and page 14
19	J46, J124	MGT transceiver power supply module, page 15
20	J21	FPGA and utility rails PMBUS connector, page 14
21	J4	MGT rails PMBUS connector, page 13
22	J1	Connector for USB to dual-UART bridge (mini-B receptacle), page 23
23	J99	Power connector for active heatsink, page 16
24	DS19, DS20, DS21, DS22, DS23, DS24, DS25, DS26	User LEDs (active-High), page 25
25	SW8, SW9	User pushbuttons (active-High), page 27
26	SW3	User DIP switches (active-High), page 26
27	J95	User I/O header, page 27
28	JA2	FMC1 connector, page 35
29	JA3	FMC2 connector page 38

Table 1-1: **KCU1250 Board Features and Operation *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
30	JA4	FMC3 connector page 41
31	J73	ATX power connector page 9
32	J83, J84, J85, J86	SMA connectors to differential MRCC pins on FPGA, page 23
33	U38	System controller
34	J3	System controller JTAG connector
35	DS1, DS12, DS16, DS27	System controller status LEDs
36	SW5, SW6, SW10, SW11, SW12	System controller GPIO pushbuttons
37	J36	JTAG chain select

Power Management

12V Input Power

The KCU1250 board receives 12V main power through J28 (callout 3, Figure 1-2) using the 12V AC adapter included with the KCU1250 board characterization kit. J28 is a 6-pin (2 x 3), right angle, mini-fit connector.

CAUTION! *When supplying 12V through J28, use only the power supply provided for use with this board (Xilinx part number 3800033).*

CAUTION! *Do NOT use a 6-pin, PC ATX power supply connector with J28. The pinout of the 6-pin, PC ATX connector is not compatible with J28 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.*

12V power can also be provided through:

- Connector J73 (callout 31, Figure 1-2), which accepts an ATX hard drive 4-pin power plug
- Connector J27 (callout 18, Figure 1-2), which can be connected to a bench-top power supply

CAUTION! *Because connector J73 provides no reverse polarity protection, use a power supply with a current limit set at 6A maximum.*

CAUTION! *Do NOT apply 12V power to more than a single input source. For example, do not apply power to J73 and J27 at the same time.*

CAUTION! *The KCU1250 board uses a P-channel MOSFET power switch (FDS6681Z, reference designator Q1) that is rated for 20A @ 12V. It is critical that the power consumed by the DUT and peripheral circuitry does not exceed this limit.*

Power Switch

The KCU1250 board main power is turned on or off using the SW1 switch (callout 2, Figure 1-2). When the switch is in the on position, power is applied to the board and the green LED DS18 illuminates (callout 15, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

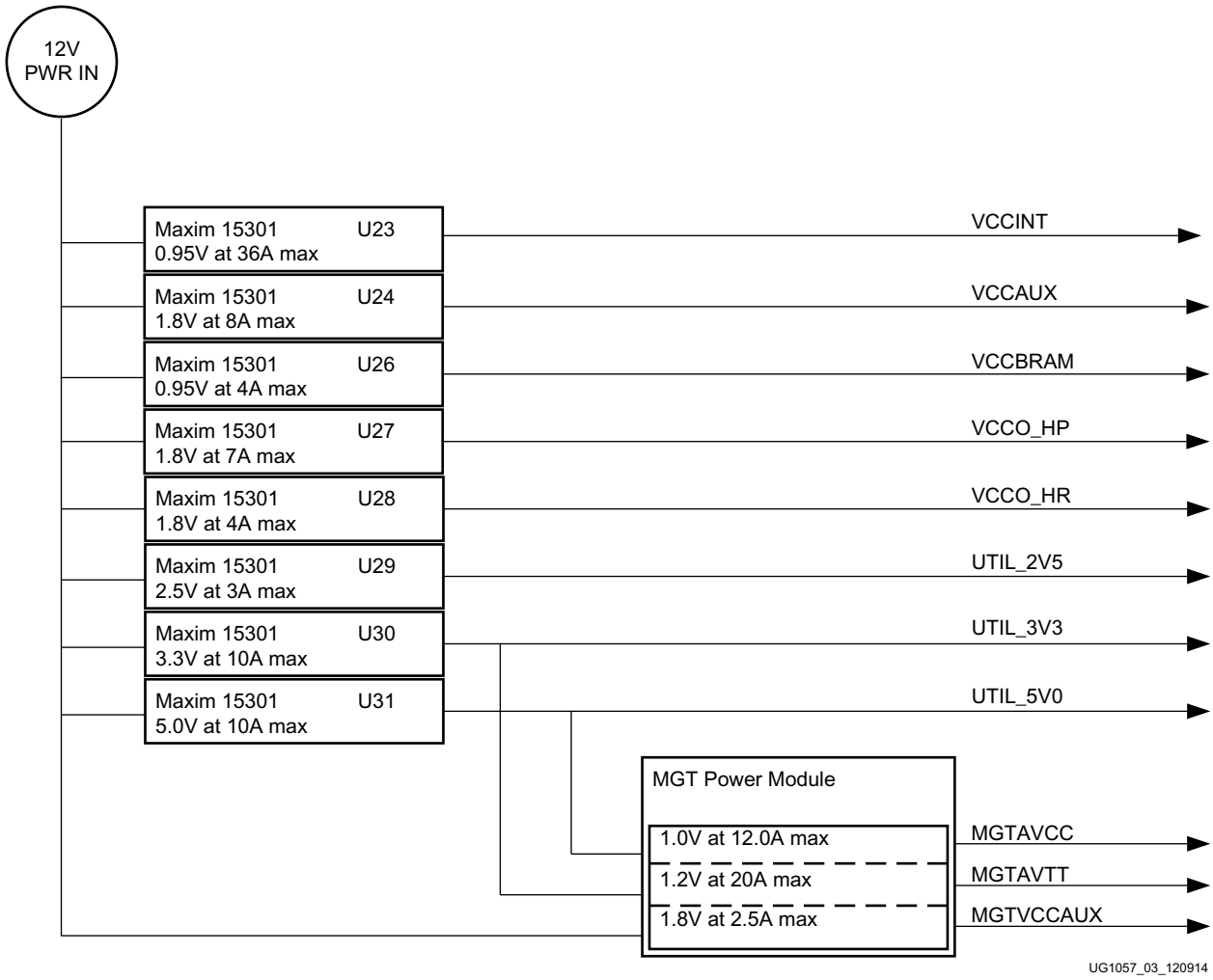


Figure 1-3: **KCU1250 Board Power Supply Block Diagram**

The KCU1250 board uses power regulators and PMBus compliant digital PWM system controllers from Maxim Integrated to supply the FPGA logic and utilities voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator	Description	Power Rail Net Name	Voltage
FPGA Logic				
Maxim MAX15301	U23	InTune Digital Point of Load (PoL) Controller, 36A	V_{CCINT}	0.95V
Maxim MAX15301	U24	InTune Digital Point of Load (PoL) Controller, 8A	V_{CCAUX}	1.8V
Maxim MAX15301	U26	InTune Digital Point of Load (PoL) Controller, 4A	V_{CCBRAM}	0.95V
Maxim MAX15301	U27	InTune Digital Point of Load (PoL) Controller, 7A	V_{CCO_HP}	1.8V
Maxim MAX15301	U28	InTune Digital Point of Load (PoL) Controller, 4A	V_{CCO_HR}	1.8V
Utility				
Maxim MAX15301	U31	InTune Digital Point of Load (PoL) Controller, 10A	UTIL_5V0	5.0V
Maxim MAX15301	U30	InTune Digital Point of Load (PoL) Controller, 10A	UTIL_3V3	3.3V
Maxim MAX15301	U29	InTune Digital Point of Load (PoL) Controller, 3A	UTIL_2V5	2.5V
MGT Transceivers (monitoring only)				
INA226	U50	Current shunt and power monitor with I2C interface	MGTAVCC	1.0V
INA226	U51	Current shunt and power monitor with I2C interface	MGTAVTT	1.2V
INA226	U52	Current shunt and power monitor with I2C interface	MGTVCCAUX	1.8V
System Controller				
Maxim MAX15053	U13	Fixed LDO regulator	SYS_1V0	1.0V
Maxim MAX15027	U33	Fixed LDO regulator	VCC_1V2	1.2V
Maxim MAX15027	U25	Fixed LDO regulator	VCC_1V8	1.8V

Notes:

1. The output voltages of the Max15301 can be reprogrammed using the Maxim InTune Digital Power Tool [Ref 5]. However, extreme caution must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components.

Using External Power Sources

Each power rail for the FPGA logic and MGT transceivers has an associated Euro-Mag spring-clamp terminal block (callout 18, Figure 1-2), which can be used to provide power from an external source (Table 1-3).

CAUTION! *Do NOT apply power to any of the FPGA logic external power supply connectors without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.*

Each onboard FPGA logic regulator can be disabled using its respective power regulation inhibitor dip switch (callout 17, Figure 1-2). A regulator is disabled when the power regulation inhibitor switch is set to the on position. Table 1-3 lists external power connectors for the different power rails.

Table 1-3: **FPGA Logic and MGT Transceiver Rails**

	Power Rail Net Name	External Supply Connector	Power Regulation Jumper
FPGA Logic	V_{CCINT}	J25	J22
	V_{CCAUX}		J23
	V_{CCBRAM}		J20
	V_{CCO_HP}		J19
	V_{CCO_HR}		J18
MGT Transceiver	MGTAVCC	J26	NA
	MGTAVTT		NA
	MGTVCCAUX		NA

Notes:

1. The MGT power module must be removed before providing external power to any of the transceiver rails (see MGT Transceiver Power Module, page 15)

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Monitoring Voltage and Current

Voltage and current monitoring and control for the Maxim power system is available through either the KCU1250 system controller or via the Maxim PowerTool™ software graphical user interface.

The KCU1250 system controller is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in Table 1-3. For details on how to use this built-in feature, see Power Monitoring Data Menu in Appendix D.

The KCU1250 board includes these PMBus connectors:

- J21 (callout 20, Figure 1-2), for use with the Maxim USB-to-PMBus interface dongle (MAXPOWERTOOL002 [Ref 8]) and the InTune Digital Power GUI.
- J4 (callout 21, Figure 1-2) is used to connect to the MGT power module PMBus using the vendor's application tool (for example, Texas Instruments USB-to-GPIO interface adaptor (EVM-P960 [Ref 9]) and the Fusion Digital Power GUI).

The onboard Maxim power controllers (U23, U24, U26, U27, U28, U29, U30, and U31) by default are isolated from the MGT power modules PMBus. However, the two interfaces can be linked by removing J8 next to the MGT power module PMBus connector J4. This configuration is required when using a Maxim MGT power module to allow for monitoring and controlling both FPGA power rails and the transceiver power rails using the Maxim InTune Digital Power GUI.

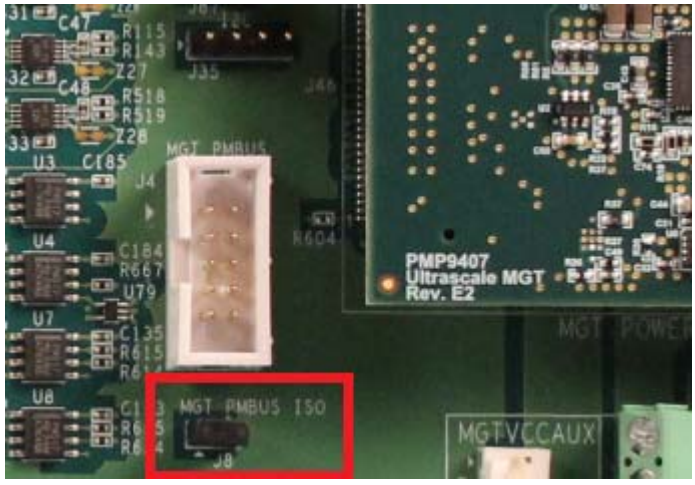


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Figure 1-4:

More information about the power system components used on the KCU1250 board is available from the Maxim Integrated InTune digital power website [Ref 5].

MGT Transceiver Power Module

The KCU1250 board includes one MGT transceiver power module (callout 19, Figure 1-2). The MGT power modules supply the MGTAVCC, MGTAVTT, and MGTVCCAUX power rails, which connect to the FPGA MGT transceivers. MGT power modules from third-party vendors are provided with the KCU1250 board for evaluation (Maxim Integrated MAXIM001 and Texas Instruments PMP9463 [Ref 5]). Either one of the modules can be plugged into J46 and J124 on the outlined and labeled power module locations shown in Figure 1-5.

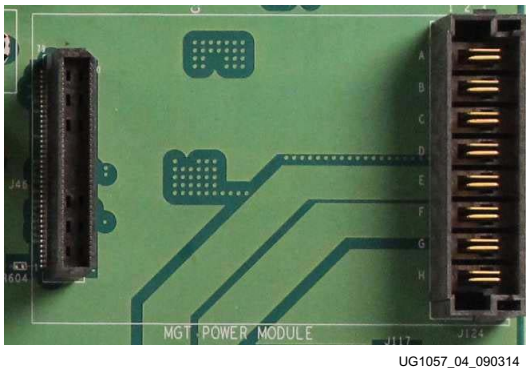

Figure 1-5: **Mounting Location, MGT Power Module**

Table 1-4 lists the nominal voltage values for MGTAVCC, MGTAVTT, and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by MGT modules included with the KCU1250 board.

Table 1-4: **MGT Power Modules**

MGT Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.0V	12A
MGTAVTT	1.2V	20A
MGTVCCAUX	1.8V	2.5A

The MGT transceiver power rails can also be supplied externally. The external supply connectors are described in Table 1-3.

CAUTION! *The MGT Power Module MUST be removed when providing external power to the MGT transceiver rails.*

Information about the available MGT power modules included with the KCU1250 board characterization kit is available from the vendor websites [Ref 5].

Active Heatsink Power Connector

An active heat sink (Figure 1-6) is provided for the FPGA (callout 23, Figure 1-2). A 12V fan is affixed to the heat sink and is powered from the 3-pin friction lock header J99 (Figure 1-7).

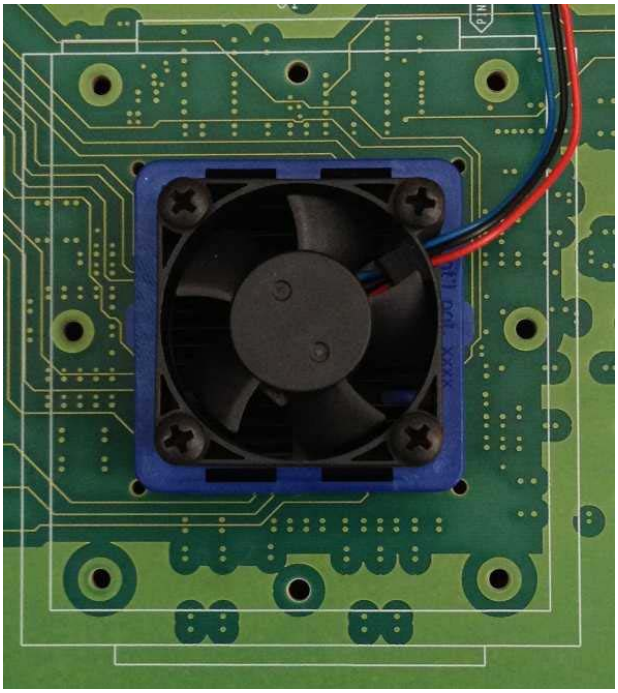

Figure 1-6: **Active FPGA Heat Sink**

The fan power connections are detailed in Table 1-6:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J99.1 - GND
Red	J99.2 - 12V
Blue	J99.3 - NC

Figure 1-7 shows the heat sink fan power connector J99.

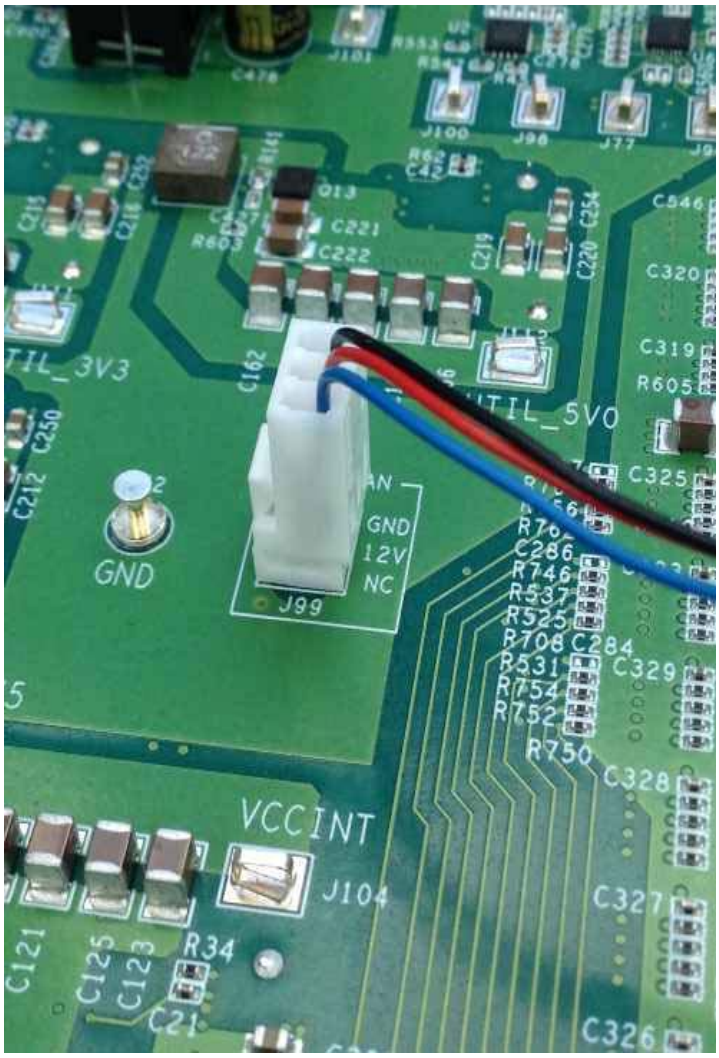

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Figure 1-7: **Heat Sink Fan Power Connector J99**

UltraScale FPGA

The KCU1250 board is populated with the UltraScale XCKU040-2FFVA1156E FPGA at U1 (callout 1, Figure 1-2). For further information on UltraScale FPGAs, see *UltraScale Architecture and Product Overview* (DS890) [Ref 1].

FPGA Configuration

The FPGA is configured though one of these options:

- Digilent embedded USB JTAG connector (callout 5, Figure 1-2)
- Platform cable USB JTAG cable connector (callout 6, Figure 1-2)
- SD card using the Zynq-7000 AP SoC system controller in 8-bit SelectMAP mode (callout 7, Figure 1-2)

The KCU1250 board includes an embedded USB-to-JTAG configuration module (Digilent U80), which allows a host computer to access the JTAG chain using a standard A to micro-B USB cable. Alternatively, a JTAG connector (J2) is available to access the JTAG chain using the Xilinx platform cable USB II configuration cable. Additionally, the FPGA can be configured from an SD card installed in J10 with the help of the system controller U38, which reads a predefined bit file from the SD card and configures the FPGA in 8-bit SelectMAP configuration mode. See FPGA CONFIG Menu.

The JTAG chain of the KCU1250 board is shown in Figure 1-8. By default, only the UltraScale FPGA is part of the chain (J6 jumper uninstalled). Installing the J6 jumper enables an 8-bit bus transceiver (U69, SN74AVC8T245) and adds the FMC interfaces to the chain.

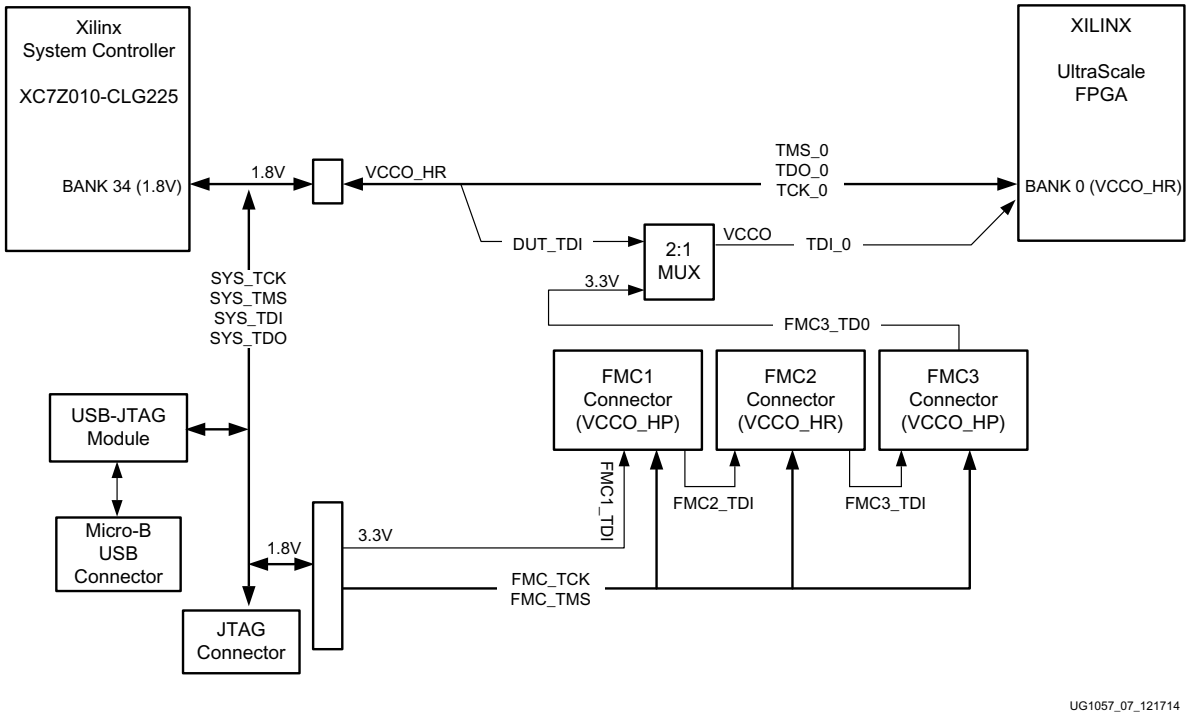

Figure 1-8: **JTAG Chain**

PROGRAM Pushbutton

Pressing the PROGRAM pushbutton SW7 (callout 14, Figure 1-2) asserts the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS17 (callout 12, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS17 lights up indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS3 (callout 13, Figure 1-2) indicates the FPGA initialization status. During FPGA initialization, the INIT LED illuminates RED. When FPGA initialization has completed, the LED illuminates GREEN.

System Controller

The KCU1250 board utilizes a Xilinx XC7Z010-CLG225 Zynq-7000 AP SoC U38 (callout 33, Figure D-1) system controller that can be used to:

- Configure the FPGA using predefined selection of configuration bit files on an SD card using 8-bit SelectMAP configuration
- Select the output frequencies of the SuperClock-2 module
- Monitor the onboard power system (PMBus)

See Appendix D, System Controller for information on the system controller menu options.

System Controller Reset

The SYS_POR pushbutton SW4 (callout 9, Figure 1-2) asserts the active-Low system controller Power-On Reset (SYS_POR). When SYS_POR is reasserted, the system controller is reconfigured using the controller design stored on an attached SPI flash.

System Controller Status LEDs

DS1, DS12, DS16, and DS27 (callout 35, Figure 1-2) show the system controller INIT_B, DONE, STATUS, and ERROR status, respectively.

System Controller Configuration DIP Switches

The DIP switch SW13 (callout 8, Figure 1-2) shown in Figure 1-9 selects the address of the UltraScale FPGA configuration bitstream to be loaded from the SD card. The switch ON position is indicated by the arrow next to bit 1 of the switch.

The ENABLE bit (switch position 1) is used to enable the SD card configuration mode.

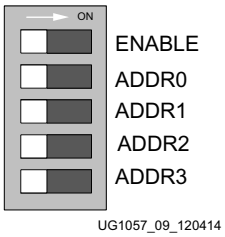

Figure 1-9: **Configuration DIP Switch (SW13)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW13 DIP Switch Configuration**

Configuration Bitstream Address	ADDR3	ADDR2	ADDR1	ADDR0
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON

System Controller GPIO Pushbuttons

SW5, SW6, SW10, SW11, SW12 (callout 36, Figure 1-2) are active-High pushbuttons connected to GPIO pins on the system controller. See GPIO Data Menu for more details.

USB to Dual-UART Bridge

The KCU1250 board uses a single-chip USB to dual-UART bridge (U32, Silicon Laboratories CP2105) for simultaneous serial communication between a host terminal and the UltraScale FPGA, and between a host terminal and the Zynq-7000 AP SoC system controller. The onboard micro-B receptacle USB connector J1 (callout 22, Figure 1-2) is connected to the dual-UART bridge.

The FPGA connects through a serial communication terminal connection (115200-8-N-1) using the standard communication port of the Silicon Labs USB to dual-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to send (RTS)
- Clear to send (CTS)

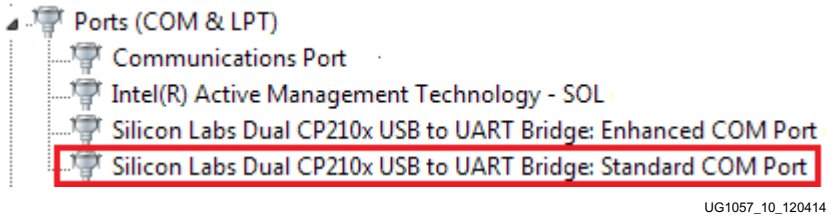

Figure 1-10: **Silicon Labs USB to UART Bridge Standard COM Port**

The dual-UART interface connections are split between two components:

- UART1 SCI (standard) interface is connected to the XCKU040 FPGA
- UART2 ECI (enhanced) interface is connected to the XC7Z010 system controller

Silicon Labs provides royalty-free virtual COM port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART bridge to appear as a pair of COM ports to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer.

IMPORTANT: *The VCP device drivers must be installed on the host PC prior to establishing communications with the KCU1250 board.*

The driver assigns the higher PC COM port number to UART1 (SCI) and the lower PC COM port number to UART(ECI).

The connections of these signals between the FPGA and the Silicon Labs CP2105 are listed in Table 1-7.

Table 1-7: **FPGA to UART Connection**

FPGA(U1)				Schematic Net Name	Device(U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
D14	RTS	Output	LVCMOS18	UART_CTS_I_B	18	CTS	Input
C14	CTS	Input	LVCMOS18	UART_RTS_O_B	19	RTS	Output
A14	TX	Output	LVCMOS18	UART_RXD_I	20	RXD	Input
B14	RX	Input	LVCMOS18	UART_TXD_O	21	TXD	Output

The bridge device also provides as many as four GPIO signals that you can define for status and control information (Table 1-8).

Table 1-8: **CP2105 USB to Dual-UART Bridge User GPIO**

FPGA(U1)				Schematic Net Name	Device(U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
F14	SelectIO™	In/Out	LVCMOS18	UART_GPIO_0	24	GPIO	In/Out
G14	SelectIO	In/Out	LVCMOS18	UART_GPIO_1	23	GPIO	In/Out
J14	SelectIO	In/Out	LVCMOS18	UART_GPIO_2	22	GPIO	In/Out
J15	SelectIO	In/Out	LVCMOS18	UART_GPIO_3	15	GPIO	In/Out

The second port of the CP2105 USB to dual-UART is connected to the onboard system controller. See Appendix D, System Controller.

300 MHz LVDS Oscillator

The KCU1250 board has one 300 MHz LVDS oscillator U42 (callout 11, Figure 1-2) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-9 lists the FPGA pin connections to the LVDS oscillator.

Table 1-9: **10 LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (42)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
E18	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	300 MHz LVDS oscillator	Output
E17	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	300 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

The KCU1250 board provides two pairs of differential SMA transceiver clock inputs (callout 32, Figure 1-2) that can be used for connecting to an external clock source. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-10.

Table 1-10: **Differential SMA Clock Connections**

FPGA(U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
G10	USER CLOCK_1_P	Input	LVDS	CLK_DIFF_1_P	J84
F10	USER CLOCK_1_N	Input	LVDS	CLK_DIFF_1_N	J85
G9	USER CLOCK_2_P	Input	LVDS	CLK_DIFF_2_P	J83
F9	USER CLOCK_2_N	Input	LVDS	CLK_DIFF_2_N	J86

SuperClock-2 Module

The SuperClock-2 module (callout 10, Figure 1-2) connects to the clock module interface connector (J36) and provides a programmable, low-noise and low-jitter clock source for the KCU1250 board (see *SuperClock-2 Module User Guide* (UG770) [Ref 4]). The clock module maps to FPGA I/O by way of 14 control pins, 2 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-11 shows the FPGA I/O mapping for the SuperClock-2 module interface. The KCU1250 board supplies UTIL_5V0, UTIL_3V3, UTIL_2V5, and V_{CCO_HP} input power to the clock module interface.

Table 1-11: **SuperClock-2 FPGA I/O Mapping**

FPGA(U1)				Schematic Net Name	J36 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
U34	Clock recovery	Input	LVDS	CM_LVDS1_P	1	Clock recovery	Output
V34	Clock recovery	Input	LVDS	CM_LVDS1_N	3	Clock recovery	Output
J8	Clock recovery	Input	LVDS	CM_LVDS2_P	9	Clock recovery	Output
H8	Clock recovery	Input	LVDS	CM_LVDS2_N	11	Clock recovery	Output
AK22	Regional clock	Input	LVDS	CM_GCLK_P	25	Global clock	Output
AK23	Regional clock	Input	LVDS	CM_GCLK_N	27	Global clock	Output
AN23	Control I/O	Output	LVCMOS18	CM_H_DEC	67	DEC	Input
AP23	Control I/O	Output	LVCMOS18	CM_H_INC	69	INC	Input
AP24	Control I/O	Output	LVCMOS18	CM_FS_ALIGN	71	ALIGN	Input
AP25	Control I/O	Input	LVCMOS18	CM_H_LOL	79	LOL	Output

Table 1-11: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA(U1)				Schematic Net Name	J36 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AP20	Control I/O	Output	LVCMOS18	CM_H_INT_ALRM	81	INT_ALRM	Input
AP21	Control I/O	Output	LVCMOS18	CM_C1B	83	C1B	Input
AM24	Control I/O	Output	LVCMOS18	CM_C2B	85	C2B	Input
AN24	Control I/O	Output	LVCMOS18	CM_C3B	87	C3B	Input
AM22	Control I/O	Output	LVCMOS18	CM_C1A	89	C1A	Input
AN22	Control I/O	Output	LVCMOS18	CM_C2A	91	C2A	Input
AM21	Control I/O	Output	LVCMOS18	CM_H_CS0_C3A	95	CS0_C3A	Input
AN21	Control I/O	Output	LVCMOS18	CM_H_CS1_C4A	97	CS1_C4A	Input
AL24	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active-High)

DS19 through DS26 (callout 24, Figure 1-2) are eight active-High LEDs that are connected to user I/O pins on the FPGA, as shown in Table 1-12. These LEDs can be used to indicate status (or other functions).

Table 1-12: **User LEDs**

FPGA(U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
D18	User LED	Output	LVCMOS18	APP_LED1	DS19
D19	User LED	Output	LVCMOS18	APP_LED2	DS20
C18	User LED	Output	LVCMOS18	APP_LED3	DS21
C19	User LED	Output	LVCMOS18	APP_LED4	DS25
B19	User LED	Output	LVCMOS18	APP_LED5	DS24
D18	User LED	Output	LVCMOS18	APP_LED6	DS23
D19	User LED	Output	LVCMOS18	APP_LED7	DS22
C18	User LED	Output	LVCMOS18	APP_LED8	DS26

User DIP Switches (Active-High) and I/O Header

The DIP switch SW3 (callout 26, Figure 1-2) provides a set of eight active-High switches which connect to user I/O pins on the FPGA, as shown in Table 1-13. These pins can be used to set control pins or any other purpose you choose. The eight I/Os also map to a test header J95 (callout 29, Figure 1-2), providing external access for these pins. The I/O pins can be connected to the onboard system controller as additional GPIO between the two devices.

IMPORTANT: *Install J7 to connect the user DIP switches to the system controller.*

Table 1-13: **User DIP Switches**

FPGA(U1)				Schematic Net Name	DIP Switch Reference Designator	J95 Test Header Pin	Device(U38) Pin
Pin	Function	Direction	IOSTANDARD				
J19	User switch	Input	LVCMOS18	USER_SW1	SW3	1	F12
J14	User switch	Input	LVCMOS18	USER_SW2		3	E13
G19	User switch	Input	LVCMOS18	USER_SW3		5	E11
F19	User switch	Input	LVCMOS18	USER_SW4		7	E12
J18	User switch	Input	LVCMOS18	USER_SW5		9	F13
H18	User switch	Input	LVCMOS18	USER_SW6		11	F14
F18	User switch	Input	LVCMOS18	USER_SW7		13	G15
F19	User switch	Input	LVCMOS18	USER_SW8		15	F15

Figure 1-11 shows the user I/O connector J28 (callout 28, Figure 1-2).

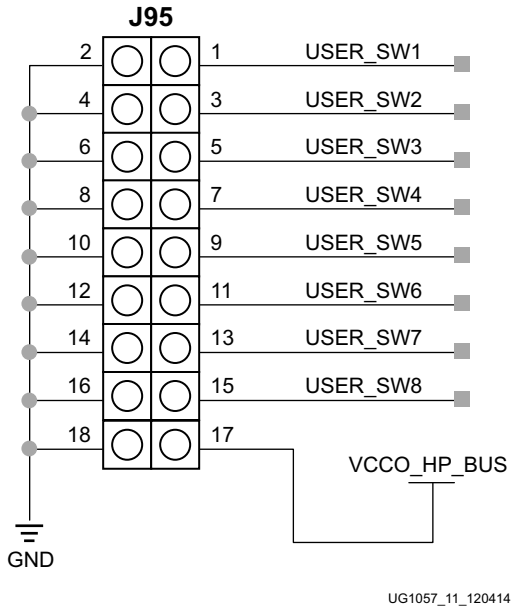

Figure 1-11: **User I/O (J95)**

User Push Buttons (Active-High)

SW8 and SW9 (callout 25, Figure 1-2) are active-High user push buttons that are connected to user I/O pins on the FPGA, as shown in Table 1-14. These switches can be used for any function.

Table 1-14: **User Push Buttons**

FPGA(U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
L15	User push button	Input	LVCMOS18	USER_PB1	SW9
L18	User push button	Input	LVCMOS18	USER_PB2	SW8

MGT Transceivers and Reference Clocks

The KCU1250 board provides access to all GTH transceiver and reference clock pins of the XCKU040 FPGA, as shown in Figure 1-12. The MGT transceivers are grouped into five sets of four RX-TX lanes, referred to as a quad (Q224 - Q228).

IMPORTANT: *Figure 1-12 is for reference only and might not reflect the current revision of the board. QUAD 131 and QUAD 132 are not available on the XCKU040 FPGA.*

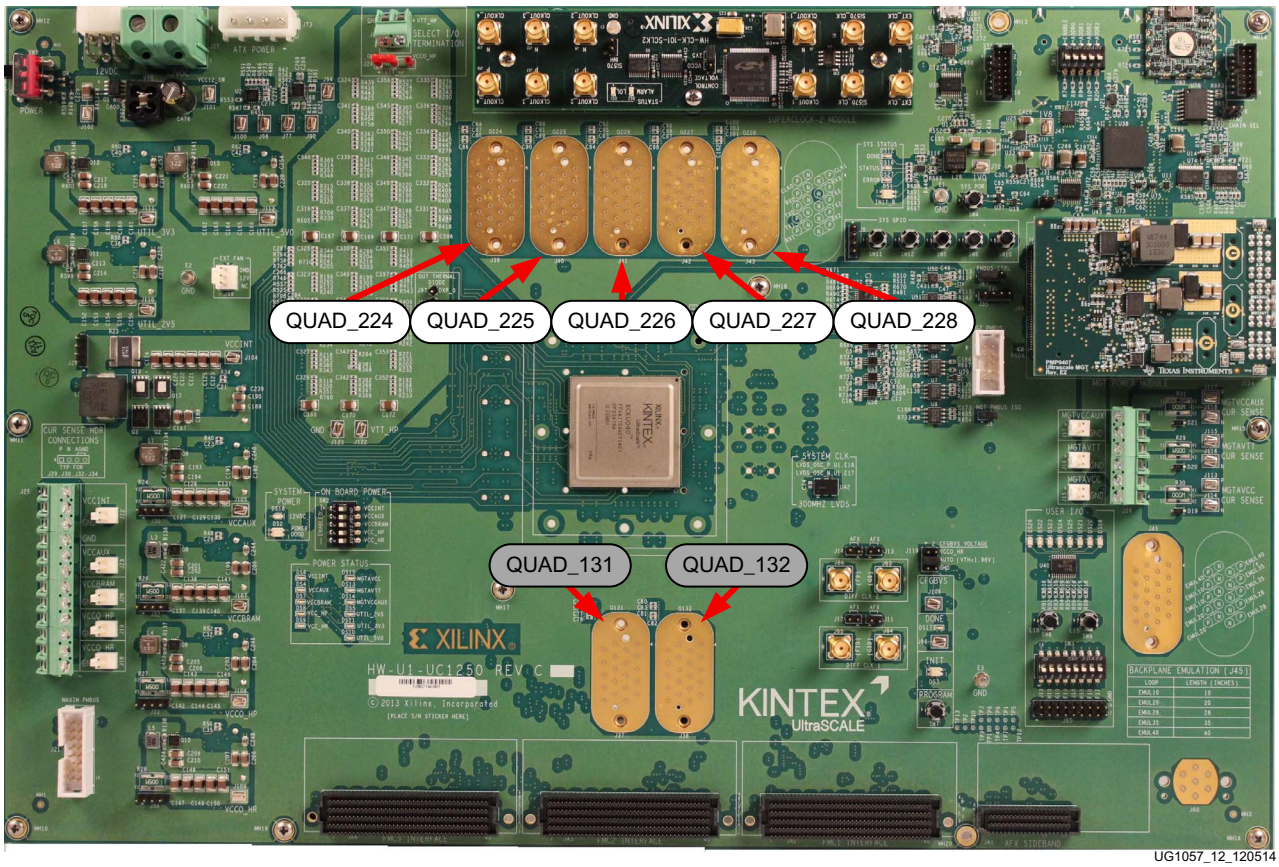

Figure 1-12: **MGT Quad Locations**

Each MGT quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad, which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc., for information about this or other cable assemblies [Ref 6]. Figure 1-13 shows the connector pad and the connector pinout.

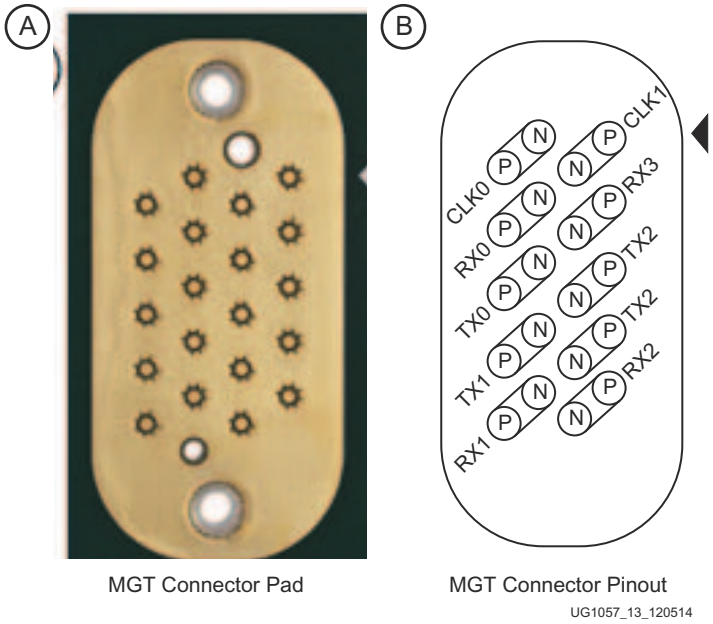

Figure 1-13: **A - MGT Connector Pad, B - MGT Connector Pinout**

The information for each GTH transceiver pin is shown in Table 1-15.

Table 1-15: **GTH Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
R34	131_RX0_N	131	J37	2498.1
R33	131_RX0_P	131	J37	2497.3
N34	131_RX1_N	131	J37	3042.2
N33	131_RX1_P	131	J37	3038.9
L34	131_RX2_N	131	J37	2931.2
L33	131_RX2_P	131	J37	2932.0
J34	131_RX3_N	131	J37	2522.8
J33	131_RX3_P	131	J37	2523.6
T32	131_TX0_N	131	J37	2748.3
T31	131_TX0_P	131	J37	2747.2
P32	131_TX1_N	131	J37	3002.0
P31	131_TX1_P	131	J37	3001.0
M32	131_TX2_N	131	J37	3060.4

Table 1-15: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
M31	131_TX2_P	131	J37	3061.0
K32	131_TX3_N	131	J37	2769.0
K31	131_TX3_P	131	J37	2769.6
G34	132_RX0_N	132	J38	2443.3
G33	132_RX0_P	132	J38	2442.5
F32	132_RX1_N	132	J38	3183.3
F31	132_RX1_P	132	J38	3182.3
E34	132_RX2_N	132	J38	3030.5
E33	132_RX2_P	132	J38	3031.3
C34	132_RX3_N	132	J38	2490.9
C33	132_RX3_P	132	J38	2491.8
H32	132_TX0_N	132	J38	2753.0
H31	132_TX0_P	132	J38	2752.0
G30	132_TX1_N	132	J38	2944.2
G29	132_TX1_P	132	J38	2943.4
D32	132_TX2_N	132	J38	2970.0
D31	132_TX2_P	132	J38	2970.6
B32	132_TX3_N	132	J38	2746.8
B31	132_TX3_P	132	J38	2748.8
AP1	224_RX0_N	224	J39	3318.6
AP2	224_RX0_P	224	J39	3319.3
AM1	224_RX1_N	224	J39	2711.7
AM2	224_RX1_P	224	J39	2712.8
AK1	224_RX2_N	224	J39	2574.3
AK2	224_RX2_P	224	J39	2573.3
AJ3	224_RX3_N	224	J39	3199.6
AJ4	224_RX3_P	224	J39	3198.6
AN3	224_TX0_N	224	J39	3059.2
AN4	224_TX0_P	224	J39	3059.5
AM5	224_TX1_N	224	J39	3084.4
AM6	224_TX1_P	224	J39	3085.5
AL3	224_TX2_N	224	J39	2836.1
AL4	224_TX2_P	224	J39	2835.6
AK5	224_TX3_N	224	J39	3103.1
AK6	224_TX3_P	224	J39	3102.7

Table 1-15: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AH1	225_RX0_N	225	J40	3027.1
AH2	225_RX0_P	225	J40	3027.7
AF1	225_RX1_N	225	J40	2419.3
AF2	225_RX1_P	225	J40	2419.9
AD1	225_RX2_N	225	J40	2340.7
AD2	225_RX2_P	225	J40	2339.8
AB1	225_RX3_N	225	J40	2889.8
AB2	225_RX3_P	225	J40	2888.8
AH5	225_TX0_N	225	J40	2917.7
AH6	225_TX0_P	225	J40	2918.9
AG3	225_TX1_N	225	J40	2668.2
AG4	225_TX1_P	225	J40	2668.8
AE3	225_TX2_N	225	J40	2589.1
AE4	225_TX2_P	225	J40	2588.2
AC3	225_TX3_N	225	J40	2829.1
AC4	225_TX3_P	225	J40	2828.1
Y1	226_RX0_N	226	J41	2715.2
Y2	226_RX0_P	226	J41	2715.8
V1	226_RX1_N	226	J41	2218.3
V2	226_RX1_P	226	J41	2218.7
T1	226_RX2_N	226	J41	2167.7
T2	226_RX2_P	226	J41	2167.6
P1	226_RX3_N	226	J41	2794.5
P2	226_RX3_P	226	J41	2793.8
AA3	226_TX0_N	226	J41	2763.0
AA4	226_TX0_P	226	J41	2763.7
W3	226_TX1_N	226	J41	2467.3
W4	226_TX1_P	226	J41	2467.4
U3	226_TX2_N	226	J41	2478.3
U4	226_TX2_P	226	J41	2476.6
R3	226_TX3_N	226	J41	2578.4
R4	226_TX3_P	226	J41	2577.4
M1	227_RX0_N	227	J42	2833.4
M2	227_RX0_P	227	J42	2834.0
K1	227_RX1_N	227	J42	2287.8

Table 1-15: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
K2	227_RX1_P	227	J42	2288.5
H1	227_RX2_N	227	J42	2368.0
H2	227_RX2_P	227	J42	2367.0
F1	227_RX3_N	227	J42	2995.4
F2	227_RX3_P	227	J42	2994.4
N3	227_TX0_N	227	J42	2802.3
N4	227_TX0_P	227	J42	2803.0
L3	227_TX1_N	227	J42	2568.8
L4	227_TX1_P	227	J42	2569.5
J3	227_TX2_N	227	J42	2649.5
J4	227_TX2_P	227	J42	2648.5
G3	227_TX3_N	227	J42	2940.4
G4	227_TX3_P	227	J42	2939.5
E3	228_RX0_N	228	J43	3117.4
E4	228_RX0_P	228	J43	3118.0
D1	228_RX1_N	228	J43	2521.3
D2	228_RX1_P	228	J43	2522.0
B1	228_RX2_N	228	J43	2601.5
B2	228_RX2_P	228	J43	2600.5
A3	228_RX3_N	228	J43	3376.9
A4	228_RX3_P	228	J43	3376.8
F5	228_TX0_N	228	J43	3125.1
F6	228_TX0_P	228	J43	3126.3
D5	228_TX1_N	228	J43	2892.8
D6	228_TX1_P	228	J43	2893.9
C3	228_TX2_N	228	J43	2883.0
C4	228_TX2_P	228	J43	2882.1
B5	228_TX3_N	228	J43	3340.9
B6	228_TX3_P	228	J43	3341.5

The information for each GTH transceiver clock input is shown in Table 1-16.

Table 1-16: **GTH Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
R30	131_REFCLK0_N	224	J37
R29	131_REFCLK0_P	224	J37
N30	131_REFCLK1_N	224	J37
N29	131_REFCLK1_P	224	J37
L30	132_REFCLK0_N	225	J38
L29	132_REFCLK0_P	225	J38
J30	132_REFCLK1_N	225	J38
J29	132_REFCLK1_P	225	J38
AF5	224_REFCLK0_N	226	J39
AF6	224_REFCLK0_P	226	J39
AD5	224_REFCLK1_N	226	J39
AD6	224_REFCLK1_P	226	J39
AB5	225_REFCLK0_N	227	J40
AB6	225_REFCLK0_P	227	J40
Y5	225_REFCLK1_N	227	J40
Y6	225_REFCLK1_P	227	J40
V5	226_REFCLK0_N	228	J41
V6	226_REFCLK0_P	228	J41
T5	226_REFCLK1_N	228	J41
T6	226_REFCLK1_P	228	J41
P5	227_REFCLK0_N	229	J42
P6	227_REFCLK0_P	229	J42
M5	227_REFCLK1_N	229	J42
M6	227_REFCLK1_P	229	J42
K5	228_REFCLK0_N	230	J43
K6	228_REFCLK0_P	230	J43
H5	228_REFCLK1_N	230	J43
H6	228_REFCLK1_P	230	J43

FPGA Mezzanine Card HPC Interface

The KCU1250 board features three high pin count (HPC) connectors as defined by the VITA 57.1 FMC specification (callout 28, 29 and 30, Figure 1-2). The FMC HPC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates.

The FMC1 HPC connector JA2 provides connectivity for:

- 43 differential user defined pairs:
  - 34 LA pairs
  - 9 HA pairs
- 4 differential clocks

The FMC2 HPC connector JA3 provides connectivity for:

- 44 differential user defined pairs:
  - 34 LA pairs
  - 10 HA pairs
- 2 differential clocks

The FMC 3 HPC connector JA4 provides connectivity for:

- 45 differential user defined pairs:
  - 34 LA pairs
  - 11 HA pairs
- 2 differential clocks

IMPORTANT: *The VADJ voltage on the FMC HPC connectors tracks V_{CCO_HP}*

The FMC HPC connectors on the KCU1250 board are identified as FMC1 at JA2, FMC2 at JA3, and FMC3 at JA4. The connections for each of these connectors are listed in Table 1-17, Table 1-18 and Table 1-19, respectively.

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
H12	FMC1_CLK0_M2C_P	H4
G12	FMC1_CLK0_M2C_N	H5
E22	FMC1_CLK1_M2C_P	G2
E23	FMC1_CLK1_M2C_N	G3
G10	FMC1_CLK2_BIDIR_P	K4
F10	FMC1_CLK2_BIDIR_N	K5
G9	FMC1_CLK3_BIDIR_P	J2
F9	FMC1_CLK3_BIDIR_N	J3
D24	FMC1_HA00_CC_P	F4
C24	FMC1_HA00_CC_N	F5
E25	FMC1_HA01_CC_P	E2
D25	FMC1_HA01_CC_N	E3
D8	FMC1_HA02P	K7
C8	FMC1_HA02N	K8
B9	FMC1_HA03P	J6
A9	FMC1_HA03N	J7
F8	FMC1_HA04P	F7
E8	FMC1_HA04N	F8
B29	FMC1_HA05P	E6
A29	FMC1_HA05N	E7
E28	FMC1_HA06P	K10
D29	FMC1_HA06N	K11
C27	FMC1_HA07P	J9
B27	FMC1_HA07N	J10
F27	FMC1_HA08P	F10
E27	FMC1_HA08N	F11
H11	FMC1_LA00_CC_P	G6
G11	FMC1_LA00_CC_N	G7
D13	FMC1_LA01_CC_P	D8
C13	FMC1_LA01_CC_N	D9
A13	FMC1_LA02P	H7
A12	FMC1_LA02N	H8

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
F13	FMC1_LA03P	G9
E13	FMC1_LA03N	G10
C11	FMC1_LA04P	H10
B11	FMC1_LA04N	H11
C12	FMC1_LA05P	D11
B12	FMC1_LA05N	D12
E11	FMC1_LA06P	C10
D11	FMC1_LA06N	C11
J13	FMC1_LA07P	H13
H13	FMC1_LA07N	H14
L12	FMC1_LA08P	G12
K12	FMC1_LA08N	G13
L13	FMC1_LA09P	D14
K13	FMC1_LA09N	D15
K11	FMC1_LA10P	C14
J11	FMC1_LA10N	C15
K10	FMC1_LA11P	H16
J10	FMC1_LA11N	H17
J9	FMC1_LA12P	G15
H9	FMC1_LA12N	G16
L8	FMC1_LA13P	D17
K8	FMC1_LA13N	D18
E10	FMC1_LA14P	C18
D10	FMC1_LA14N	C19
D9	FMC1_LA15P	H19
C9	FMC1_LA15N	H20
B10	FMC1_LA16P	G18
A10	FMC1_LA16N	G19
D23	FMC1_LA17_CC_P	D20
C23	FMC1_LA17_CC_N	D21
H21	FMC1_LA18_CC_P	C22
G21	FMC1_LA18_CC_N	C23
G22	FMC1_LA19P	H22
F22	FMC1_LA19N	H23
G20	FMC1_LA20P	G21

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
F20	FMC1_LA20N	G22
F24	FMC1_LA21P	H25
F23	FMC1_LA21N	H26
E21	FMC1_LA22P	G24
E20	FMC1_LA22N	G25
G24	FMC1_LA23P	D23
F25	FMC1_LA23N	D24
D21	FMC1_LA24P	H28
D20	FMC1_LA24N	H29
B20	FMC1_LA25P	G27
A20	FMC1_LA25N	G28
C22	FMC1_LA26P	D26
C21	FMC1_LA26N	D27
B22	FMC1_LA27P	C26
B21	FMC1_LA27N	C27
B24	FMC1_LA28P	H31
A24	FMC1_LA28N	H32
C26	FMC1_LA29P	G30
B26	FMC1_LA29N	G31
B25	FMC1_LA30P	H34
A25	FMC1_LA30N	H35
E26	FMC1_LA31P	G33
D26	FMC1_LA31N	G34
A27	FMC1_LA32P	H37
A28	FMC1_LA32N	H38
D28	FMC1_LA33P	G36
C28	FMC1_LA33N	G37
E12	FMC1_PRSNT_M2C_L	H2

Table 1-18 shows the VITA 57.1 FMC2 HPC connections at JA3.

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
R13	FMC2_CLK0_M2C_P	H4
P13	FMC2_CLK0_M2C_N	H5
R11	FMC2_CLK1_M2C_P	G2
P11	FMC2_CLK1_M2C_N	G3
AU17	FMC2_HA00_CC_P	F4
AV17	FMC2_HA00_CC_N	F5
AV18	FMC2_HA01_CC_P	E2
AW18	FMC2_HA01_CC_N	E3
BC18	FMC2_HA02P	K7
BD18	FMC2_HA02N	K8
BD16	FMC2_HA03P	J6
BD15	FMC2_HA03N	J7
BC19	FMC2_HA04P	F7
BD19	FMC2_HA04N	F8
AN13	FMC2_HA05P	E6
AP13	FMC2_HA05N	E7
AP11	FMC2_HA06P	K10
AP10	FMC2_HA06N	K11
K26	FMC2_HA07P	J9
K27	FMC2_HA07N	J10
G25	FMC2_HA08P	F10
G26	FMC2_HA08N	F11
H27	FMC2_HA09P	E9
G27	FMC2_HA09N	E10
AF10	FMC2_LA00_CC_P	G6
AG10	FMC2_LA00_CC_N	G7
AG11	FMC2_LA01_CC_P	D8
AH11	FMC2_LA01_CC_N	D9
AK8	FMC2_LA02P	H7
AL8	FMC2_LA02N	H8
AJ9	FMC2_LA03P	G9
AJ8	FMC2_LA03N	G10
AN8	FMC2_LA04P	H10

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
AP8	FMC2_LA04N	H11
AK10	FMC2_LA05P	D11
AL9	FMC2_LA05N	D12
AN9	FMC2_LA06P	C10
AP9	FMC2_LA06N	C11
AL10	FMC2_LA07P	H13
AM10	FMC2_LA07N	H14
AH9	FMC2_LA08P	G12
AH8	FMC2_LA08N	G13
AD9	FMC2_LA09P	D14
AD8	FMC2_LA09N	D15
AD10	FMC2_LA10P	C14
AE10	FMC2_LA10N	C15
AE8	FMC2_LA11P	H16
AF8	FMC2_LA11N	H17
AD11	FMC2_LA12P	G15
AE11	FMC2_LA12N	G16
AE12	FMC2_LA13P	D17
AF12	FMC2_LA13N	D18
AH13	FMC2_LA14P	C18
AJ13	FMC2_LA14N	C19
AE13	FMC2_LA15P	H19
AF13	FMC2_LA15N	H20
AK13	FMC2_LA16P	G18
AL13	FMC2_LA16N	G19
N24	FMC2_LA17_CC_P	D20
M24	FMC2_LA17_CC_N	D21
M25	FMC2_LA18_CC_P	C22
M26	FMC2_LA18_CC_N	C23
K20	FMC2_LA19P	H22
K21	FMC2_LA19N	H23
N21	FMC2_LA20P	G21
M21	FMC2_LA20N	G22
P20	FMC2_LA21P	H25
P21	FMC2_LA21N	H26

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
N22	FMC2_LA22P	G24
M22	FMC2_LA22N	G25
R23	FMC2_LA23P	D23
P23	FMC2_LA23N	D24
R25	FMC2_LA24P	H28
R26	FMC2_LA24N	H29
T24	FMC2_LA25P	G27
T25	FMC2_LA25N	G28
T27	FMC2_LA26P	D26
R27	FMC2_LA26N	D27
L22	FMC2_LA27P	C26
K23	FMC2_LA27N	C27
L25	FMC2_LA28P	H31
K25	FMC2_LA28N	H32
L23	FMC2_LA29P	G30
L24	FMC2_LA29N	G31
M27	FMC2_LA30P	H34
L27	FMC2_LA30N	H35
J23	FMC2_LA31P	G33
H24	FMC2_LA31N	G34
J26	FMC2_LA32P	H37
H26	FMC2_LA32N	H38
J24	FMC2_LA32P	G36
J25	FMC2_LA33N	G37
AM9	FMC2_PRSNT_M2C_L	H2

Table 1-19 shows the VITA 57.1 FMC3 HPC connections at JA4.

Table 1-19: **VITA 57.1 FMC3 HPC Connections at JA4**

U1 FPGA Pin	Net Name	FMC Pin
W25	FMC3_CLK0_M2C_P	H4
Y25	FMC3_CLK0_M2C_N	H5
AB30	FMC3_CLK1_M2C_P	G2
AB31	FMC3_CLK1_M2C_N	G3
Y23	FMC3_HA00_CC_P	F4
AA23	FMC3_HA00_CC_N	F5
AC31	FMC3_HA01_CC_P	E2
AC32	FMC3_HA01_CC_N	E3
AA27	FMC3_HA02P	K7
AB27	FMC3_HA02N	K8
AC26	FMC3_HA03P	J6
AC27	FMC3_HA03N	J7
AB24	FMC3_HA04P	F7
AC24	FMC3_HA04N	F8
AD25	FMC3_HA05P	E6
AD26	FMC3_HA05N	E7
Y26	FMC3_HA06P	K10
Y27	FMC3_HA06N	K11
AF29	FMC3_HA07P	J9
AG29	FMC3_HA07N	J10
AC28	FMC3_HA08P	F10
AD28	FMC3_HA08N	F11
AE28	FMC3_HA09P	E9
AF28	FMC3_HA09N	E10
AE27	FMC3_HA10P	K13
AF27	FMC3_HA10N	K14
W23	FMC3_LA00_CC_P	G6
W24	FMC3_LA00_CC_N	G7
AA24	FMC3_LA01_CC_P	D8
AA25	FMC3_LA01_CC_N	D9
V26	FMC3_LA02P	H7
W26	FMC3_LA02N	H8
V29	FMC3_LA03P	G9

Table 1-19: **VITA 57.1 FMC3 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
W29	FMC3_LA03N	G10
U26	FMC3_LA04P	H10
U27	FMC3_LA04N	H11
W28	FMC3_LA05P	D11
Y28	FMC3_LA05N	D12
U24	FMC3_LA06P	C10
U25	FMC3_LA06N	C11
V27	FMC3_LA07P	H13
V28	FMC3_LA07N	H14
V21	FMC3_LA08P	G12
W21	FMC3_LA08N	G13
T22	FMC3_LA09P	D14
T23	FMC3_LA09N	D15
V22	FMC3_LA10P	C14
V23	FMC3_LA10N	C15
U21	FMC3_LA11P	H16
U22	FMC3_LA11N	H17
AB21	FMC3_LA12P	G15
AC21	FMC3_LA12N	G16
AA20	FMC3_LA13P	D17
AB20	FMC3_LA13N	D18
AC22	FMC3_LA14P	C18
AC23	FMC3_LA14N	C19
AA22	FMC3_LA15P	H19
AB22	FMC3_LA15N	H20
AB25	FMC3_LA16P	G18
AB26	FMC3_LA16N	G19
AA32	FMC3_LA17_CC_P	D20
AB32	FMC3_LA17_CC_N	D21
AD30	FMC3_LA18_CC_P	C22
AD31	FMC3_LA18_CC_N	C23
V31	FMC3_LA19P	H22
W31	FMC3_LA19N	H23
Y31	FMC3_LA20P	G21
Y32	FMC3_LA20N	G22

Table 1-19: **VITA 57.1 FMC3 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
V33	FMC3_LA21P	H25
W34	FMC3_LA21N	H26
W30	FMC3_LA22P	G24
Y30	FMC3_LA22N	G25
W33	FMC3_LA23P	D23
Y33	FMC3_LA23N	D24
AC33	FMC3_LA24P	H28
AD33	FMC3_LA24N	H29
AA34	FMC3_LA25P	G27
AB34	FMC3_LA25N	G28
AA29	FMC3_LA26P	D26
AB29	FMC3_LA26N	D27
AC34	FMC3_LA27P	C26
AD34	FMC3_LA27N	C27
AE33	FMC3_LA28P	H31
AF34	FMC3_LA28N	H32
AE32	FMC3_LA29P	G30
AF32	FMC3_LA29N	G31
AF33	FMC3_LA30P	H34
AG34	FMC3_LA30N	H35
AG31	FMC3_LA31P	G33
AG32	FMC3_LA31N	G34
AF30	FMC3_LA32P	H37
AG30	FMC3_LA32N	H38
AD29	FMC3_LA33P	G36
AE30	FMC3_LA33N	G37
U29	FMC3_PRSNT_M2C_L	H2

System Monitor

The SYSMON monitors the physical environment using on-chip temperature and supply sensors, up to 17 external analog inputs, and an integrated analog-to-digital converter (ADC). The SYSMON is powered using the on-chip reference voltage (VREFP) shown in Figure 1-14. More information about the system monitor is available in *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 2].

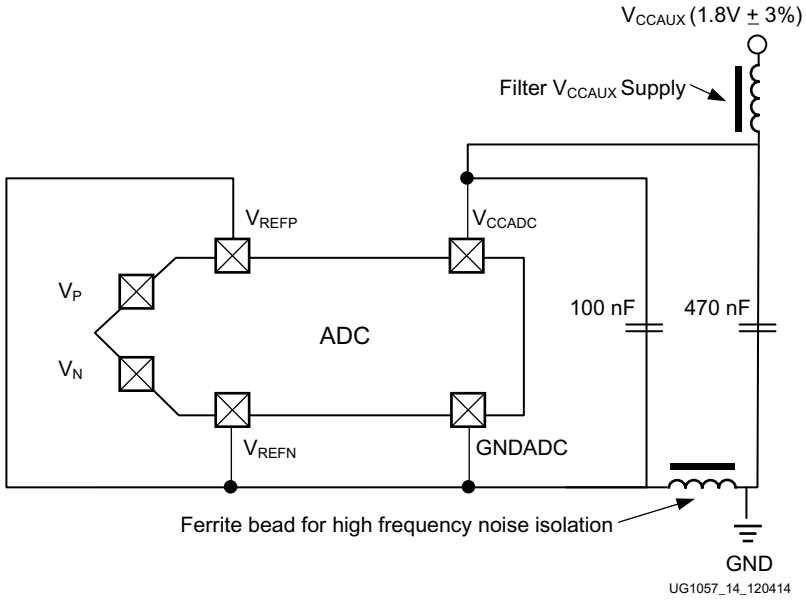

Figure 1-14: **SYSMON On-chip Reference**

I2C Bus Management

The I2C bus is routed through U22, an 8-channel I2C-bus multiplexer (NXP Semiconductor TCA9548). The I2C IDcode for the TCA9548 device is 0x75. The multiplexer provides I2C/PMBus communication between the bus master (system controller or FPGA) and six sub-systems:

- Onboard regulators and power monitoring
- SuperClock-2 module
- MGT power module
- FMC1
- FMC2
- FMC3

Table 1-20 shows the I2C channel assignments.

Table 1-20: **I2C Channel Assignments**

U22 Channel	I2C Component
0	System PMBus
1	SuperClock-2 module
2	MGT power module
3	FMC1
4	FMC2
5	FMC3

The upstream port of the TCA9548 multiplexer connects to PCA9306 (U46, U53, U55, and U58) dual bidirectional I2C and SMBus voltage-level translator and bus repeaters, with an enable (EN) signal (see Figure 1-15). J121 and J125 are used to enable or disable the bus repeaters and isolate the system controller or the UltraScale FPGA I2C bus.

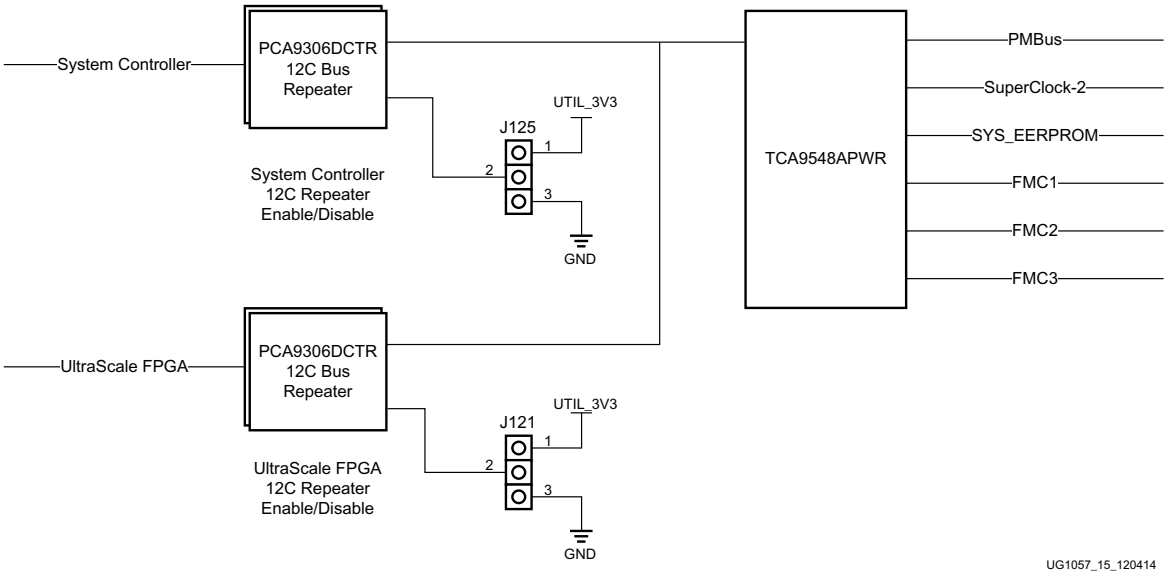

Figure 1-15: **I2C Bus Multiplexer and Upstream Repeater**

Default Jumper Settings

Introduction

Table A-1 lists the jumpers that must be installed on the KCU1250 board for proper operation. These jumpers must be installed except where specifically noted in this user guide.

IMPORTANT: *Any jumper not listed in Table A-1 should be left open for normal operation.*

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper/Dip-switch Position	Comments
SW2.1	V_{CCINT}	Lower left	OFF	
SW2.2	V_{CCBRAM}	Lower left	OFF	
SW2.3	V_{CCAUX}	Lower left	OFF	
SW2.4	V_{CCO_HP}	Lower left	OFF	
SW2.5	V_{CCO_HR}	Lower left	OFF	
J87	MGT PMBUS CTRL	Upper left	GND (2-3)	
J8	MGT PMBUS isolation	Center right	Installed	
J24	V_{TT_HP} source	Upper left	GND (1-2)	Red 20A jumper
J25	V_{TT_HR} source	Lower left	GND (1-2)	Red 20A jumper
J121	I2C_DUT	Center right	GND (2-3)	Disabled
J125	I2C_SYS	Center right	Pull-up (1-2)	Enabled

VITA 57.1 FMC Connector Pinouts

Introduction

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG1057_aB_01_121814

Figure B-1: **FMC Connector Pinouts**

Master Constraints File Listing

Introduction

The KCU1250 board master Xilinx design constraints (XDC) file template provides for designs targeting the KCU1250 UltraScale FPGA GTH transceiver characterization board. Net names in the listed constraints correlate with net names on the KCU1250 board schematic. Users must identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 3] for more information.

IMPORTANT: *See the UltraScale FPGA KCU1250 characterization kit website for the latest XDC file.*

KCU1250 Board XDC Listing

```
#FMC1
set_property PACKAGE_PIN E12       [get_ports "FMC1_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_PRSNT_M2C_L"]
set_property PACKAGE_PIN H12       [get_ports "FMC1_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK0_M2C_P"]
set_property PACKAGE_PIN G12       [get_ports "FMC1_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK0_M2C_N"]
set_property PACKAGE_PIN E22       [get_ports "FMC1_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK1_M2C_P"]
set_property PACKAGE_PIN E23       [get_ports "FMC1_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK1_M2C_N"]

#FMC1 LA
set_property PACKAGE_PIN H11       [get_ports "FMC1_LA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA00_CC_P"]
set_property PACKAGE_PIN G11       [get_ports "FMC1_LA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA00_CC_N"]
set_property PACKAGE_PIN D13       [get_ports "FMC1_LA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA01_CC_P"]
set_property PACKAGE_PIN C13       [get_ports "FMC1_LA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA01_CC_N"]
set_property PACKAGE_PIN A13       [get_ports "FMC1_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA02P"]
set_property PACKAGE_PIN A12       [get_ports "FMC1_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA02N"]
```

```
set_property PACKAGE_PIN F13      [get_ports "FMC1_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA03P"]
set_property PACKAGE_PIN E13      [get_ports "FMC1_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA03N"]
set_property PACKAGE_PIN C11      [get_ports "FMC1_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA04P"]
set_property PACKAGE_PIN B11      [get_ports "FMC1_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA04N"]
set_property PACKAGE_PIN C12      [get_ports "FMC1_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA05P"]
set_property PACKAGE_PIN B12      [get_ports "FMC1_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA05N"]
set_property PACKAGE_PIN E11      [get_ports "FMC1_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA06P"]
set_property PACKAGE_PIN D11      [get_ports "FMC1_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA06N"]
set_property PACKAGE_PIN J13      [get_ports "FMC1_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA07P"]
set_property PACKAGE_PIN H13      [get_ports "FMC1_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA07N"]
set_property PACKAGE_PIN L12      [get_ports "FMC1_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA08P"]
set_property PACKAGE_PIN K12      [get_ports "FMC1_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA08N"]
set_property PACKAGE_PIN L13      [get_ports "FMC1_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA09P"]
set_property PACKAGE_PIN K13      [get_ports "FMC1_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA09N"]
set_property PACKAGE_PIN K11      [get_ports "FMC1_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA10P"]
set_property PACKAGE_PIN J11      [get_ports "FMC1_LA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA10N"]
set_property PACKAGE_PIN K10      [get_ports "FMC1_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA11P"]
set_property PACKAGE_PIN J10      [get_ports "FMC1_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA11N"]
set_property PACKAGE_PIN J9       [get_ports "FMC1_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA12P"]
set_property PACKAGE_PIN H9       [get_ports "FMC1_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA12N"]
set_property PACKAGE_PIN L8       [get_ports "FMC1_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA13P"]
set_property PACKAGE_PIN K8       [get_ports "FMC1_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA13N"]
set_property PACKAGE_PIN E10      [get_ports "FMC1_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA14P"]
set_property PACKAGE_PIN D10      [get_ports "FMC1_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA14N"]
set_property PACKAGE_PIN D9       [get_ports "FMC1_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA15P"]
set_property PACKAGE_PIN C9       [get_ports "FMC1_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA15N"]
set_property PACKAGE_PIN B10      [get_ports "FMC1_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA16P"]
set_property PACKAGE_PIN A10      [get_ports "FMC1_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA16N"]
set_property PACKAGE_PIN D23      [get_ports "FMC1_LA17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA17_CC_P"]
set_property PACKAGE_PIN C23      [get_ports "FMC1_LA17_CC_N"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA17_CC_N"]
set_property PACKAGE_PIN H21      [get_ports "FMC1_LA18_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA18_CC_P"]
set_property PACKAGE_PIN G21      [get_ports "FMC1_LA18_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA18_CC_N"]
set_property PACKAGE_PIN G22      [get_ports "FMC1_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA19P"]
set_property PACKAGE_PIN F22      [get_ports "FMC1_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA19N"]
set_property PACKAGE_PIN G20      [get_ports "FMC1_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA20P"]
set_property PACKAGE_PIN F20      [get_ports "FMC1_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA20N"]
set_property PACKAGE_PIN F23      [get_ports "FMC1_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA21P"]
set_property PACKAGE_PIN F24      [get_ports "FMC1_LA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA21N"]
set_property PACKAGE_PIN E20      [get_ports "FMC1_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA22P"]
set_property PACKAGE_PIN E21      [get_ports "FMC1_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA22N"]
set_property PACKAGE_PIN G24      [get_ports "FMC1_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA23P"]
set_property PACKAGE_PIN F25      [get_ports "FMC1_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA23N"]
set_property PACKAGE_PIN D20      [get_ports "FMC1_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA24P"]
set_property PACKAGE_PIN D21      [get_ports "FMC1_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA24N"]
set_property PACKAGE_PIN B20      [get_ports "FMC1_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA25P"]
set_property PACKAGE_PIN A20      [get_ports "FMC1_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA25N"]
set_property PACKAGE_PIN C21      [get_ports "FMC1_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA26P"]
set_property PACKAGE_PIN C22      [get_ports "FMC1_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA26N"]
set_property PACKAGE_PIN B21      [get_ports "FMC1_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA27P"]
set_property PACKAGE_PIN B22      [get_ports "FMC1_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA27N"]
set_property PACKAGE_PIN B24      [get_ports "FMC1_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA28P"]
set_property PACKAGE_PIN A24      [get_ports "FMC1_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA28N"]
set_property PACKAGE_PIN C26      [get_ports "FMC1_LA29P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA29P"]
set_property PACKAGE_PIN B26      [get_ports "FMC1_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA29N"]
set_property PACKAGE_PIN B25      [get_ports "FMC1_LA30P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA30P"]
set_property PACKAGE_PIN A25      [get_ports "FMC1_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA30N"]
set_property PACKAGE_PIN E26      [get_ports "FMC1_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA31P"]
set_property PACKAGE_PIN D26      [get_ports "FMC1_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA31N"]
set_property PACKAGE_PIN A27      [get_ports "FMC1_LA32P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA32P"]
```

```
set_property PACKAGE_PIN A28      [get_ports "FMC1_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA32N"]
set_property PACKAGE_PIN D28      [get_ports "FMC1_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA33P"]
set_property PACKAGE_PIN C28      [get_ports "FMC1_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA33N"]

#FMC1 HA
set_property PACKAGE_PIN D24      [get_ports "FMC1_HA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA00_CC_P"]
set_property PACKAGE_PIN C24      [get_ports "FMC1_HA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA00_CC_N"]
set_property PACKAGE_PIN E25      [get_ports "FMC1_HA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA01_CC_P"]
set_property PACKAGE_PIN D25      [get_ports "FMC1_HA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA01_CC_N"]
set_property PACKAGE_PIN D8       [get_ports "FMC1_HA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA02P"]
set_property PACKAGE_PIN C8       [get_ports "FMC1_HA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA02N"]
set_property PACKAGE_PIN B9       [get_ports "FMC1_HA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA03P"]
set_property PACKAGE_PIN A9       [get_ports "FMC1_HA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA03N"]
set_property PACKAGE_PIN F8       [get_ports "FMC1_HA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA04P"]
set_property PACKAGE_PIN E8       [get_ports "FMC1_HA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA04N"]
set_property PACKAGE_PIN B29      [get_ports "FMC1_HA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA05P"]
set_property PACKAGE_PIN A29      [get_ports "FMC1_HA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA05N"]
set_property PACKAGE_PIN E28      [get_ports "FMC1_HA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA06P"]
set_property PACKAGE_PIN D29      [get_ports "FMC1_HA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA06N"]
set_property PACKAGE_PIN C27      [get_ports "FMC1_HA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA07P"]
set_property PACKAGE_PIN B27      [get_ports "FMC1_HA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA07N"]
set_property PACKAGE_PIN F27      [get_ports "FMC1_HA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA08P"]
set_property PACKAGE_PIN E27      [get_ports "FMC1_HA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA08N"]

#FMC2
set_property PACKAGE_PIN AM9      [get_ports "FMC2_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_PRSNT_M2C_L"]
set_property PACKAGE_PIN AF9      [get_ports "FMC2_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK0_M2C_P"]
set_property PACKAGE_PIN AG9      [get_ports "FMC2_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK0_M2C_N"]
set_property PACKAGE_PIN P24      [get_ports "FMC2_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK1_M2C_P"]
set_property PACKAGE_PIN P25      [get_ports "FMC2_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK1_M2C_N"]
```

```
#FMC2 LA
set_property PACKAGE_PIN AF10      [get_ports "FMC2_LA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA00_CC_P"]
set_property PACKAGE_PIN AG10      [get_ports "FMC2_LA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA00_CC_N"]
set_property PACKAGE_PIN AG11      [get_ports "FMC2_LA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA01_CC_P"]
set_property PACKAGE_PIN AH11      [get_ports "FMC2_LA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA01_CC_N"]
set_property PACKAGE_PIN AK8       [get_ports "FMC2_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA02P"]
set_property PACKAGE_PIN AL8       [get_ports "FMC2_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA02N"]
set_property PACKAGE_PIN AJ9       [get_ports "FMC2_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA03P"]
set_property PACKAGE_PIN AJ8       [get_ports "FMC2_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA03N"]
set_property PACKAGE_PIN AN8       [get_ports "FMC2_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA04P"]
set_property PACKAGE_PIN AP8       [get_ports "FMC2_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA04N"]
set_property PACKAGE_PIN AK10      [get_ports "FMC2_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA05P"]
set_property PACKAGE_PIN AL9       [get_ports "FMC2_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA05N"]
set_property PACKAGE_PIN AN9       [get_ports "FMC2_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA06P"]
set_property PACKAGE_PIN AP9       [get_ports "FMC2_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA06N"]
set_property PACKAGE_PIN AL10      [get_ports "FMC2_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA07P"]
set_property PACKAGE_PIN AM10      [get_ports "FMC2_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA07N"]
set_property PACKAGE_PIN AH9       [get_ports "FMC2_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA08P"]
set_property PACKAGE_PIN AH8       [get_ports "FMC2_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA08N"]
set_property PACKAGE_PIN AD9       [get_ports "FMC2_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA09P"]
set_property PACKAGE_PIN AD8       [get_ports "FMC2_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA09N"]
set_property PACKAGE_PIN AD10      [get_ports "FMC2_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA10P"]
set_property PACKAGE_PIN AE10      [get_ports "FMC2_LA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA10N"]
set_property PACKAGE_PIN AE8       [get_ports "FMC2_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA11P"]
set_property PACKAGE_PIN AF8       [get_ports "FMC2_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA11N"]
set_property PACKAGE_PIN AD11      [get_ports "FMC2_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA12P"]
set_property PACKAGE_PIN AE11      [get_ports "FMC2_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA12N"]
set_property PACKAGE_PIN AE12      [get_ports "FMC2_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA13P"]
set_property PACKAGE_PIN AF12      [get_ports "FMC2_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA13N"]
set_property PACKAGE_PIN AH13      [get_ports "FMC2_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA14P"]
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set_property PACKAGE_PIN AJ13     [get_ports "FMC2_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA14N"]
set_property PACKAGE_PIN AE13     [get_ports "FMC2_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA15P"]
set_property PACKAGE_PIN AF13     [get_ports "FMC2_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA15N"]
set_property PACKAGE_PIN AK13     [get_ports "FMC2_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA16P"]
set_property PACKAGE_PIN AL13     [get_ports "FMC2_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA16N"]
set_property PACKAGE_PIN N24      [get_ports "FMC2_LA17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA17_CC_P"]
set_property PACKAGE_PIN M24      [get_ports "FMC2_LA17_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA17_CC_N"]
set_property PACKAGE_PIN M25      [get_ports "FMC2_LA18_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA18_CC_P"]
set_property PACKAGE_PIN M26      [get_ports "FMC2_LA18_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA18_CC_N"]
set_property PACKAGE_PIN K20      [get_ports "FMC2_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA19P"]
set_property PACKAGE_PIN K21      [get_ports "FMC2_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA19N"]
set_property PACKAGE_PIN N21      [get_ports "FMC2_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA20P"]
set_property PACKAGE_PIN M21      [get_ports "FMC2_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA20N"]
set_property PACKAGE_PIN P20      [get_ports "FMC2_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA21P"]
set_property PACKAGE_PIN P21      [get_ports "FMC2_LA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA21N"]
set_property PACKAGE_PIN N22      [get_ports "FMC2_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA22P"]
set_property PACKAGE_PIN M22      [get_ports "FMC2_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA22N"]
set_property PACKAGE_PIN R23      [get_ports "FMC2_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA23P"]
set_property PACKAGE_PIN P23      [get_ports "FMC2_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA23N"]
set_property PACKAGE_PIN R25      [get_ports "FMC2_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA24P"]
set_property PACKAGE_PIN R26      [get_ports "FMC2_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA24N"]
set_property PACKAGE_PIN T24      [get_ports "FMC2_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA25P"]
set_property PACKAGE_PIN T25      [get_ports "FMC2_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA25N"]
set_property PACKAGE_PIN T27      [get_ports "FMC2_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA26P"]
set_property PACKAGE_PIN R27      [get_ports "FMC2_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA26N"]
set_property PACKAGE_PIN L22      [get_ports "FMC2_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA27P"]
set_property PACKAGE_PIN K23      [get_ports "FMC2_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA27N"]
set_property PACKAGE_PIN L25      [get_ports "FMC2_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA28P"]
set_property PACKAGE_PIN K25      [get_ports "FMC2_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA28N"]
set_property PACKAGE_PIN L23      [get_ports "FMC2_LA29P"]
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```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA29P"]
set_property PACKAGE_PIN L24      [get_ports "FMC2_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA29N"]
set_property PACKAGE_PIN M27      [get_ports "FMC2_LA30P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA30P"]
set_property PACKAGE_PIN L27      [get_ports "FMC2_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA30N"]
set_property PACKAGE_PIN J23      [get_ports "FMC2_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA31P"]
set_property PACKAGE_PIN H24      [get_ports "FMC2_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA31N"]
set_property PACKAGE_PIN J26      [get_ports "FMC2_LA32P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA32P"]
set_property PACKAGE_PIN H26      [get_ports "FMC2_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA32N"]
set_property PACKAGE_PIN J24      [get_ports "FMC2_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA33P"]
set_property PACKAGE_PIN J25      [get_ports "FMC2_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA33N"]

#FMC2 HA
set_property PACKAGE_PIN AG12     [get_ports "FMC2_HA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA00_CC_P"]
set_property PACKAGE_PIN AH12     [get_ports "FMC2_HA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA00_CC_N"]
set_property PACKAGE_PIN P26      [get_ports "FMC2_HA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA01_CC_P"]
set_property PACKAGE_PIN N26      [get_ports "FMC2_HA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA01_CC_N"]
set_property PACKAGE_PIN AK12     [get_ports "FMC2_HA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA02P"]
set_property PACKAGE_PIN AL12     [get_ports "FMC2_HA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA02N"]
set_property PACKAGE_PIN AM12     [get_ports "FMC2_HA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA03P"]
set_property PACKAGE_PIN AN12     [get_ports "FMC2_HA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA03N"]
set_property PACKAGE_PIN AM11     [get_ports "FMC2_HA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA04P"]
set_property PACKAGE_PIN AN11     [get_ports "FMC2_HA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA04N"]
set_property PACKAGE_PIN AN13     [get_ports "FMC2_HA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA05P"]
set_property PACKAGE_PIN AP13     [get_ports "FMC2_HA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA05N"]
set_property PACKAGE_PIN AP11     [get_ports "FMC2_HA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA06P"]
set_property PACKAGE_PIN AP10     [get_ports "FMC2_HA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA06N"]
set_property PACKAGE_PIN K26      [get_ports "FMC2_HA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA07P"]
set_property PACKAGE_PIN K27      [get_ports "FMC2_HA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA07N"]
set_property PACKAGE_PIN G25      [get_ports "FMC2_HA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA08P"]
set_property PACKAGE_PIN G26      [get_ports "FMC2_HA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA08N"]
set_property PACKAGE_PIN H27      [get_ports "FMC2_HA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA09P"]
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```
set_property PACKAGE_PIN G27      [get_ports "FMC2_HA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA09N"]

#FMC3
set_property PACKAGE_PIN U29      [get_ports "FMC3_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_PRSNT_M2C_L"]
set_property PACKAGE_PIN W25      [get_ports "FMC3_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK0_M2C_P"]
set_property PACKAGE_PIN Y25      [get_ports "FMC3_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK0_M2C_N"]
set_property PACKAGE_PIN AB30     [get_ports "FMC3_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK1_M2C_P"]
set_property PACKAGE_PIN AB31     [get_ports "FMC3_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK1_M2C_N"]

#FMC3 LA
set_property PACKAGE_PIN W23      [get_ports "FMC3_LA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA00_CC_P"]
set_property PACKAGE_PIN W24      [get_ports "FMC3_LA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA00_CC_N"]
set_property PACKAGE_PIN AA24     [get_ports "FMC3_LA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA01_CC_P"]
set_property PACKAGE_PIN AA25     [get_ports "FMC3_LA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA01_CC_N"]
set_property PACKAGE_PIN V26      [get_ports "FMC3_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA02P"]
set_property PACKAGE_PIN W26      [get_ports "FMC3_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA02N"]
set_property PACKAGE_PIN V29      [get_ports "FMC3_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA03P"]
set_property PACKAGE_PIN W29      [get_ports "FMC3_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA03N"]
set_property PACKAGE_PIN U26      [get_ports "FMC3_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA04P"]
set_property PACKAGE_PIN U27      [get_ports "FMC3_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA04N"]
set_property PACKAGE_PIN W28      [get_ports "FMC3_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA05P"]
set_property PACKAGE_PIN Y28      [get_ports "FMC3_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA05N"]
set_property PACKAGE_PIN U24      [get_ports "FMC3_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA06P"]
set_property PACKAGE_PIN U25      [get_ports "FMC3_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA06N"]
set_property PACKAGE_PIN V27      [get_ports "FMC3_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA07P"]
set_property PACKAGE_PIN V28      [get_ports "FMC3_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA07N"]
set_property PACKAGE_PIN V21      [get_ports "FMC3_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA08P"]
set_property PACKAGE_PIN W21      [get_ports "FMC3_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA08N"]
set_property PACKAGE_PIN T22      [get_ports "FMC3_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA09P"]
set_property PACKAGE_PIN T23      [get_ports "FMC3_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA09N"]
set_property PACKAGE_PIN V22      [get_ports "FMC3_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA10P"]
set_property PACKAGE_PIN V23      [get_ports "FMC3_LA10N"]
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set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA10N"]
set_property PACKAGE_PIN U21      [get_ports "FMC3_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA11P"]
set_property PACKAGE_PIN U22      [get_ports "FMC3_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA11N"]
set_property PACKAGE_PIN AB21     [get_ports "FMC3_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA12P"]
set_property PACKAGE_PIN AC21     [get_ports "FMC3_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA12N"]
set_property PACKAGE_PIN AA20     [get_ports "FMC3_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA13P"]
set_property PACKAGE_PIN AB20     [get_ports "FMC3_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA13N"]
set_property PACKAGE_PIN AC22     [get_ports "FMC3_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA14P"]
set_property PACKAGE_PIN AC23     [get_ports "FMC3_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA14N"]
set_property PACKAGE_PIN AA22     [get_ports "FMC3_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA15P"]
set_property PACKAGE_PIN AB22     [get_ports "FMC3_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA15N"]
set_property PACKAGE_PIN AB25     [get_ports "FMC3_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA16P"]
set_property PACKAGE_PIN AB26     [get_ports "FMC3_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA16N"]
set_property PACKAGE_PIN AA32     [get_ports "FMC3_LA17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA17_CC_P"]
set_property PACKAGE_PIN AB32     [get_ports "FMC3_LA17_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA17_CC_N"]
set_property PACKAGE_PIN AD30     [get_ports "FMC3_LA18_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA18_CC_P"]
set_property PACKAGE_PIN AD31     [get_ports "FMC3_LA18_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA18_CC_N"]
set_property PACKAGE_PIN V31      [get_ports "FMC3_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA19P"]
set_property PACKAGE_PIN W31      [get_ports "FMC3_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA19N"]
set_property PACKAGE_PIN Y31      [get_ports "FMC3_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA20P"]
set_property PACKAGE_PIN Y32      [get_ports "FMC3_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA20N"]
set_property PACKAGE_PIN V33      [get_ports "FMC3_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA21P"]
set_property PACKAGE_PIN W34      [get_ports "FMC3_LA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA21N"]
set_property PACKAGE_PIN W30      [get_ports "FMC3_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA22P"]
set_property PACKAGE_PIN Y30      [get_ports "FMC3_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA22N"]
set_property PACKAGE_PIN W33      [get_ports "FMC3_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA23P"]
set_property PACKAGE_PIN Y33      [get_ports "FMC3_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA23N"]
set_property PACKAGE_PIN AC33     [get_ports "FMC3_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA24P"]
set_property PACKAGE_PIN AD33     [get_ports "FMC3_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA24N"]
set_property PACKAGE_PIN AA34     [get_ports "FMC3_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA25P"]
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set_property PACKAGE_PIN AB34     [get_ports "FMC3_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA25N"]
set_property PACKAGE_PIN AA29     [get_ports "FMC3_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA26P"]
set_property PACKAGE_PIN AB29     [get_ports "FMC3_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA26N"]
set_property PACKAGE_PIN AC34     [get_ports "FMC3_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA27P"]
set_property PACKAGE_PIN AD34     [get_ports "FMC3_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA27N"]
set_property PACKAGE_PIN AE33     [get_ports "FMC3_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA28P"]
set_property PACKAGE_PIN AF34     [get_ports "FMC3_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA28N"]
set_property PACKAGE_PIN AE32     [get_ports "FMC3_LA29P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA29P"]
set_property PACKAGE_PIN AF32     [get_ports "FMC3_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA29N"]
set_property PACKAGE_PIN AF33     [get_ports "FMC3_LA30P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA30P"]
set_property PACKAGE_PIN AG34     [get_ports "FMC3_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA30N"]
set_property PACKAGE_PIN AG31     [get_ports "FMC3_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA31P"]
set_property PACKAGE_PIN AG32     [get_ports "FMC3_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA31N"]
set_property PACKAGE_PIN AF30     [get_ports "FMC3_LA32P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA32P"]
set_property PACKAGE_PIN AG30     [get_ports "FMC3_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA32N"]
set_property PACKAGE_PIN AD29     [get_ports "FMC3_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA33P"]
set_property PACKAGE_PIN AE30     [get_ports "FMC3_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA33N"]

#FMC3 HA
set_property PACKAGE_PIN Y23      [get_ports "FMC3_HA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA00_CC_P"]
set_property PACKAGE_PIN AA23     [get_ports "FMC3_HA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA00_CC_N"]
set_property PACKAGE_PIN AC31     [get_ports "FMC3_HA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA01_CC_P"]
set_property PACKAGE_PIN AC32     [get_ports "FMC3_HA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA01_CC_N"]
set_property PACKAGE_PIN AA27     [get_ports "FMC3_HA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA02P"]
set_property PACKAGE_PIN AB27     [get_ports "FMC3_HA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA02N"]
set_property PACKAGE_PIN AC26     [get_ports "FMC3_HA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA03P"]
set_property PACKAGE_PIN AC27     [get_ports "FMC3_HA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA03N"]
set_property PACKAGE_PIN AB24     [get_ports "FMC3_HA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA04P"]
set_property PACKAGE_PIN AC24     [get_ports "FMC3_HA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA04N"]
set_property PACKAGE_PIN AD25     [get_ports "FMC3_HA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA05P"]
set_property PACKAGE_PIN AD26     [get_ports "FMC3_HA05N"]
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set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA05N"]
set_property PACKAGE_PIN Y26      [get_ports "FMC3_HA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA06P"]
set_property PACKAGE_PIN Y27      [get_ports "FMC3_HA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA06N"]
set_property PACKAGE_PIN AF29     [get_ports "FMC3_HA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA07P"]
set_property PACKAGE_PIN AG29     [get_ports "FMC3_HA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA07N"]
set_property PACKAGE_PIN AC28     [get_ports "FMC3_HA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA08P"]
set_property PACKAGE_PIN AD28     [get_ports "FMC3_HA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA08N"]
set_property PACKAGE_PIN AE28     [get_ports "FMC3_HA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA09P"]
set_property PACKAGE_PIN AF28     [get_ports "FMC3_HA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA09N"]
set_property PACKAGE_PIN AE27     [get_ports "FMC3_HA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA10P"]
set_property PACKAGE_PIN AF27     [get_ports "FMC3_HA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA10N"]

#SuperClock2_MODULE
set_property PACKAGE_PIN AL24     [get_ports "CM_RST"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_RST"]
set_property PACKAGE_PIN AP21     [get_ports "CM_C1B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C1B"]
set_property PACKAGE_PIN AM24     [get_ports "CM_C2B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C2B"]
set_property PACKAGE_PIN AN24     [get_ports "CM_C3B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C3B"]
set_property PACKAGE_PIN AM22     [get_ports "CM_C1A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C1A"]
set_property PACKAGE_PIN AN22     [get_ports "CM_C2A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C2A"]
set_property PACKAGE_PIN AM21     [get_ports "CM_H_CS0_C3A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_CS0_C3A"]
set_property PACKAGE_PIN AN21     [get_ports "CM_H_CS1_C4A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_CS1_C4A"]
set_property PACKAGE_PIN AN23     [get_ports "CM_H_DEC"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_DEC"]
set_property PACKAGE_PIN AP23     [get_ports "CM_H_INC"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_INC"]
set_property PACKAGE_PIN AP24     [get_ports "CM_FS_ALIGN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_FS_ALIGN"]
set_property PACKAGE_PIN AP25     [get_ports "CM_H_LOL"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_LOL"]
set_property PACKAGE_PIN AP20     [get_ports "CM_H_INT_ALRM"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_INT_ALRM"]
set_property PACKAGE_PIN U34      [get_ports "CM_LVDS1_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS1_P"]
set_property PACKAGE_PIN V34      [get_ports "CM_LVDS1_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS1_N"]
set_property PACKAGE_PIN J8       [get_ports "CM_LVDS2_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS2_P"]
set_property PACKAGE_PIN H8       [get_ports "CM_LVDS2_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS2_N"]
set_property PACKAGE_PIN AK22     [get_ports "CM_GCLK_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_GCLK_P"]
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set_property PACKAGE_PIN AK23     [get_ports "CM_GCLK_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_GCLK_N"]

#SWITCHES
set_property PACKAGE_PIN J19      [get_ports "USER_SW1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW1"]
set_property PACKAGE_PIN H19      [get_ports "USER_SW2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW2"]
set_property PACKAGE_PIN G19      [get_ports "USER_SW3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW3"]
set_property PACKAGE_PIN F19      [get_ports "USER_SW4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW4"]
set_property PACKAGE_PIN J18      [get_ports "USER_SW5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW5"]
set_property PACKAGE_PIN H18      [get_ports "USER_SW6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW6"]
set_property PACKAGE_PIN F18      [get_ports "USER_SW7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW7"]
set_property PACKAGE_PIN F17      [get_ports "USER_SW8"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW8"]
set_property PACKAGE_PIN L15      [get_ports "USER_PB1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_PB1"]
set_property PACKAGE_PIN L18      [get_ports "USER_PB2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_PB2"]

#LEDs
set_property PACKAGE_PIN D18      [get_ports "APP_LED1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED1"]
set_property PACKAGE_PIN D19      [get_ports "APP_LED2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED2"]
set_property PACKAGE_PIN C18      [get_ports "APP_LED3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED3"]
set_property PACKAGE_PIN C19      [get_ports "APP_LED4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED4"]
set_property PACKAGE_PIN B19      [get_ports "APP_LED5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED5"]
set_property PACKAGE_PIN A19      [get_ports "APP_LED6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED6"]
set_property PACKAGE_PIN A18      [get_ports "APP_LED7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED7"]
set_property PACKAGE_PIN B16      [get_ports "APP_LED8"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED8"]

#SMAs
set_property PACKAGE_PIN G10      [get_ports "CLK_DIFF_1_P"]
set_property IOSTANDARD  LVDS     [get_ports "CLK_DIFF_1_P"]
set_property PACKAGE_PIN F10      [get_ports "CLK_DIFF_1_N"]
set_property IOSTANDARD  LVDS  [get_ports "CLK_DIFF_1_N"]
set_property PACKAGE_PIN G9       [get_ports "CLK_DIFF_2_P"]
set_property IOSTANDARD  LVDS   [get_ports "CLK_DIFF_2_P"]
set_property PACKAGE_PIN F9       [get_ports "CLK_DIFF_2_N"]
set_property IOSTANDARD  LVDS  [get_ports "CLK_DIFF_2_N"]

#SYSTEM CLOCKS
set_property PACKAGE_PIN E18      [get_ports "LVDS_OSC_P"]
set_property IOSTANDARD  LVDS   [get_ports "LVDS_OSC_P"]
set_property PACKAGE_PIN E17      [get_ports "LVDS_OSC_N"]
set_property IOSTANDARD  LVDS  [get_ports "LVDS_OSC_N"]
```

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#PMBUS
set_property PACKAGE_PIN E15      [get_ports "DUT_PMBUS_ALERT"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_ALERT"]
set_property PACKAGE_PIN B15      [get_ports "DUT_PMBUS_CLK"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_CLK"]
set_property PACKAGE_PIN A15      [get_ports "DUT_PMBUS_DATA"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_DATA"]
set_property PACKAGE_PIN N27      [get_ports "DUT_SMAP_CSI_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_CSI_B"]
set_property PACKAGE_PIN M20      [get_ports "DUT_SMAP_D4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D4"]
set_property PACKAGE_PIN L20      [get_ports "DUT_SMAP_D5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D5"]
set_property PACKAGE_PIN R21      [get_ports "DUT_SMAP_D6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D6"]
set_property PACKAGE_PIN R22      [get_ports "DUT_SMAP_D7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D7"]
set_property PACKAGE_PIN K16      [get_ports "DUT_FREQ_CLK"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_CLK"]
set_property PACKAGE_PIN K15      [get_ports "DUT_FREQ_DATA"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_DATA"]
set_property PACKAGE_PIN K18      [get_ports "DUT_FREQ_BSY"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_BSY"]
set_property PACKAGE_PIN K17      [get_ports "DUT_FREQ_RDY"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_RDY"]

#UART
set_property PACKAGE_PIN B14      [get_ports "UART_TXD_O"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_TXD_O"]
set_property PACKAGE_PIN A14      [get_ports "UART_RXD_I"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_RXD_I"]
set_property PACKAGE_PIN C14      [get_ports "UART_RTS_O_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_RTS_O_B"]
set_property PACKAGE_PIN D14      [get_ports "UART_CTS_I_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_CTS_I_B"]

#USB_GPIOs
set_property PACKAGE_PIN F14      [get_ports "UART_GPIO_0"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_0"]
set_property PACKAGE_PIN G14      [get_ports "UART_GPIO_1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_1"]
set_property PACKAGE_PIN J14      [get_ports "UART_GPIO_2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_2"]
set_property PACKAGE_PIN J15      [get_ports "UART_GPIO_3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_3"]

#MGTs
set_property PACKAGE_PIN N29      [get_ports "131_REFCLK1_P"]
set_property PACKAGE_PIN N30      [get_ports "131_REFCLK1_N"]
set_property PACKAGE_PIN R29      [get_ports "131_REFCLK0_P"]
set_property PACKAGE_PIN R30      [get_ports "131_REFCLK0_N"]
set_property PACKAGE_PIN K31      [get_ports "131_TX3_P"]
set_property PACKAGE_PIN K32      [get_ports "131_TX3_N"]
set_property PACKAGE_PIN J33      [get_ports "131_RX3_P"]
set_property PACKAGE_PIN J34      [get_ports "131_RX3_N"]
set_property PACKAGE_PIN M31      [get_ports "131_TX2_P"]
set_property PACKAGE_PIN M32      [get_ports "131_TX2_N"]
set_property PACKAGE_PIN L33      [get_ports "131_RX2_P"]
set_property PACKAGE_PIN L34      [get_ports "131_RX2_N"]
```

```
set_property PACKAGE_PIN P31      [get_ports "131_TX1_P"]
set_property PACKAGE_PIN P32      [get_ports "131_TX1_N"]
set_property PACKAGE_PIN N33      [get_ports "131_RX1_P"]
set_property PACKAGE_PIN N34      [get_ports "131_RX1_N"]
set_property PACKAGE_PIN T31      [get_ports "131_TX0_P"]
set_property PACKAGE_PIN T32      [get_ports "131_TX0_N"]
set_property PACKAGE_PIN R33      [get_ports "131_RX0_P"]
set_property PACKAGE_PIN R34      [get_ports "131_RX0_N"]
set_property PACKAGE_PIN J29      [get_ports "132_REFCLK1_P"]
set_property PACKAGE_PIN J30      [get_ports "132_REFCLK1_N"]
set_property PACKAGE_PIN L29      [get_ports "132_REFCLK0_P"]
set_property PACKAGE_PIN L30      [get_ports "132_REFCLK0_N"]
set_property PACKAGE_PIN B31      [get_ports "132_TX3_P"]
set_property PACKAGE_PIN B32      [get_ports "132_TX3_N"]
set_property PACKAGE_PIN C33      [get_ports "132_RX3_P"]
set_property PACKAGE_PIN C34      [get_ports "132_RX3_N"]
set_property PACKAGE_PIN D31      [get_ports "132_TX2_P"]
set_property PACKAGE_PIN D32      [get_ports "132_TX2_N"]
set_property PACKAGE_PIN E33      [get_ports "132_RX2_P"]
set_property PACKAGE_PIN E34      [get_ports "132_RX2_N"]
set_property PACKAGE_PIN G29      [get_ports "132_TX1_P"]
set_property PACKAGE_PIN G30      [get_ports "132_TX1_N"]
set_property PACKAGE_PIN F31      [get_ports "132_RX1_P"]
set_property PACKAGE_PIN F32      [get_ports "132_RX1_N"]
set_property PACKAGE_PIN H31      [get_ports "132_TX0_P"]
set_property PACKAGE_PIN H32      [get_ports "132_TX0_N"]
set_property PACKAGE_PIN G33      [get_ports "132_RX0_P"]
set_property PACKAGE_PIN G34      [get_ports "132_RX0_N"]
set_property PACKAGE_PIN AD6      [get_ports "224_REFCLK1_P"]
set_property PACKAGE_PIN AD5      [get_ports "224_REFCLK1_N"]
set_property PACKAGE_PIN AF6      [get_ports "224_REFCLK0_P"]
set_property PACKAGE_PIN AF5      [get_ports "224_REFCLK0_N"]
set_property PACKAGE_PIN AK6      [get_ports "224_TX3_P"]
set_property PACKAGE_PIN AK5      [get_ports "224_TX3_N"]
set_property PACKAGE_PIN AJ4      [get_ports "224_RX3_P"]
set_property PACKAGE_PIN AJ3      [get_ports "224_RX3_N"]
set_property PACKAGE_PIN AL4      [get_ports "224_TX2_P"]
set_property PACKAGE_PIN AL3      [get_ports "224_TX2_N"]
set_property PACKAGE_PIN AK2      [get_ports "224_RX2_P"]
set_property PACKAGE_PIN AK1      [get_ports "224_RX2_N"]
set_property PACKAGE_PIN AM6      [get_ports "224_TX1_P"]
set_property PACKAGE_PIN AM5      [get_ports "224_TX1_N"]
set_property PACKAGE_PIN AM2      [get_ports "224_RX1_P"]
set_property PACKAGE_PIN AM1      [get_ports "224_RX1_N"]
set_property PACKAGE_PIN AN4      [get_ports "224_TX0_P"]
set_property PACKAGE_PIN AN3      [get_ports "224_TX0_N"]
set_property PACKAGE_PIN AP2      [get_ports "224_RX0_P"]
set_property PACKAGE_PIN AP1      [get_ports "224_RX0_N"]
set_property PACKAGE_PIN Y6       [get_ports "225_REFCLK1_P"]
set_property PACKAGE_PIN Y5       [get_ports "225_REFCLK1_N"]
set_property PACKAGE_PIN AB6      [get_ports "225_REFCLK0_P"]
set_property PACKAGE_PIN AB5      [get_ports "225_REFCLK0_N"]
set_property PACKAGE_PIN AC4      [get_ports "225_TX3_P"]
set_property PACKAGE_PIN AC3      [get_ports "225_TX3_N"]
set_property PACKAGE_PIN AB2      [get_ports "225_RX3_P"]
set_property PACKAGE_PIN AB1      [get_ports "225_RX3_N"]
set_property PACKAGE_PIN AE4      [get_ports "225_TX2_P"]
set_property PACKAGE_PIN AE3      [get_ports "225_TX2_N"]
set_property PACKAGE_PIN AD2      [get_ports "225_RX2_P"]
```

```
set_property PACKAGE_PIN AD1      [get_ports "225_RX2_N"]
set_property PACKAGE_PIN AG4      [get_ports "225_TX1_P"]
set_property PACKAGE_PIN AG3      [get_ports "225_TX1_N"]
set_property PACKAGE_PIN AF2      [get_ports "225_RX1_P"]
set_property PACKAGE_PIN AF1      [get_ports "225_RX1_N"]
set_property PACKAGE_PIN AH6      [get_ports "225_TX0_P"]
set_property PACKAGE_PIN AH5      [get_ports "225_TX0_N"]
set_property PACKAGE_PIN AH2      [get_ports "225_RX0_P"]
set_property PACKAGE_PIN AH1      [get_ports "225_RX0_N"]
set_property PACKAGE_PIN T6       [get_ports "226_REFCLK1_P"]
set_property PACKAGE_PIN T5       [get_ports "226_REFCLK1_N"]
set_property PACKAGE_PIN V6       [get_ports "226_REFCLK0_P"]
set_property PACKAGE_PIN V5       [get_ports "226_REFCLK0_N"]
set_property PACKAGE_PIN R4       [get_ports "226_TX3_P"]
set_property PACKAGE_PIN R3       [get_ports "226_TX3_N"]
set_property PACKAGE_PIN P2       [get_ports "226_RX3_P"]
set_property PACKAGE_PIN P1       [get_ports "226_RX3_N"]
set_property PACKAGE_PIN U4       [get_ports "226_TX2_P"]
set_property PACKAGE_PIN U3       [get_ports "226_TX2_N"]
set_property PACKAGE_PIN T2       [get_ports "226_RX2_P"]
set_property PACKAGE_PIN T1       [get_ports "226_RX2_N"]
set_property PACKAGE_PIN W4       [get_ports "226_TX1_P"]
set_property PACKAGE_PIN W3       [get_ports "226_TX1_N"]
set_property PACKAGE_PIN V2       [get_ports "226_RX1_P"]
set_property PACKAGE_PIN V1       [get_ports "226_RX1_N"]
set_property PACKAGE_PIN AA4      [get_ports "226_TX0_P"]
set_property PACKAGE_PIN AA3      [get_ports "226_TX0_N"]
set_property PACKAGE_PIN Y2       [get_ports "226_RX0_P"]
set_property PACKAGE_PIN Y1       [get_ports "226_RX0_N"]
set_property PACKAGE_PIN M6       [get_ports "227_REFCLK1_P"]
set_property PACKAGE_PIN M5       [get_ports "227_REFCLK1_N"]
set_property PACKAGE_PIN P6       [get_ports "227_REFCLK0_P"]
set_property PACKAGE_PIN P5       [get_ports "227_REFCLK0_N"]
set_property PACKAGE_PIN G4       [get_ports "227_TX3_P"]
set_property PACKAGE_PIN G3       [get_ports "227_TX3_N"]
set_property PACKAGE_PIN F2       [get_ports "227_RX3_P"]
set_property PACKAGE_PIN F1       [get_ports "227_RX3_N"]
set_property PACKAGE_PIN J4       [get_ports "227_TX2_P"]
set_property PACKAGE_PIN J3       [get_ports "227_TX2_N"]
set_property PACKAGE_PIN H2       [get_ports "227_RX2_P"]
set_property PACKAGE_PIN H1       [get_ports "227_RX2_N"]
set_property PACKAGE_PIN L4       [get_ports "227_TX1_P"]
set_property PACKAGE_PIN L3       [get_ports "227_TX1_N"]
set_property PACKAGE_PIN K2       [get_ports "227_RX1_P"]
set_property PACKAGE_PIN K1       [get_ports "227_RX1_N"]
set_property PACKAGE_PIN N4       [get_ports "227_TX0_P"]
set_property PACKAGE_PIN N3       [get_ports "227_TX0_N"]
set_property PACKAGE_PIN M2       [get_ports "227_RX0_P"]
set_property PACKAGE_PIN M1       [get_ports "227_RX0_N"]
set_property PACKAGE_PIN H6       [get_ports "228_REFCLK1_P"]
set_property PACKAGE_PIN H5       [get_ports "228_REFCLK1_N"]
set_property PACKAGE_PIN K6       [get_ports "228_REFCLK0_P"]
set_property PACKAGE_PIN K5       [get_ports "228_REFCLK0_N"]
set_property PACKAGE_PIN B6       [get_ports "228_TX3_P"]
set_property PACKAGE_PIN B5       [get_ports "228_TX3_N"]
set_property PACKAGE_PIN A4       [get_ports "228_RX3_P"]
set_property PACKAGE_PIN A3       [get_ports "228_RX3_N"]
set_property PACKAGE_PIN C4       [get_ports "228_TX2_P"]
set_property PACKAGE_PIN C3       [get_ports "228_TX2_N"]
```

```
set_property PACKAGE_PIN B2       [get_ports "228_RX2_P"]
set_property PACKAGE_PIN B1       [get_ports "228_RX2_N"]
set_property PACKAGE_PIN D6       [get_ports "228_TX1_P"]
set_property PACKAGE_PIN D5       [get_ports "228_TX1_N"]
set_property PACKAGE_PIN D2       [get_ports "228_RX1_P"]
set_property PACKAGE_PIN D1       [get_ports "228_RX1_N"]
set_property PACKAGE_PIN F6       [get_ports "228_TX0_P"]
set_property PACKAGE_PIN F5       [get_ports "228_TX0_N"]
set_property PACKAGE_PIN E4       [get_ports "228_RX0_P"]
set_property PACKAGE_PIN E3       [get_ports "228_RX0_N"]
```

System Controller

Main Menu

The system controller command line can be accessed through a serial communication terminal connection (115200-8-N-1) using the enhanced communication port of the Silicon Labs USB to dual-UART described in USB to Dual-UART Bridge.

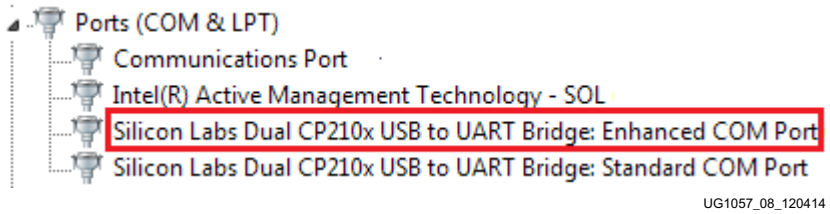

Figure D-1: **Silicon Labs Enhanced COM Port**

The main menu lists the available options.

```
KCU1250 System Controller
- Main Menu -
------------------------------
1. Set Programmable Clocks
2. Get Power System (PMBUS) Voltages
3. Get Power Monitoring Data (INA226)
4. Adjust FPGA Mezzanine Card (FMC) Settings
5. Get GPIO Data
6. Configure UltraScale FPGA Select an option
```

Programmable Clocks Menu

The clock menu is used to set the frequency of the SuperClock-2 module (see SuperClock-2 Module) clock sources.

```
KCU1250 System Controller
      - Clock Menu -
-----------------------------
1. Set KCU1250 Si570 Frequency
2. Set KCU1250 Si5368 Frequency
0. Return to Main Menu
```

Clock Menu Options

This section includes a description of the clock menu options, presenting arbitrary sample value entries and the system controller responses. The entry value commentary is shown in parentheses.

- Set KCU1250 Si570 Frequency

  ```
  Enter the Si570 frequency (10-810MHz):

  200
  ```

  (Enter a value between 10 and 810.)

  ```
  Freq:200.0000000000 HS_DIV=7 N1=4 DCO=5600.0 RFREQ=0x030FFFF785
  ```

  (The returned values include diagnostic information.)

- Set KCU1250 Si5368 Frequency

  ```
  Enter the Si5368 output frequency (0.002-808MHz):

  200

  Freq:200.0000000000 fosc=5600.000MHz f3= 5.000KHz LBW=0.200KHz
  N1=28 N1_HS=7 NC1_LS=4 N2=1120000 N2_HS=4 N2_LS=280000 N31=40000
  N32=22857
  ```

  (The returned values include diagnostic information.)

  Note: Several seconds might elapse before the result is returned.

IMPORTANT: *Make sure J121 is set to position (2-3) DUT I2C DIS to isolate the DUT I2C signals and prevent bus contention. If contention occurs, the system controller stalls while executing the above commands.*

- Return to Main Menu

This option returns to the menu level above.

PMBus Menu

The PMBus bus commands are used to read the voltage settings of the KCU1250 board power rails controlled by the Maxim power system. Through the PMBus menu these power rails can be read once or scanned continuously until stopped by a key press. Table D-1 lists the voltage rails accessible through the system controller's interface to the Maxim PMBus.

Table D-1: **Voltage Rails Accessible Through System Controller's Interface to PMBus**

Maxim Power Supply Rail	I2C Address	Nominal Voltage
VCCINT	0x0A	0.95V
VCCAUX	0x0B	1.80V
VCCBRAM	0x0F	0.95V
VCCO_HP	0x13	1.80V
VCCO_HR	0x11	1.80V
UTIL_5V0	0x1C	5.00V
UTIL_3V3	0x1D	3.30V
UTIL_2V5	0x1A	2.50V

PMBus Menu Options

```
KCU1250 System Controller
    - PMBus Menu -
-----------------------------
1. Get PMBus Voltages
2. Continuous Scan PMBus Voltages
3. Get VCCINT Voltage
4. Get VCCAUX Voltage
5. Get VCCBRAM Voltage
6. Get VCCOHP Voltage
7. Get VCCOHR Voltage
8. Get UTIL5V0 Voltage
9. Get UTIL3V3 Voltage
A. Get UTIL2V5 Voltage
0. Return to Main Menu
```

- Get PMBus Voltages

```
VCCINT = 0.950V
VCCAUX = 1.800V
VCCBRAM = 0.950V
VCCO_HP = 1.800V
VCCO_HR = 1.801V
UTIL2V5 = 2.500V
UTIL3V3 = 3.300V
UTIL5V0 = 4.999V
```

- Continuous Scan PMBus Voltages

  The voltages listed in option 1 are displayed and updated about once per second. Pressing any key displays the PMBus menu.

- Get VCCINT Voltage

```
VCCINT = 0.950V
Unscaled Hex: MSB = 0x0F, LSB = 0x32
```

  (The returned values include diagnostic information.)

- Get VCCAUX Voltage

```
VCCAUX = 1.800V
Unscaled Hex: MSB = 0x1C, LSB = 0xCC
```

  (The returned values include diagnostic information.)

- Get VCCBRAM Voltage

```
VCCBRAM = 0.950V
Unscaled Hex: MSB = 0x0F, LSB = 0x33
```

(The returned values include diagnostic information.)

- Get VCCO_HP Voltage

```
VCCO_HP = 1.800V
Unscaled Hex: MSB = 0x1C, LSB = 0xCE
```

(The returned values include diagnostic information.)

- Get VCCO_HR Voltage

```
VCCO_HR = 1.800V
Unscaled Hex: MSB = 0x1C, LSB = 0xCD
```

(The returned values include diagnostic information.)

- Get UTIL5V0 Voltage

```
UTIL5V0 = 5.000V
Unscaled Hex: MSB = 0x50, LSB = 0x02
```

(The returned values include diagnostic information.)

- Get UTIL3V3 Voltage

```
UTIL3V3 = 3.299V
Unscaled Hex: MSB = 0x34, LSB = 0xC8
```

(The returned values include diagnostic information.)

- Get UTIL2V5 Voltage

```
UTIL2V5 = 2.500V
Unscaled Hex: MSB = 0x28, LSB = 0x02
```

(The returned values include diagnostic information.)

Power Monitoring Data Menu

The KCU1250 board includes the Texas Instruments INA226 power monitoring device. The Power Monitoring Data menu, unlike the PMBus menu, provides both voltage and current monitoring for the MGT power modules, as well as for the FPGA fabric power rails.

```
KCU1250 System Controller
    - Power Monitoring Data Menu -
----------------------------
1. Continuous Scan Voltage and Current
2. Advanced INA226 Setting
```

- Continuous Scan Voltage and Current

  This option lists the voltages shown in option 1 of the PMBus menu and displays the average, minimum, and maximum current of each rail. The list is updated about once per second. Pressing any key displays the PMBus menu.

- Advanced INA226 Setting

  This option can be used to select one of the PMBus power monitors and explore additional user settings such as monitor calibration. Refer to the INA226 data sheet [Ref 7] for device registers information.

  - Select the Advanced Setting Operation

    ```
    KCU1250 System Controller
        - INA226 Advanced Menu -
    ----------------------------
    1. Select INA226 Device
    2. Get INA226 Register
    3. Set INA226 Register
    0. Return to Previous Menu
    ```

    - Select the Device

      ```
      KCU1250 System Controller
          - Select INA226 Menu -
      ----------------------------
      1. Select VCCINT Monitor
      2. Select VCCAUX Monitor
      3. Select VCCBRAM Monitor
      4. Select VCCO_HP Monitor
      5. Select VCCO_HR Monitor
      6. Select MGTAVCC Monitor
      7. Select MGTAVTT Monitor
      8. Select MGTVCCAUX Monitor
      0. Return to Previous Menu
      ```

- Read the Selected INA226 Registers

```
KCU1250 System Controller
    - RAIL INA226 Menu -
----------------------------
1. Get SHUNT Register
2. Get BUS Register
3. Get POWER Register
4. Get CURRENT Register
5. Get CALIBRATION Register
6. Get MASK_ENABLE Register
7. Get ALERT_LIMIT Register
8. Get CONFIGURATION Register
9. Get DIE ID Register
0. Return to Previous Menu
```

- Set the Selected INA226 Registers

```
KCU1250 System Controller
    - RAIL INA226 Menu -
----------------------------
1. Set CALIBRATION Register
2. Set MASK_ENABLE Register
3. Set ALERT_LIMIT Register
4. Set CONFIGURATION Register
0. Return to Previous Menu
```

FPGA Mezzanine Card Menu

The KCU1250 board includes three FPGA mezzanine card (FMC) ANSI/VITA 57.1 expansion interfaces. All FMC cards must host an IIC EEPROM that can be read through the FMC menu. A raw hexadecimal display and a formatted version of the FMC EEPROM data are provided through the FMC menu. The VITA 57.1 standard identifies the data fields of the intelligent platform management interface (IPMI) specification used for the FMC EEPROM. The KCU1250 board system controller supports the programmable clock resources on these FMC modules:

IMPORTANT: *These FMC modules are not included.*

- FMC XM101 LVDS QSE card
- FMC XM104 MGT serial connectivity card
- FMC XM105 debug card
- FMC XM107 loopback card

These mezzanine cards can be attached to JA2 (callout 28), J3A (callout 29), or J4A (callout 30) of the KCU1250 board expansion ports. Table D-2 shows the accessible clock resources on each FMC module.

Table D-2: **Clock Resources on FMC Modules**

Xilinx FMC Module/Board	Clock Source #1	Clock Source #2
XM101	Si570	SI570
XM104	Si570	Si5638
XM105	Si570	N/A
XM107	Si570	N/A

FMC Menu Options

```
KCU1250 System Controller
     - FMC Menu -
------------------------------
1. Set FMC XMxxx CLOCKS
2. Read FMC1 IIC EEPROM
3. Read FMC2 IIC EEPROM
4. Read FMC3 IIC EEPROM
0. Return to Main Menu
```

Identify the FMC module type(s) and the FMC connecter number. These examples use FMC-XM107 connected to FMC1.

- Set FMC XMxxx Clocks

```
KCU1250 System Controller
       - FMC Clock Menu -
------------------------------
1. Set FMC XM101 Clocks
2. Set FMC XM104 Clocks
3. Set FMC XM105 Clocks
4. Set FMC XM107 Clocks
0. Return to FMC Menu
```

- Set FMC XM107 Clocks

```
KCU1250 System Controller
       - XM107 Menu -
------------------------------
1. Set FMC1 Si570 Frequency
2. Set FMC2 Si570 Frequency
3. Set FMC3 Si570 Frequency
0. Return to FMC Clock Menu
```

- Set FMC1 Si570 Frequency

  (The returned values include diagnostic information.)

```
FMC1 card present
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 37

Enter the Si570 frequency (10-810MHz):
100
Freq:100.0000000000 HS_DIV=5 N1=10 DCO=5000.0 RFREQ=0x02BC7E566E
```

  (The returned values include diagnostic information.)

- Read FMC IIC EEPROM

  If the FMC IIC EEPROM has been programmed, several data groupings are displayed:

```
ReadBuffer[000] - ReadBuffer[255] displays various value contents
Common Header
Board Area Info
MultiRecord Area
- OEM FMC Record
- DC Load Records (three groups)
- DC Output Records (three groups)
```

  If the FMC IIC EEPROM has not been programmed, ReadBuffer[000] - ReadBuffer[255] displays buffer contents = `0xFF`, and the common header reports "Invalid Format Version FF".

GPIO Data Menu

The system controller continuously scans specific user activated inputs and several onboard status signals. Positions 1 - 4 (ADDR3, ADDR2, ADDR1, ADDR0) of address DIP switch SW13 are monitored, as well as five user pushbuttons (SW5, SW6, SW10, SW11, SW12).

GPIO Menu Options

```
KCU1250 System Controller
- GPIO Menu-
1. Get GPIO PL Data
2. Continuous Scan GPIO Readings
0. Return to Main Menu
Select an option
```

- Get GPIO PL Data

  The signals monitored with this option are currently not available in the KCU1250 board.

```
----------------------
FMC1_PRSNT = NO
FMC2_PRSNT = NO
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = NO
PMBUS_ALERT = No
```

- Continuous Scan GPIO Readings

```
Press any Key to Return to GPIO Menu
```

  When any of the address DIP SW13 poles 1-4 are changed, or a pushbutton pressed, the value beneath the switch position changes accordingly (showing a 0 or a 1).

```
SYS ADDR (SW13) (ADDR3, ADDR2, ADDR1, ADDR0)
                     0      0      0      0
Pushbuttons (SW11, SW12, SW5, SW6, SW10)
                0      0     0     0      0
----------------------
FMC1_PRSNT    = NO
FMC2_PRSNT    = NO
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = NO
PMBUS_ALERT   = NO
```

FPGA CONFIG Menu

The system controller CONFIG menu is used to configure the KCU1250 board UltraScale FPGA from an SD card (callout 7). The directory structure and content of the SD card must adhere to the data format specified in Xilinx XAPP1229. One of 16 bitstreams can be selected for use by the configuration engine by setting a binary encoded value on the system controller mode DIP switch SW13 (see System Controller Configuration DIP Switches).

CONFIG Menu Options

```
KCU1250 System Controller
    - CONFIG Menu -
----------------------------
1. Configure UltraScale FPGA from SD Card
0. Return to Main Menu
```

- Configure UltraScale FPGA from microSD Card

```
Info: Xilinx.sys opened
Info Configuration definition file "kcu1250/set0/config.def" opened
Info: Clock divider is set to 2
Info: Total 1 device(s) in the chain
Info: Total 1 configuration target(s) in the chain
Info: Configuring target(s)...
Info: Bitfile "kcu1250/set0/kcu1250_leds.bit" opened
...10%...20%...30%...40%...50%...60%...70%...80%...90%...100%
Configuration completed successfully
```

- Return to Main Menu

  This option returns to the menu level above.

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the KCU1250 board master answer record concerning the CE requirements for the PC Test Environment:

Master Answer Record (Xilinx AR63058)

Declaration of Conformity

The Kintex UltraScale KCU1250 Declaration of Conformity will be made available online.

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For continual updates, add the Answer Record to your myAlerts

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the KCU1250 board and its documentation is available on these websites:

KCU1250 Characterization Kit

KCU1250 Characterization Kit – Master Answer Record (Xilinx AR63058)

These Xilinx documents provide supplemental material useful with this guide:

1. *UltraScale Architecture and Product Overview* (DS890)
2. *UltraScale Architecture System Monitor User Guide* (UG580)
3. *Vivado Design Suite User Guide: Using Constraints* (UG903)
4. *SuperClock-2 Module User Guide* (UG770)

For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

5. Information about the power system components used by the KCU1250 board is available from the Maxim Integrated website at: www.maximintegrated.com/en/products/power/intune

   Information about the MGT power supply modules included with the KCU1250 characterization kit is available from these vendors:

   a. Texas Instruments: http://www.ti.com/tool/pmp9463?keyMatch=PMP9463&tisearch=Search-EN

   b. Maxim Integrated: www.maximintegrated.com/XilinxModule

6. Samtec, Inc.: www.samtec.com
7. Texas Instruments: http://www.ti.com/lit/ds/symlink/ina226.pdf
8. Maxim Integrated: MAXPOWERTOOL002
9. Texas Instruments: EVM-P960

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