VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board

User Guide

UG957 (v1.3) October 17, 2014

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/10/2012	1.0	Initial Xilinx release.
07/30/2013	1.1	Revised Table 1-16. Replaced the Master UCF listing with the Master XDC listing in Appendix C, Master Constraints File Listing. Updated links.
12/18/2013	1.2	Revised Table 1-7 through Table 1-12 and Table 1-17. Changed device number from XC7V485T-3 FFG1761E to XC7VX485T-3 FFG1761E and XC7V485T to XC7VX485T. Pair numbers changed in FPGA Mezzanine Card HPC Interface, page 30. Revised Figure 1-10. Changed title of Appendix C to Master Constraints File Listing. Updated references in Appendix D, Additional Resources. Updated the Declaration of Conformity link in Appendix E, Regulatory and Compliance Information.
10/17/2014	1.3	In FPGA Compatibility, page 5, “Unsupported interfaces are highlighted in this document” was removed. The number of GTX transceiver power modules supplied with the VC7203 board changed from four to three in 7 Series GTX Transceiver Power Module, page 13. The VC7203 Board XDC Listing changed. The module vendor websites changed in References, page 73, Bellnix was removed, and General Electric was added.

Table of Contents

Appendix E: Regulatory and Compliance Information

XILINX

Chapter 1

VC7203 Board Features and Operation

This chapter describes the components, features, and operation of the VC7203 Virtex®-7 FPGA GTX Transceiver Characterization Board. The VC7203 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex-7 XC7VX485T-3 FFG1761E FPGA. The VC7203 board schematic, bill-of-material (BOM), layout files and reference designs are available online at the Virtex-7 FPGA VC7203 Characterization Kit website.

FPGA Compatibility

The VC7203 board is provided with Virtex-7 XC7VX485T-3 FFG1761E FPGA. The board also supports all device densities (i.e., XC7VX330T, XC7V585T, XC7VX690T, XC7V1500T, and XC7V2000T devices) in the pin-compatible FFG1761, FLG1761, and FHG1761 packages. However, certain interfaces that are available in larger density devices might not be available in the XC7VX485T device (for example: GTX QUAD_111, GTX QUAD_112, FMC 3, and so on).

VC7203 Board Features

- Virtex-7 XC7VX485T-3 FFG1761E FPGA
- Onboard power supplies for all necessary voltages
- Power jacks for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ solution Secure Digital (SD) controller
- Power module supporting Virtex-7 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Nine Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Three VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I^2C bus
- PMBus connectivity to onboard digital power supplies

- Active cooling for the FPGA

The VC7203 board block diagram is shown in Figure 1-1.

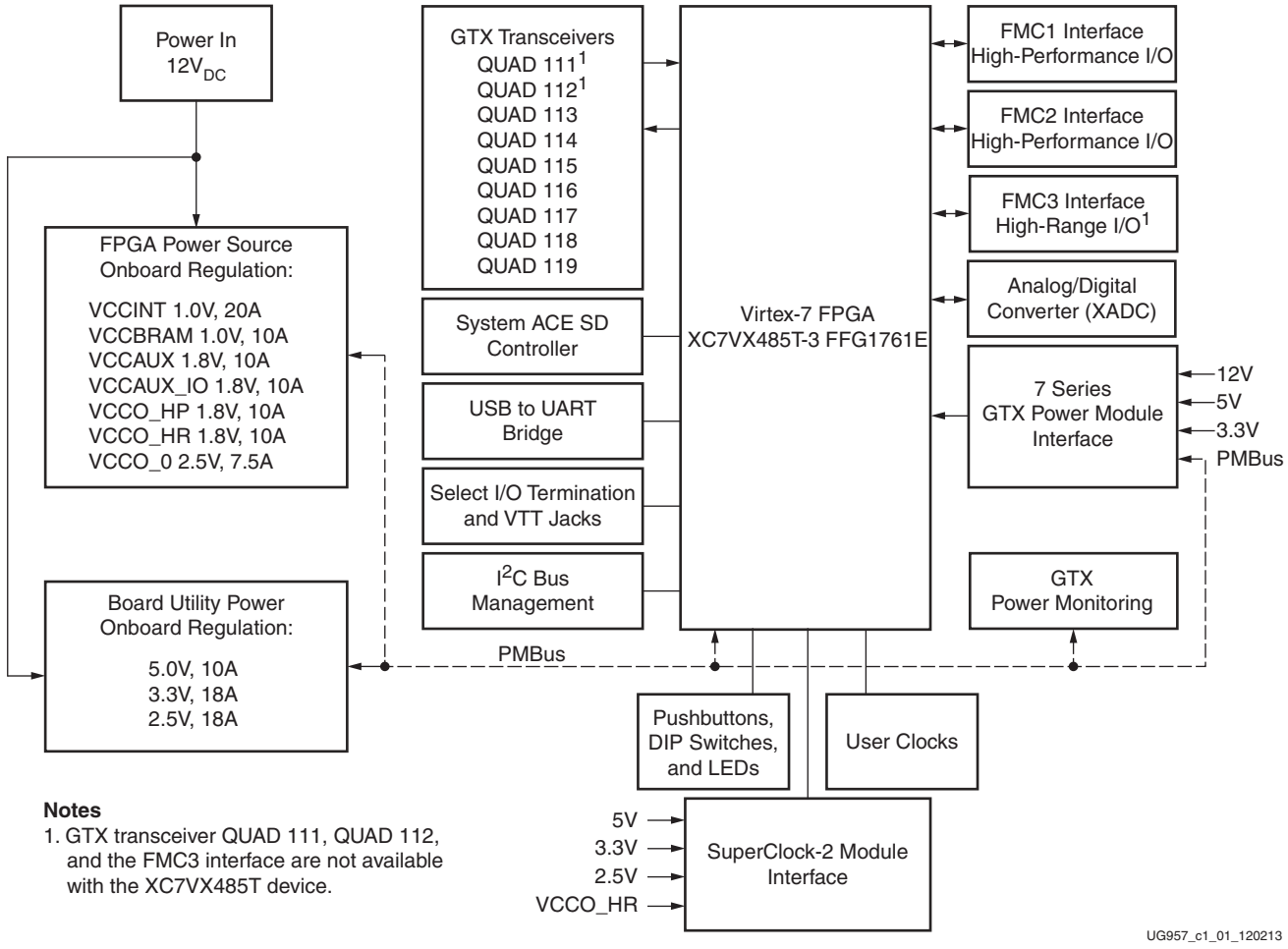


Figure 1-1: **VC7203 Board Block Diagram**

Detailed Description

Figure 1-2 shows the VC7203 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Caution! The VC7203 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

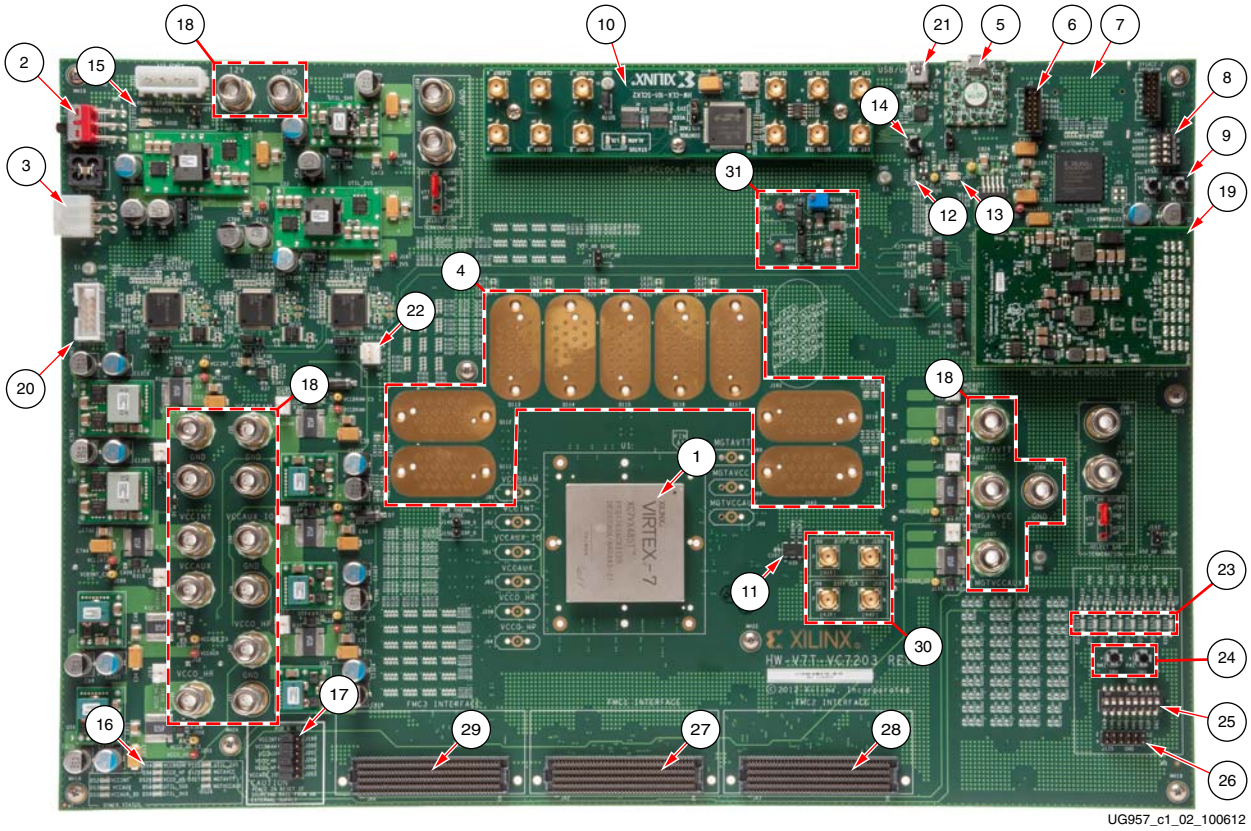


Figure 1-2: **VC7203 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **VC7203 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	Virtex-7 XC7VX485T-3 FFG1761E FPGA, page 15
2	SW1	Power switch, page 9
3	J2	12V Mini-Fit connector, page 8
4	J84, J85, J86, J158, J159, J160, J161, J162, J163	GTX transceiver connector pads Q111 , Q112, Q113, Q114, Q115, Q116, Q117, Q118 and Q119, page 22
5	U8	USB JTAG connector (micro-B receptacle), page 15
6	J7	JTAG connector (alternate access for programming cables), page 15
7	J211	System ACE tool SD card connector (back-side of board), page 15
8	SW8	System ACE tool SD configuration address DIP switches, page 17
9	SW7	System ACE tool SD RESET button, page 17
10		SuperClock-2 module, page 19
11	U35	200 MHz 2.5V LVDS oscillator, page 18
12	DS21	FPGA DONE status LED, page 17
13	DS25	FPGA INIT_B status LED, page 17

Table 1-1: **VC7203 Board Feature Descriptions *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
14	SW3	FPGA PROG_B pushbutton, page 17
15	DS11	12V power status LED, page 9
16	DS2, DS3, DS4, DS5, DS6, DS8, DS9, DS10, DS26, DS27, DS28, DS29	Status LEDS for FPGA logic, transceiver and utility power,
17	J199, J200, J201 J202, J203 J204	Power regulation jumpers for onboard regulators
18	J28, J29, J31, J32, J33, J34, J35, J36, J37, J40, J104, J105, J106, J107, J177, J178, J196	External power supply jacks, page 12
19		GTX transceiver power supply module, page 13
20	J26	PMBUS connector, page 12
21	J79	Connector for USB to UART bridge (mini-B receptacle), page 29
22	J121	Power connector for active heatsink, page 13
23	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (active-High), page 20
24	SW4, SW5	User pushbuttons (active-High), page 21
25	SW2	User DIP switches (active-High), page 20
26	J125	User I/O header, page 20
27	JA2	FMC1 connector, page 30
28	JA3	FMC2 connector page 30
29	JA4	FMC3 connector1 page 30
30	J98, J99, J100, J101	SMA connectors to differential MRCC pins on FPGA, page 18
31	J141, J142, R233	Jumpers and potentiometer for XADC reference and analog supply set-up, page 44

Power Management

Board 12V Input Power

The VC7203 board receives 12V main power through J2 (callout 3, Figure 1-2) using the 12V AC adapter that ships with the board. J2 is a 6-pin (2 x 3), right angle, Mini-Fit connector.

Caution! When supplying 12V through J2, use only the power supply provided for use with this board (Xilinx part number 3800033).

Caution! Do **NOT** use a 6-pin, PC ATX power supply connector with J2. The pinout of the 6-pin, PC ATX connector is not compatible J2 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.

12V power can also be provided through:

- Connector J131 which accepts an ATX hard drive, 4-pin, power plug
- Jacks J29 (12V) and J28 (ground) (callout 18, Figure 1-2)which can be connected to a bench-top power supply

Caution! Because jacks J29 and J28 provide no reverse polarity protection, use a power supply with a current limit set at 6A max.

Caution! Do **NOT** apply 12V power to more than a single input source. For example, do not apply power to J2 and J131 at the same time.

Power Switch

Main board power is turned on or off using switch SW1 (callout 2, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates (callout 15, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

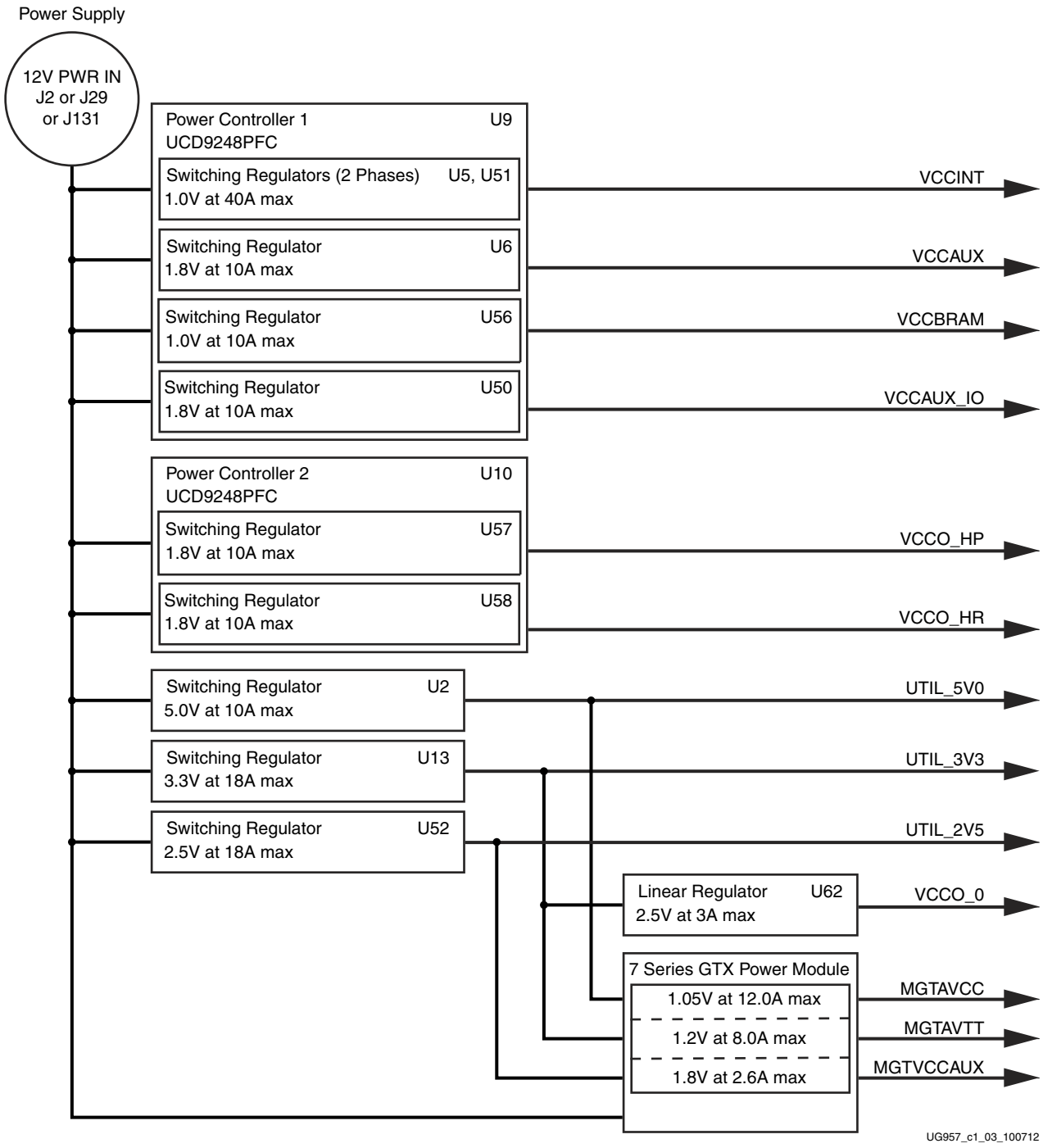


Figure 1-3: **VC7203 Board Power Supply Block Diagram**

The VC7203 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the FPGA logic and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator	Description	Power Rail Net Name	Voltage
FPGA Logic				
UCD9248PFC	U9	Digital PWM system controller, PMBUS address 52		
PTD08A020W	U5, U51	Adjustable(1) switching regulator, 40A (two phases at 20A/phase), 0.6V to 3.6V	VCCINT	1.0V
PTD08A010W	U6	Adjustable(1) switching regulator, 10A, 0.6V to 3.6V	VCCAUX	1.8V
PTD08A010W	U56	Adjustable(1) switching regulator 10A, 0.6V to 3.6V	VCCBRAM	1.0V
PTD08A020W	U50	Adjustable(1) switching regulator, 40A (two phases @ 20A/phase), 0.6V to 3.6V	VCCAUX_IO	1.8V (default)
UCD9248PFC	U10	Digital PWM system controller, PMBUS address 53		
PTD08A010W	U57	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HP	1.8V
PTD08A010W	U58	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HR	1.8V (default)
Utility				
PTH12060W	U2	Fixed switching regulator, 10A	UTIL_5V0	5.0V
PTH12020W	U13	Fixed switching regulator, 18A	UTIL_3V3	3.3V
PTH12020W	U52	Fixed switching regulator, 18A	UTIL_2V5	2.5V
TPS75925	U62	Fixed LDO regulator, 3A	VCCO_0	2.5V
GTX Transceivers (monitoring only)				
UCD9248PFC(2)	U11	Digital PWM system controller, PMBUS address 54		
XADC(3)				
ADP123	U43	Fixed LDO regulator	VCCADC_ADP	1.8V
REF3012	U45	Fixed LDO regulator	VREF_3012	1.25V
System ACE Tool SD				
ADP123	U21	Fixed LDO regulator	VCC_1V2	1.2V

Notes:

1. The output voltages of regulators controlled by a UCD9248 can be reprogrammed using the Texas Instruments Fusion Digital Power Designer application (www.ti.com/tool/fusion_digital_power_designer). However, **extreme caution must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components**.
2. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC, MGTAVTT, and MGTVCCAUX rail voltage and current levels which can be observed in real time using the Texas Instruments Fusion Digital Power Designer application (see Monitoring Voltage and Current, page 12). Transceiver supply voltages cannot be changed from this controller.
3. For information on XADC see *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 1]

Using External Power Sources

Callout 18, Figure 1-2

Each voltage rail for the FPGA logic and GTX transceivers has an associated jack (or jacks) that can be used to provide power from an external source (Table 1-3). The jacks are binding posts that accept standard banana plugs.

Caution! Do **NOT** apply power to any of the FPGA logic power supply jacks without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.

Each onboard FPGA Logic regulator can be disabled by using its respective Power Regulation jumper (callout 17, Figure 1-2) shown in Table 1-3. A regulator is disabled by moving its Power Regulation jumper from POR_B to RESET.

Table 1-3: **FPGA Logic and GTX Transceiver Rails**

	Power Rail Net Name	External Supply Jack(s)	Power Regulation Jumper
FPGA Logic	VCCINT	J32, J178	J199
	VCCAUX	J33	J201
	VCCBRAM	J35	J200
	VCCAUX_IO	J34	J203
	VCCO_HP	J40	J202
	VCCO_HR	J196	J204
GTX Transceiver	MGTAVCC	J105	None(1)
	MGTAVTT	J106	None(1)
	MGTVCCAUX	J107	None(1)

Notes:

1. The GTX power module must be removed before providing external power to any of the transceiver rails (see 7 Series GTX Transceiver Power Module, page 13).

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Monitoring Voltage and Current

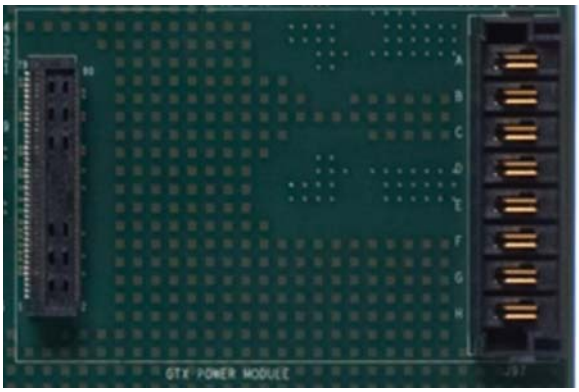
Voltage and current monitoring and control are available for FPGA logic and transceiver power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, and U11 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J26 (callout 20, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the VC7203 board are available from the Texas Instruments digital power website [Ref 2].

7 Series GTX Transceiver Power Module

The 7 series GTX transceiver power module (callout 19, Figure 1-2) supplies MGTAVCC, MGTAVTT and MGTVCCAUX voltages to the FPGA GTX transceivers. Three 7 series GTX power modules from third-party vendors are provided with the VC7203 board for evaluation. Any one of the three modules can be plugged into connectors J66 and J97 in the outlined and labeled power module location shown in Figure 1-4.



UG957_C1_04_100712

Figure 1-4: **Mounting Location, 7 Series GTX Transceiver Power Module**

Table 1-4 lists the nominal voltage values for the MGTAVCC, MGTAVTT and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by 7 series GTX modules included with the VC7203 board.

Table 1-4: **7 Series GTX Transceiver Power Module**

GTX Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.05V	12A
MGTAVTT	1.2V	8A
MGTVCCAUX	1.8V	2.6A

Each GTX transceiver rail comes with an associated jack that can be used to provide external power. These external supply jacks are shown in Table 1-3.

Caution! The 7 series GTX module **MUST** be removed when providing external power to the GTX transceiver rails.

Information about the 7 series GTX power supply modules included with the VC7203 kit is available from the vendor websites [Ref 3].

Active Heatsink Power Connector

Callout 22, Figure 1-2

An active heatsink (Figure 1-5) is provided for the FPGA. A 12V fan is affixed to the heatsink and is powered from the 3-pin friction lock header J121 (Figure 1-6).

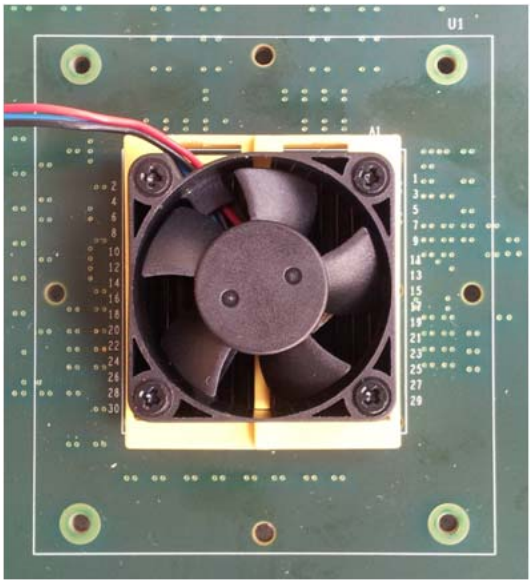


Figure 1-5: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-5:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-6 shows the heatsink fan power connector J121.

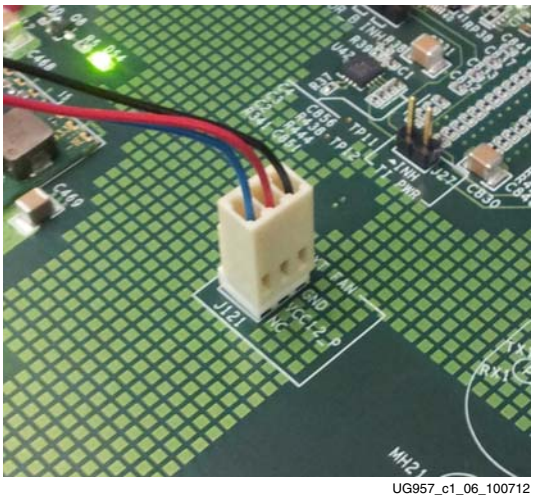


Figure 1-6: **Heatsink Fan Power Connector J121**

Virtex-7 FPGA

The VC7203 board is populated with the Virtex-7 XC7VX485T-3 FFG1761E FPGA at U1 (callout 1, Figure 1-2). For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 4].

FPGA Configuration

The FPGA is configured through JTAG using one of the following options:

- USB JTAG connector (callout 5, Figure 1-2)
- System ACE tool SD (callout 7, Figure 1-2)
- JTAG cable connector (callout 6, Figure 1-2)

The VC7203 board comes with an embedded USB-to-JTAG configuration module (U8) which allows a host computer to access the board JTAG chain using a Standard A to Micro-B USB cable. Alternately, the FPGA can be configured through the System ACE tool from an SD memory card installed in J211 (see System ACE Tool SD Configuration Address DIP Switches, page 17). Finally, a JTAG connector (J7) is available to provide access to the JTAG chain using one of the Xilinx configuration cables—Platform Cable USB, Platform Cable USB II, or Parallel Cable IV (PCIV).

The JTAG chain of the board is illustrated in Figure 1-7. By default only the Virtex-7 FPGA and the System ACE SD tool controller are part of the chain (J1 jumper OFF). Installing the J1 jumper adds the FMC interfaces as well.

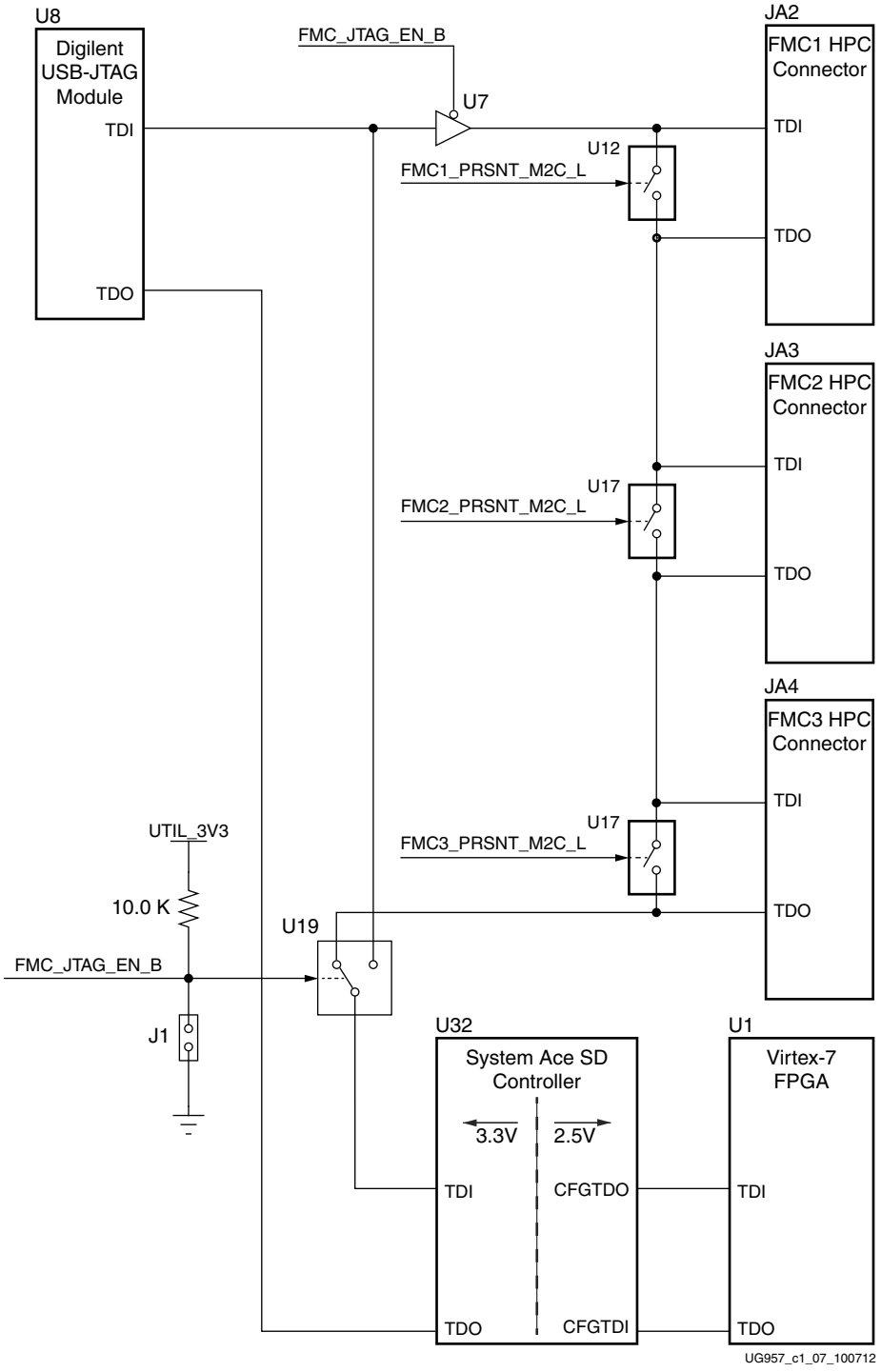


Figure 1-7: **JTAG Chain**

PROG_B Pushbutton

Pressing the PROG pushbutton SW3 (callout 14, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 12, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 13, Figure 1-2) indicates the FPGA initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE Tool SD Controller

The onboard System ACE tool SD controller U32 allows storage of multiple configuration files on an SD card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector J211 (callout 7, Figure 1-2) located directly below the System ACE SD controller on the back side of the board.

System ACE Tool SD Controller Reset

Pressing the SASD RESET pushbutton SW7 (callout 9, Figure 1-2) resets the System ACE tool SD controller. The reset pin is an active-Low input.

System ACE Tool SD Configuration Address DIP Switches

DIP switch SW8 shown in Figure 1-8 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW8 is shown in Figure 1-2 as callout 8.

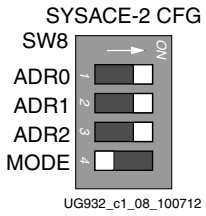


Figure 1-8: **Configuration Address DIP Switch (SW8)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW8 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 11, Figure 1-2).

The VC7203 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-7 lists the FPGA pin connections to the LVDS oscillator.

Table 1-7: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (U35)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
E19	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	200 MHz LVDS oscillator	Output
E18	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	201 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

Callout 30, Figure 1-2.

The VC7203 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-8.

Table 1-8: **Differential SMA Clock Connections**

FPGA (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	I/O Standard		
H19	USER CLOCK_1_P	Input	LVDS_25	CLK_DIFF_1_P	J99
G18	USER CLOCK_1_N	Input	LVDS_25	CLK_DIFF_1_N	J100
K39	USER CLOCK_2_P	Input	LVDS_25	CLK_DIFF_2_P	J98
K40	USER CLOCK_2_N	Input	LVDS_25	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 10, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the VC7203 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-9 shows the FPGA I/O mapping for the SuperClock-2 module interface. The VC7203 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HR input power to the clock module interface.

Table 1-9: **SuperClock-2 FPGA I/O Mapping**

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
E12	Clock Recovery	Input	LVDS_25	CM_LVDS1_P	1	Clock Recovery	Output
D12	Clock Recovery	Input	LVDS_25	CM_LVDS1_N	3	Clock Recovery	Output
L12	Clock Recovery	Input	LVDS_25	CM_LVDS2_P	9	Clock Recovery	Output
L11	Clock Recovery	Input	LVDS_25	CM_LVDS2_N	11	Clock Recovery	Output
BA1	Clock Recovery	Output	LVDS	CM_LVDS3_P	17	Clock Recovery	Input
BB1	Clock Recovery	Output	LVDS	CM_LVDS3_N	19	Clock Recovery	Input
K19	Regional Clock	Input	LVDS_25	CM_GCLK_P	25	Global Clock	Output
J18	Regional Clock	Input	LVDS_25	CM_GCLK_N	27	Global Clock	Output
C19	Control I/O	In/Out	LVCMOS18	CM_CTRL_0	61	NC	—
B19	Control I/O	In/Out	LVCMOS18	CM_CTRL_1	63	NC	—
A16	Control I/O	In/Out	LVCMOS18	CM_CTRL_2	65	NC	—
A15	Control I/O	Output	LVCMOS18	CM_CTRL_3	67	DEC	Input
A20	Control I/O	Output	LVCMOS18	CM_CTRL_4	69	INC	Input
A19	Control I/O	Output	LVCMOS18	CM_CTRL_5	71	ALIGN	Input
B17	Control I/O	In/Out	LVCMOS18	CM_CTRL_6	73	NC	—
A17	Control I/O	In/Out	LVCMOS18	CM_CTRL_7	75	NC	—
B21	Control I/O	In/Out	LVCMOS18	CM_CTRL_8	77	NC	—
A21	Control I/O	In/Out	LVCMOS18	CM_CTRL_9	79	LOL	
C18	Control I/O	Output	LVCMOS18	CM_CTRL_10	81	INT_ALRM	Input
B18	Control I/O	Output	LVCMOS18	CM_CTRL_11	83	C1B	Input
D20	Control I/O	Output	LVCMOS18	CM_CTRL_12	85	C2B	Input
C20	Control I/O	Output	LVCMOS18	CM_CTRL_13	87	C3B	Input
F17	Control I/O	Output	LVCMOS18	CM_CTRL_14	89	C1A	Input
E17	Control I/O	Output	LVCMOS18	CM_CTRL_15	91	C2A	Input
D21	Control I/O	In/Out	LVCMOS18	CM_CTRL_16	93	NC	—

Table 1-9: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
C21	Control I/O	Output	LVCMOS18	CM_CTRL_17	95	CS0_C3A	Input
D18	Control I/O	Output	LVCMOS18	CM_CTRL_18	97	CS1_C4A	Input
D17	Control I/O	In/Out	LVCMOS18	CM_CTRL_19	99	NC	—
F20	Control I/O	In/Out	LVCMOS18	CM_CTRL_20	101	NC	—
E20	Control I/O	In/Out	LVCMOS18	CM_CTRL_21	103	NC	—
K17	Control I/O	In/Out	LVCMOS18	CM_CTRL_22	105	NC	—
J17	Control I/O	In/Out	LVCMOS18	CM_CTRL_23	107	NC	—
J20	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active-High)

Callout 23, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-10 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-10: **User LEDs**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	I/O Standard		
M37	User LED	Output	LVCMOS18	APP_LED1	DS19
M38	User LED	Output	LVCMOS18	APP_LED2	DS20
R42	User LED	Output	LVCMOS18	APP_LED3	DS17
P42	User LED	Output	LVCMOS18	APP_LED4	DS18
N38	User LED	Output	LVCMOS18	APP_LED5	DS16
M39	User LED	Output	LVCMOS18	APP_LED6	DS15
R40	User LED	Output	LVCMOS18	APP_LED7	DS13
P40	User LED	Output	LVCMOS18	APP_LED8	DS14

User DIP Switches (Active-High) and I/O Header

Callout 25, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-11. These pins can be used to set control pins or any other purpose determined by the user. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 26, Figure 1-2.).

Table 1-11: **User DIP Switches**

FPGA (U1)				Schematic Net Name	SW2 DIP Switch Pin	J125 Test Header Pin
Pin	Function	Direction	I/O Standard			
E42	User Switch	Input	LVCMOS18	USER_SW1	1	2
C40	User Switch	Input	LVCMOS18	USER_SW2	2	4
C41	User Switch	Input	LVCMOS18	USER_SW3	3	6
H40	User Switch	Input	LVCMOS18	USER_SW4	4	8
H41	User Switch	Input	LVCMOS18	USER_SW5	5	10
H39	User Switch	Input	LVCMOS18	USER_SW6	6	12
G39	User Switch	Input	LVCMOS18	USER_SW7	7	—
G41	User Switch	Input	LVCMOS18	USER_SW8	8	—

Figure 1-9 shows the user test I/O connector J125 (callout 26, Figure 1-2).

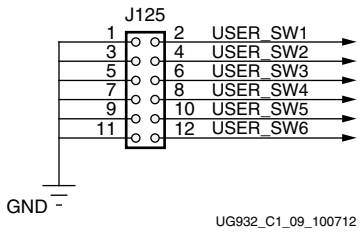


Figure 1-9: **User Test I/O**

User Pushbuttons (Active-High)

Callout 24, Figure 1-2.

SW4 and SW5 are active-High user pushbuttons that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switches can be used for any purpose determined by the user.

Table 1-12: **User Pushbuttons**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	I/O Standard		
P41	User Pushbutton	Input	LVCMOS18	USER_PB1	SW5
N41	User Pushbutton	Input	LVCMOS18	USER_PB2	SW4

GTX Transceivers and Reference Clocks

Callout 4, Figure 1-2.

The VC7203 board provides access to all GTX transceiver and reference clock pins on the FPGA as shown in Figure 1-10. The GTX transceivers are grouped into nine sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: QUAD 111 and QUAD 112 do not connect to pins on the XCVX485T.

Note: Figure 1-10 is for reference only and might not reflect the current revision of the board.

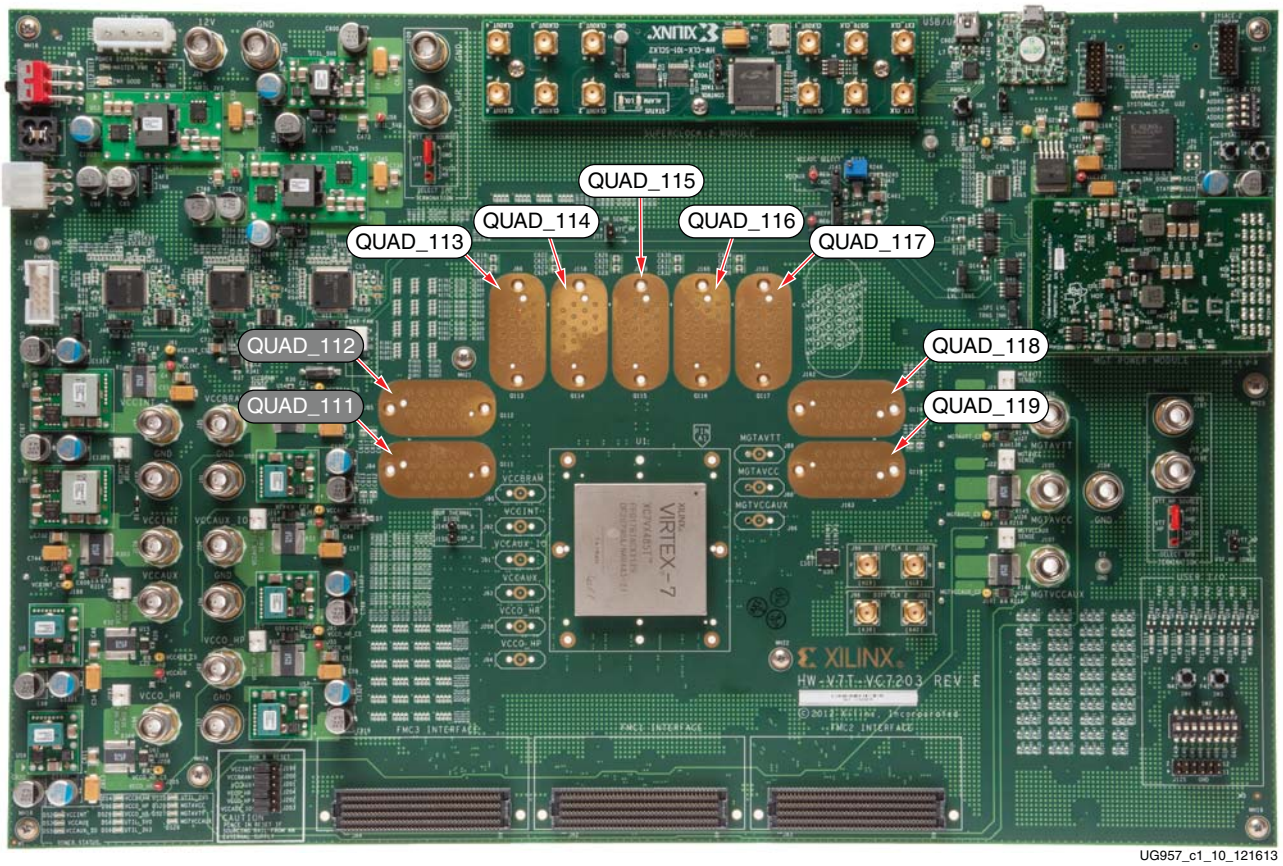


Figure 1-10: **GTX Quad Locations**

Each GTX Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about this or other cable assemblies. Figure 1-11 *A* shows the connector pad. Figure 1-11 *B* shows the connector pinout.

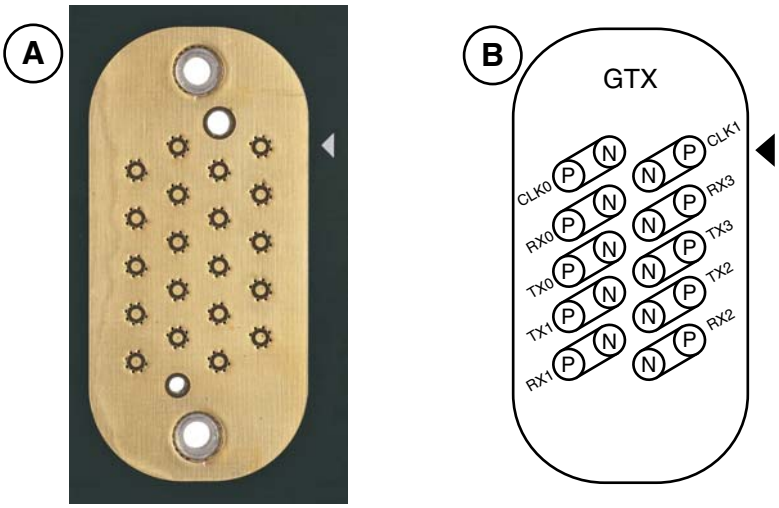


Figure 1-11: **A – GTX Connector Pad. B – GTX Connector Pinout**

Information for each GTX transceiver pin is shown in Table 1-13.

Table 1-13: **GTX Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
BB4	111_TX0_P	111	J84	1,929
BB3	111_TX0_N	111	J84	1,929
BB8	111_RX0_P	111	J84	2,149
BB7	111_RX0_N	111	J84	2,148
BA2	111_TX1_P	111	J84	1,808
BA1	111_TX1_N	111	J84	1,808
BA6	111_RX1_P	111	J84	1,855
BA5	111_RX1_N	111	J84	1,855
AY4	111_TX2_P	111	J84	2,097
AY3	111_TX2_N	111	J84	2,097
AY8	111_RX2_P	111	J84	2,101
AY7	111_RX2_N	111	J84	2,100
AW2	111_TX3_P	111	J84	2,650
AW1	111_TX3_N	111	J84	2,650
AW6	111_RX3_P	111	J84	2,533
AW5	111_RX3_N	111	J84	2,532
AV4	112_TX0_P	112	J85	2,692
AV3	112_TX0_N	112	J85	2,692

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AV8	112_RX0_P	112	J85	2,996
AV7	112_RX0_N	112	J85	2,996
AU2	112_TX1_P	112	J85	2,511
AU1	112_TX1_N	112	J85	2,511
AU6	112_RX1_P	112	J85	2,546
AU5	112_RX1_N	112	J85	2,545
AT4	112_TX2_P	112	J85	2,785
AT3	112_TX2_N	112	J85	2,785
AR6	112_RX2_P	112	J85	2,803
AR5	112_RX2_N	112	J85	2,803
AR2	112_TX3_P	112	J85	3,385
AR1	112_TX3_N	112	J85	3,385
AP8	112_RX3_P	112	J85	3,365
AP7	112_RX3_N	112	J85	3,365
AP4	113_TX0_P	113	J86	2,949
AP3	113_TX0_N	113	J86	2,949
AN6	113_RX0_P	113	J86	3,243
AN5	113_RX0_N	113	J86	3,243
AN2	113_TX1_P	113	J86	2,736
AN1	113_TX1_N	113	J86	2,736
AM8	113_RX1_P	113	J86	2,822
AM7	113_RX1_N	113	J86	2,822
AM4	113_TX2_P	113	J86	2,736
AM3	113_TX2_N	113	J86	2,736
AL6	113_RX2_P	113	J86	2,455
AL5	113_RX2_N	113	J86	2,455
AL2	113_TX3_P	113	J86	2,812
AL1	113_TX3_N	113	J86	2,812
AJ6	113_RX3_P	113	J86	2,892
AJ5	113_RX3_N	113	J86	2,892
AK4	114_TX0_P	114	J158	2,430
AK3	114_TX0_N	114	J158	2,430

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AG6	114_RX0_P	114	J158	2,715
AG5	114_RX0_N	114	J158	2,714
AJ2	114_TX1_P	114	J158	2,180
AJ1	114_TX1_N	114	J158	2,180
AF4	114_RX1_P	114	J158	2,181
AF3	114_RX1_N	114	J158	2,181
AH4	114_TX2_P	114	J158	2,207
AH3	114_TX2_N	114	J158	2,207
AE6	114_RX2_P	114	J158	2,160
AE5	114_RX2_N	114	J158	2,160
AG2	114_TX3_P	114	J158	2,570
AG1	114_TX3_N	114	J158	2,571
AD4	114_RX3_P	114	J158	2,570
AD3	114_RX3_N	114	J158	2,570
Y2	115_TX0_P	115	J83	2,805
Y1	115_TX0_N	115	J83	2,806
AA4	115_RX0_P	115	J83	2,898
AA3	115_RX0_N	115	J83	2,898
V2	115_TX1_P	115	J83	2,525
V1	115_TX1_N	115	J83	2,523
Y6	115_RX1_P	115	J83	2,489
Y5	115_RX1_N	115	J83	2,489
U4	115_TX2_P	115	J83	2,549
U3	115_TX2_N	115	J83	2,549
W4	115_RX2_P	115	J83	2,308
W3	115_RX2_N	115	J83	2,309
T2	115_TX3_P	115	J83	2,840
T1	115_TX3_N	115	J83	2,840
V6	115_RX3_P	115	J83	2,933
V5	115_RX3_N	115	J83	2,933
P2	116_TX0_P	116	J84	2,677
P1	116_TX0_N	116	J84	2,677

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
T6	116_RX0_P	116	J84	2,667
T5	116_RX0_N	116	J84	2,668
N4	116_TX1_P	116	J84	2,469
N3	116_TX1_N	116	J84	2,469
R4	116_RX1_P	116	J84	2,207
R3	116_RX1_N	116	J84	2,207
M2	116_TX2_P	116	J84	2,359
M1	116_TX2_N	116	J84	2,357
P6	116_RX2_P	116	J84	2,218
P5	116_RX2_N	116	J84	2,218
L4	116_TX3_P	116	J84	2,555
L3	116_TX3_N	116	J84	2,555
M6	116_RX3_P	116	J84	2,821
M5	116_RX3_N	116	J84	2,821
K2	117_TX0_P	117	J85	2,617
K1	117_TX0_N	117	J85	2,616
K6	117_RX0_P	117	J85	2,886
K5	117_RX0_N	117	J85	2,886
J4	117_TX1_P	117	J85	2,400
J3	117_TX1_N	117	J85	2,401
H6	117_RX1_P	117	J85	2,337
H5	117_RX1_N	117	J85	2,337
H2	117_TX2_P	117	J85	2,635
H1	117_TX2_N	117	J85	2,634
G4	117_RX2_P	117	J85	2,349
G3	117_RX2_N	117	J85	2,349
F2	117_TX3_P	117	J85	2,823
F1	117_TX3_N	117	J85	2,823
F6	117_RX3_P	117	J85	2,873
F5	117_RX3_N	117	J85	2,872
D2	118_TX0_P	118	J86	2,842
D1	118_TX0_N	118	J86	2,844

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
E4	118_RX0_P	118	J86	3,048
E3	118_RX0_N	118	J86	3,049
C4	118_TX1_P	118	J86	2,629
C3	118_TX1_N	118	J86	2,628
D6	118_RX1_P	118	J86	2,597
D5	118_RX1_N	118	J86	2,597
B2	118_TX2_P	118	J86	2,787
B1	118_TX2_N	118	J86	2,789
B6	118_RX2_P	118	J86	2,681
B5	118_RX2_N	118	J86	2,680
A4	118_TX3_P	118	J86	3,044
A3	118_TX3_N	118	J86	3,044
A8	118_RX3_P	118	J86	3,515
A7	118_RX3_N	118	J86	3,515
E2	119_TX0_P	119	J163	2,570
E1	119_TX0_N	119	J163	2,570
D8	119_RX0_P	119	J163	2,677
D7	119_RX0_N	119	J163	2,677
D4	119_TX1_P	119	J163	2,176
D3	119_TX1_N	119	J163	2,177
C6	119_RX1_P	119	J163	2,068
C5	119_RX1_N	119	J163	2,067
C2	119_TX2_P	119	J163	1,974
C1	119_TX2_N	119	J163	1,974
B8	119_RX2_P	119	J163	1,775
B7	119_RX2_N	119	J163	1,774
B4	119_TX3_P	119	J163	2,039
B3	119_TX3_N	119	J163	2,039
A6	119_RX3_P	119	J163	2,339
A5	119_RX3_N	119	J163	2,339

Information for each GTX transceiver clock input is shown in Table 1-14.

Table 1-14: **GTX Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
AW10	111_REFCLK0_P	111	J84
AW9	111_REFCLK0_N	111	J84
BA10	111_REFCLK1_P	111	J84
BA9	111_REFCLK1_N	111	J84
AT8	112_REFCLK0_P	112	J85
AT7	112_REFCLK0_N	112	J85
AU10	112_REFCLK1_P	112	J85
AU9	112_REFCLK1_N	112	J85
AH8	113_REFCLK0_P	113	J86
AH7	113_REFCLK0_N	113	J86
AK7	113_REFCLK1_N	113	J86
AK8	113_REFCLK1_P	113	J86
AD8	114_REFCLK0_P	114	J158
AD7	114_REFCLK0_N	114	J158
AF8	114_REFCLK1_P	114	J158
AF7	114_REFCLK1_N	114	J158
R8	115_REFCLK0_P	115	J83
R7	115_REFCLK0_N	115	J83
U8	115_REFCLK1_P	115	J83
U7	115_REFCLK1_N	115	J83
L8	116_REFCLK0_P	116	J84
L7	116_REFCLK0_N	116	J84
N8	116_REFCLK1_P	116	J84
N7	116_REFCLK1_N	116	J84
G8	117_REFCLK0_P	117	J85
G7	117_REFCLK0_N	117	J85
J8	117_REFCLK1_P	117	J85
J7	117_REFCLK1_N	117	J85
C8	118_REFCLK0_P	118	J86
C7	118_REFCLK0_N	118	J86
E8	118_REFCLK1_P	118	J86
E7	118_REFCLK1_N	118	J86

Table 1-14: **GTX Transceiver Reference Clock Inputs *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector
A10	119_REFCLK0_P	119	J163
A9	119_REFCLK0_N	119	J163
C10	119_REFCLK1_P	119	J163
C9	119_REFCLK1_N	119	J163

USB-to-UART Bridge

Callout 21, Figure 1-2.

A USB-to-UART bridge (U34, Silicon Laboratories CP2103) is provided for serial communication between a host computer and the FPGA over a USB cable. The USB connector on the board is a mini-B receptacle (J79) and its pinout is shown in Table 1-15.

Table 1-15: **USB Mini-B Receptacle Pin Assignments and Signals**

J79 Pin	Signal Name	Description
1	VBUS	+5V into the CP2103 USB-to-UART bridge at U34. Used to sense USB network connection.
2	USB_DATA_N	Bidirectional differential serial data (N-side).
3	USB_DATA_P	Bidirectional differential serial data (P-side).
4	GROUND	Signal ground.

The CP2103 supports an I/O voltage range of 1.8V to 3.3V. Xilinx UART IP is expected to be implemented in the FPGA fabric. The FPGA supports the USB-to-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 are listed in Table 1-16.

Table 1-16: **FPGA to UART Connections**

FPGA (U1)				Schematic Net Name	Device (U34)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
B31	RTS	Output	LVCMOS18	USB_CTS_I_B	22	CTS	Input
C31	CTS	Input	LVCMOS18	USB_RTS_0_B	23	RTS	Output
A30	TX	Output	LVCMOS18	USB_RXD_I	24	RXD	Input
A29	RX	Input	LVCMOS18	USB_TXD_0	25	TXD	Output

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information (Table 1-17).

Table 1-17: **CP2103 USB-to-UART Bridge User GPIO**

FPGA (U1)				Schematic Net Name	Device (U34)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
B28	SelectIO	In/Out	LVCMOS18	USB_GPIO_0	19	GPIO	In/Out
B29	SelectIO	In/Out	LVCMOS18	USB_GPIO_1	18	GPIO	In/Out
A31	SelectIO	In/Out	LVCMOS18	USB_GPIO_2	17	GPIO	In/Out
A32	SelectIO	In/Out	LVCMOS18	USB_GPIO_3	16	GPIO	In/Out

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB-to-UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the VC7203 board.

FPGA Mezzanine Card HPC Interface

Callout 27, 28, and 29, Figure 1-2.

The VC7203 board features three high pin count (HPC) connectors as defined by the VITA 57.1 FPGA Mezzanine card (FMC) specification. The FMC HPC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates.

FMC1 HPC connector JA2 provides connectivity for:

- 68 differential user defined pairs:
  - 34 LA pairs
  - 17 HA pairs
  - 17 HB pairs
- 4 differential clocks

FMC2 HPC connector JA3 provides connectivity for:

- 68 differential user defined pairs:
  - 34 LA pairs
  - 17 HA pairs
  - 17 HB pairs
- 4 differential clocks

FMC3 HPC connector JA4 provides connectivity for:

- 65 differential user defined pairs:
  - 34 LA pairs
  - 16 HA pairs
  - 15 HB pairs
- 4 differential clocks

Note: FMC3 is not supported by the XC7VX485T device. The I/O banks that connect to FMC3 are not available in this device.

Note: The V_{ADJ} voltage on the three FMC HPC connectors tracks VCCO_HP.

The FMC HPC connectors on the VC7203 board are identified as FMC1 at JA2, FMC2 at JA3 and FMC3 at JA4. The connections for each of these connectors are listed in Table 1-18 and Table 1-19, page 35 respectively.

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
AJ32	FMC1_CLK0_M2C_P	H4
AK32	FMC1_CLK0_M2C_N	H5
AL31	FMC1_CLK1_M2C_P	G2
AL32	FMC1_CLK1_M2C_N	G3
AD32	FMC1_CLK2_BIDIR_P	K4
AD33	FMC1_CLK2_BIDIR_N	K5
AC34	FMC1_CLK3_BIDIR_P	J2
AD35	FMC1_CLK3_BIDIR_N	J3
AV40	FMC1_HA00_CC_P	F4
AW40	FMC1_HA00_CC_N	F5
AY39	FMC1_HA01_CC_P	E2
AY40	FMC1_HA01_CC_N	E3
AT41	FMC1_HA02_P	K7
AU42	FMC1_HA02_N	K8
AY42	FMC1_HA03_P	J6
BA42	FMC1_HA03_N	J7
AU41	FMC1_HA04_P	F7
AV41	FMC1_HA04_N	F8
BA41	FMC1_HA05_P	E6
BB41	FMC1_HA05_N	E7
AW41	FMC1_HA06_P	K10
AW42	FMC1_HA06_N	K11
AJ30	FMC1_HA07_P	J9
AK30	FMC1_HA07_N	J10
AF29	FMC1_HA08_P	F10
AG29	FMC1_HA08_N	F11
AK28	FMC1_HA09_P	E9
AK29	FMC1_HA09_N	E10

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AF30	FMC1_HA10_P	K13
AG31	FMC1_HA10_N	K14
AH28	FMC1_HA11_P	J12
AJ28	FMC1_HA11_N	J13
AC31	FMC1_HA12_P	F13
AD31	FMC1_HA12_N	F14
AA31	FMC1_HA13_P	E12
AA32	FMC1_HA13_N	E13
AC30	FMC1_HA14_P	J15
AD30	FMC1_HA14_N	J16
AA29	FMC1_HA15_P	F16
AA30	FMC1_HA15_N	F17
AB29	FMC1_HA16_P	E15
AC29	FMC1_HA16_N	E16
AB33	FMC1_HB00_CC_P	K25
AC33	FMC1_HB00_CC_N	K26
AF35	FMC1_HB01_P	J24
AF36	FMC1_HB01_N	J25
AE37	FMC1_HB02_P	F22
AF37	FMC1_HB02_N	F23
AF34	FMC1_HB03_P	E21
AG34	FMC1_HB03_N	E22
AD36	FMC1_HB04_P	F25
AD37	FMC1_HB04_N	F26
AC35	FMC1_HB05_P	E24
AC36	FMC1_HB05_N	E25
AB31	FMC1_HB06_CC_P	K28
AB32	FMC1_HB06_CC_N	K29
AG36	FMC1_HB07_P	J27
AH36	FMC1_HB07_N	J28
Y37	FMC1_HB08_P	F28
AA37	FMC1_HB08_N	F29
Y35	FMC1_HB09_P	E27

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AA36	FMC1_HB09_N	E28
AB36	FMC1_HB10_P	K31
AB37	FMC1_HB10_N	K32
AA34	FMC1_HB11_P	J30
AA35	FMC1_HB11_N	J31
AE32	FMC1_HB12_P	F31
AE33	FMC1_HB12_N	F32
AF31	FMC1_HB13_P	E30
AF32	FMC1_HB13_N	E31
AE34	FMC1_HB14_P	K34
AE35	FMC1_HB14_N	K35
AE29	FMC1_HB15_P	J33
AE30	FMC1_HB15_N	J34
Y32	FMC1_HB16_P	F34
Y33	FMC1_HB16_N	F35
AU38	FMC1_LA00_CC_P	G6
AV38	FMC1_LA00_CC_N	G7
AU39	FMC1_LA01_CC_P	D8
AV39	FMC1_LA01_CC_N	D9
AN38	FMC1_LA02_P	H7
AP38	FMC1_LA02_N	H8
AM41	FMC1_LA03_P	G9
AM42	FMC1_LA03_N	G10
AR38	FMC1_LA04_P	H10
AR39	FMC1_LA04_N	H11
AN40	FMC1_LA05_P	D11
AN41	FMC1_LA05_N	D12
AR37	FMC1_LA06_P	C10
AT37	FMC1_LA06_N	C11
AM39	FMC1_LA07_P	H13
AN39	FMC1_LA07_N	H14
AP40	FMC1_LA08_P	G12
AR40	FMC1_LA08_N	G13

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AP41	FMC1_LA09_P	D14
AP42	FMC1_LA09_N	D15
AT39	FMC1_LA10_P	C14
AT40	FMC1_LA10_N	C15
AR42	FMC1_LA11_P	H16
AT42	FMC1_LA11_N	H17
AW37	FMC1_LA12_P	G15
AY37	FMC1_LA12_N	G16
BA37	FMC1_LA13_P	D17
BB37	FMC1_LA13_N	D18
AW38	FMC1_LA14_P	C18
AY38	FMC1_LA14_N	C19
BB38	FMC1_LA15_P	H19
BB39	FMC1_LA15_N	H20
BA39	FMC1_LA16_P	G18
BA40	FMC1_LA16_N	G19
AK34	FMC1_LA17_CC_P	D20
AL34	FMC1_LA17_CC_N	D21
AJ33	FMC1_LA18_CC_P	C22
AK33	FMC1_LA18_CC_N	C23
AM36	FMC1_LA19_P	H22
AN36	FMC1_LA19_N	H23
AJ36	FMC1_LA20_P	G21
AJ37	FMC1_LA20_N	G22
AP36	FMC1_LA21_P	H25
AP37	FMC1_LA21_N	H26
AK37	FMC1_LA22_P	G24
AL37	FMC1_LA22_N	G25
AN35	FMC1_LA23_P	D23
AP35	FMC1_LA23_N	D24
AL36	FMC1_LA24_P	H28
AM37	FMC1_LA24_N	H29
AG33	FMC1_LA25_P	G27

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AH33	FMC1_LA25_N	G28
AK35	FMC1_LA26_P	D26
AL35	FMC1_LA26_N	D27
AH31	FMC1_LA27_P	C26
AJ31	FMC1_LA27_N	C27
AH34	FMC1_LA28_P	H31
AJ35	FMC1_LA28_N	H32
AM34	FMC1_LA29_P	G30
AN34	FMC1_LA29_N	G31
AM31	FMC1_LA30_P	H34
AM32	FMC1_LA30_N	H35
AM33	FMC1_LA31_P	G33
AN33	FMC1_LA31_N	G34
AL29	FMC1_LA32_P	H37
AL30	FMC1_LA32_N	H38
AH29	FMC1_LA33_P	G36
AH30	FMC1_LA33_N	G37
AM38	FMC1_PRSNT_M2C_L	H2

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
E34	FMC2_CLK0_M2C_P	H4
E35	FMC2_CLK0_M2C_N	H5
D37	FMC2_CLK1_M2C_P	G2
D38	FMC2_CLK1_M2C_N	G3
M24	FMC2_CLK2_BIDIR_P	K4
L24	FMC2_CLK2_BIDIR_N	K5
K23	FMC2_CLK3_BIDIR_P	J2
J23	FMC2_CLK3_BIDIR_N	J3
N30	FMC2_HA00_CC_P	F4
M31	FMC2_HA00_CC_N	F5
P30	FMC2_HA01_CC_P	E2
N31	FMC2_HA01_CC_N	E3

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
V30	FMC2_HA02_P	K7
V31	FMC2_HA02_N	K8
T29	FMC2_HA03_P	J6
T30	FMC2_HA03_N	J7
W30	FMC2_HA04_P	F7
W31	FMC2_HA04_N	F8
V29	FMC2_HA05_P	E6
U29	FMC2_HA05_N	E7
Y29	FMC2_HA06_P	K10
Y30	FMC2_HA06_N	K11
G36	FMC2_HA07_P	J9
G37	FMC2_HA07_N	J10
F39	FMC2_HA08_P	F10
E39	FMC2_HA08_N	F11
J37	FMC2_HA09_P	E9
J38	FMC2_HA09_N	E10
H38	FMC2_HA10_P	K13
G38	FMC2_HA10_N	K14
J36	FMC2_HA11_P	J12
H36	FMC2_HA11_N	J13
P25	FMC2_HA12_P	F13
P26	FMC2_HA12_N	F14
P22	FMC2_HA13_P	E12
P23	FMC2_HA13_N	E13
N25	FMC2_HA14_P	J15
N26	FMC2_HA14_N	J16
N23	FMC2_HA15_P	F16
N24	FMC2_HA15_N	F17
M27	FMC2_HA16_P	E15
L27	FMC2_HA16_N	E16
J25	FMC2_HB00_CC_P	K25
J26	FMC2_HB00_CC_N	K26
H24	FMC2_HB01_P	J24

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
G24	FMC2_HB01_N	J25
J21	FMC2_HB02_P	F22
H21	FMC2_HB02_N	F23
H25	FMC2_HB03_P	E21
H26	FMC2_HB03_N	E22
G21	FMC2_HB04_P	F25
G22	FMC2_HB04_N	F26
G26	FMC2_HB05_P	E24
G27	FMC2_HB05_N	E25
K24	FMC2_HB06_CC_P	K28
K25	FMC2_HB06_CC_N	K29
H23	FMC2_HB07_P	J27
G23	FMC2_HB07_N	J28
G28	FMC2_HB08_P	F28
G29	FMC2_HB08_N	F29
K28	FMC2_HB09_P	E27
J28	FMC2_HB09_N	E28
H28	FMC2_HB10_P	K31
H29	FMC2_HB10_N	K32
K27	FMC2_HB11_P	J30
J27	FMC2_HB11_N	J31
M22	FMC2_HB12_P	F31
L22	FMC2_HB12_N	F32
L25	FMC2_HB13_P	E30
L26	FMC2_HB13_N	E31
K22	FMC2_HB14_P	K34
J22	FMC2_HB14_N	K35
M21	FMC2_HB15_P	J33
L21	FMC2_HB15_N	J34
P21	FMC2_HB16_P	F34
N21	FMC2_HB16_N	F35
L31	FMC2_LA00_CC_P	G6
K32	FMC2_LA00_CC_N	G7

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
M32	FMC2_LA01_CC_P	D8
L32	FMC2_LA01_CC_N	D9
K35	FMC2_LA02_P	H7
J35	FMC2_LA02_N	H8
J32	FMC2_LA03_P	G9
J33	FMC2_LA03_N	G10
K33	FMC2_LA04_P	H10
K34	FMC2_LA04_N	H11
L34	FMC2_LA05_P	D11
L35	FMC2_LA05_N	D12
M33	FMC2_LA06_P	C10
M34	FMC2_LA06_N	C11
H34	FMC2_LA07_P	H13
H35	FMC2_LA07_N	H14
K29	FMC2_LA08_P	G12
K30	FMC2_LA08_N	G13
J30	FMC2_LA09_P	D14
H30	FMC2_LA09_N	D15
L29	FMC2_LA10_P	C14
L30	FMC2_LA10_N	C15
J31	FMC2_LA11_P	H16
H31	FMC2_LA11_N	H17
M28	FMC2_LA12_P	G15
M29	FMC2_LA12_N	G16
R28	FMC2_LA13_P	D17
P28	FMC2_LA13_N	D18
N28	FMC2_LA14_P	C18
N29	FMC2_LA14_N	C19
R30	FMC2_LA15_P	H19
P31	FMC2_LA15_N	H20
U31	FMC2_LA16_P	G18
T31	FMC2_LA16_N	G19
C35	FMC2_LA17_CC_P	D20

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
C36	FMC2_LA17_CC_N	D21
D35	FMC2_LA18_CC_P	C22
D36	FMC2_LA18_CC_N	C23
B36	FMC2_LA19_P	H22
A37	FMC2_LA19_N	H23
B34	FMC2_LA20_P	G21
A34	FMC2_LA20_N	G22
B39	FMC2_LA21_P	H25
A39	FMC2_LA21_N	H26
A35	FMC2_LA22_P	G24
A36	FMC2_LA22_N	G25
C38	FMC2_LA23_P	D23
C39	FMC2_LA23_N	D24
B37	FMC2_LA24_P	H28
B38	FMC2_LA24_N	H29
E32	FMC2_LA25_P	G27
D32	FMC2_LA25_N	G28
B32	FMC2_LA26_P	D26
B33	FMC2_LA26_N	D27
E33	FMC2_LA27_P	C26
D33	FMC2_LA27_N	C27
C33	FMC2_LA28_P	H31
C34	FMC2_LA28_N	H32
G32	FMC2_LA29_P	G30
F32	FMC2_LA29_N	G31
F36	FMC2_LA30_P	H34
F37	FMC2_LA30_N	H35
F34	FMC2_LA31_P	G33
F35	FMC2_LA31_N	G34
H33	FMC2_LA32_P	H37
G33	FMC2_LA32_N	H38
E37	FMC2_LA33_P	G36

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
E38	FMC2_LA33_N	G37
G31	FMC2_PRSNT_M2C_L	H2

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4**

U1 FPGA Pin	Net Name	FMC Pin
AY18	FMC3_CLK0_M2C_P	H4
AY17	FMC3_CLK0_M2C_N	H5
AW18	FMC3_CLK1_M2C_P	G2
AW17	FMC3_CLK1_M2C_N	G3
H15	FMC3_CLK2_BIDIR_P	K4
H14	FMC3_CLK2_BIDIR_N	K5
J13	FMC3_CLK3_BIDIR_P	J2
H13	FMC3_CLK3_BIDIR_N	J3
AU14	FMC3_HA00_CC_P	F4
AU13	FMC3_HA00_CC_N	F5
AV13	FMC3_HA01_CC_P	E2
AW13	FMC3_HA01_CC_N	E3
AW12	FMC3_HA02_P	K7
AY12	FMC3_HA02_N	K8
BA15	FMC3_HA03_P	J6
BA14	FMC3_HA03_N	J7
AY14	FMC3_HA04_P	F7
AY13	FMC3_HA04_N	F8
BB14	FMC3_HA05_P	E6
BB13	FMC3_HA05_N	E7
AV20	FMC3_HA06_P	K10
AW20	FMC3_HA06_N	K11
BA17	FMC3_HA07_P	J9
BB17	FMC3_HA07_N	J10
AY20	FMC3_HA08_P	F10
BA20	FMC3_HA08_N	F11
BA16	FMC3_HA09_P	E9
BB16	FMC3_HA09_N	E10

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AY19	FMC3_HA10_P	K13
BA19	FMC3_HA10_N	K14
C16	FMC3_HA11_P	J12
B16	FMC3_HA11_N	J13
B14	FMC3_HA12_P	F13
A14	FMC3_HA12_N	F14
C15	FMC3_HA13_P	E12
C14	FMC3_HA13_N	E13
D13	FMC3_HA14_P	J15
C13	FMC3_HA14_N	J16
D16	FMC3_HA15_P	F16
D15	FMC3_HA15_N	F17
G14	FMC3_HB00_CC_P	K25
G13	FMC3_HB00_CC_N	K26
F16	FMC3_HB01_P	J24
E15	FMC3_HB01_N	J25
E14	FMC3_HB02_P	F22
E13	FMC3_HB02_N	F23
H16	FMC3_HB03_P	E21
G16	FMC3_HB03_N	E22
G12	FMC3_HB04_P	F25
F12	FMC3_HB04_N	F26
K12	FMC3_HB05_P	E24
J12	FMC3_HB05_N	E25
F15	FMC3_HB06_CC_P	K28
F14	FMC3_HB06_CC_N	K29
K15	FMC3_HB07_P	J27
J15	FMC3_HB07_N	J28
K14	FMC3_HB08_P	F28
K13	FMC3_HB08_N	F29
L16	FMC3_HB09_P	E27
L15	FMC3_HB09_N	E28
M14	FMC3_HB10_P	K31

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
L14	FMC3_HB10_N	K32
N16	FMC3_HB11_P	J30
M16	FMC3_HB11_N	J31
N13	FMC3_HB12_P	F31
M13	FMC3_HB12_N	F32
N15	FMC3_HB13_P	E30
N14	FMC3_HB13_N	E31
M12	FMC3_HB14_P	K34
M11	FMC3_HB14_N	K35
AP13	FMC3_LA00_CC_P	G6
AR13	FMC3_LA00_CC_N	G7
AR14	FMC3_LA01_CC_P	D8
AT14	FMC3_LA01_CC_N	D9
AJ16	FMC3_LA02_P	H7
AJ15	FMC3_LA02_N	H8
AK14	FMC3_LA03_P	G9
AK13	FMC3_LA03_N	G10
AK15	FMC3_LA04_P	H10
AL14	FMC3_LA04_N	H11
AJ13	FMC3_LA05_P	D11
AJ12	FMC3_LA05_N	D12
AL16	FMC3_LA06_P	C10
AL15	FMC3_LA06_N	C11
AK12	FMC3_LA07_P	H13
AL12	FMC3_LA07_N	H14
AM13	FMC3_LA08_P	G12
AN13	FMC3_LA08_N	G13
AM12	FMC3_LA09_P	D14
AM11	FMC3_LA09_N	D15
AN15	FMC3_LA10_P	C14
AN14	FMC3_LA10_N	C15
AN11	FMC3_LA11_P	H16
AP11	FMC3_LA11_N	H17

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AP12	FMC3_LA12_P	G15
AR12	FMC3_LA12_N	G16
AR15	FMC3_LA13_P	D17
AT15	FMC3_LA13_N	D18
AT12	FMC3_LA14_P	C18
AU12	FMC3_LA14_N	C19
AV15	FMC3_LA15_P	H19
AV14	FMC3_LA15_N	H20
AW15	FMC3_LA16_P	G18
AY15	FMC3_LA16_N	G19
AT17	FMC3_LA17_CC_P	D20
AU17	FMC3_LA17_CC_N	D21
AU18	FMC3_LA18_CC_P	C22
AV18	FMC3_LA18_CC_N	C23
AL19	FMC3_LA19_P	H22
AM19	FMC3_LA19_N	H23
AK17	FMC3_LA20_P	G21
AL17	FMC3_LA20_N	G22
AM18	FMC3_LA21_P	H25
AM17	FMC3_LA21_N	H26
AK19	FMC3_LA22_P	G24
AK18	FMC3_LA22_N	G25
AM16	FMC3_LA23_P	D23
AN16	FMC3_LA23_N	D24
AJ18	FMC3_LA24_P	H28
AJ17	FMC3_LA24_N	H29
AP18	FMC3_LA25_P	G27
AP17	FMC3_LA25_N	G28
AP20	FMC3_LA26_P	D26
AR19	FMC3_LA26_N	D27
AN19	FMC3_LA27_P	C26
AN18	FMC3_LA27_N	C27
AR18	FMC3_LA28_P	H31

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AR17	FMC3_LA28_N	H32
AU19	FMC3_LA29_P	G30
AV19	FMC3_LA29_N	G31
AT20	FMC3_LA30_P	H34
AT19	FMC3_LA30_N	H35
AV16	FMC3_LA31_P	G33
AW16	FMC3_LA31_N	G34
AT16	FMC3_LA32_P	H37
AU16	FMC3_LA32_N	H38
BB19	FMC3_LA33_P	G36
BB18	FMC3_LA33_N	G37
AR20	FMC3_PRSNT_M2C_L	H2

XADC

Callout 31, Figure 1-2.

7 series FPGAs provide an Analog Front End (XADC) block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors. See *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 1] for details on the capabilities of the analog front end.

The VC7203 board provides two options for providing power (VCCADC) to the analog circuitry in the XADC. Either option can be selected by placing a shunt in one of two positions on the 3-pin VCCADC SELECT header, J141 (callout 31, Figure 1-2):

- **Pins 1-2 (VCCAUX):** In this configuration VCCADC is provided from VCCAUX through a low pass filter network.
- **Pin 2-3 (REG):** In this configuration VCCADC is provided by an onboard regulator, U43 (Analog Devices P/N ADP123AUJZ-R7). The output voltage of the regulator VCCADC can be adjusted using the potentiometer R233.

In addition, the VC7203 board provides two options for providing the reference voltage for the analog-to-digital converter. Either option can be selected by placing a shunt in one of two positions on the 3-pin VREF SEL header J142 (callout 31, Figure 1-2):

- **Pins 1-2 (REG):** In this configuration the ADC reference voltage is provided by an onboard, low-temperature coefficient 1.25V reference, U45 (Texas Instruments P/N REF3012AIDBZT)
- **Pin 2-3 (AGND):** In this configuration the VREFP on XADC is connected to analog ground and the ADC uses an on-chip reference.

I2C Bus Management

The I^{2}C bus is controlled through U39, an 8-channel I^{2}C-bus multiplexer (NXP Semiconductor PCA9547). The FPGA communicates with the multiplexer through I^{2}C data and clock signals mapped to FPGA pins E21 and F21, respectively. The I^{2}C idcode for the PCA9547 device is `0x70`. The bus hosts four components:

- SuperClock-2 module
- 7 series GTX transceiver power supply module
- FMC1
- FMC2
- FMC3

An I^{2}C component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-21.

Table 1-21: **I^{2}C Channel Assignments**

U39 Channel	I^{2}C Component
0	SuperClock-2 module
1	7 series GTX transceiver power supply module
2	FMC1
3	FMC2
7	FMC3

XILINX

Appendix A

Default Jumper Settings

Table A-1 lists the jumpers that must be installed on the VC7203 board for proper operation. These jumpers must be installed except where specifically noted in this user guide.

Note: Any jumper not listed in Table A-1 should be left open for normal operation.

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper	Comments
J4	UTIL_3V3	Upper Left	AFX (1-2)	
J184	UTIL_2V5	Upper Left	AFX (1-2)	
J24	UTIL_5V0	Upper Left	AFX (1-2)	
J78	VTT_HR SOURCE	Upper Left	GND (1-2)	Red 20A jumper
J210	PMBUS CTRL	Upper Left	GND (2-3)	
J48		Upper Left	POR (1-2)	
J49		Upper Left	POR (1-2)	
J50		Upper Left	POR (1-2)	
J199	VCCINT	Lower Left	POR_B (1-2)	
J200	VCCBRAM	Lower Left	POR_B (1-2)	
J201	VCCAUX	Lower Left	POR_B (1-2)	
J204	VCCO_HR	Lower Left	POR_B (1-2)	
J202	VCCO_HP	Lower Left	POR_B (1-2)	
J203	VCCAUX_IO	Lower Left	POR_B (1-2)	
J141	VCCADC SELECT	Upper Center	VCCAUX (1-2)	
J142	VREF SEL	Upper Center	REG (1-2)	
J23	SPI LVL TRNS INH	Upper Right	Installed	
J195	VTT_HP SOURCE	Center Right	GND (1-2)	Red 20A jumper

VITA 57.1 FMC Connector Pinouts

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG957_ac_01_100712

Figure B-1: **FMC HPC Connector Pinout**

XILINX

Appendix C

Master Constraints File Listing

The master Xilinx design constraints (XDC) file template for the VC7203 board provides for designs targeting the VC7203 Virtex®-7 FPGA GTX Transceiver Characterization Board. Net names in the listed constraints correlate with net names on the VC7203 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 5] for more information.

Note: Visit the Virtex-7 FPGA VC7203 Characterization Kit support page for the latest XDC file.

VC7203 Board XDC Listing

```
#FMC1
set_property PACKAGE_PIN AM38 [get_ports FMC1_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_PRSNT_M2C_L]
set_property PACKAGE_PIN AJ32 [get_ports FMC1_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK0_M2C_P]
set_property PACKAGE_PIN AK32 [get_ports FMC1_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK0_M2C_N]
set_property PACKAGE_PIN AL31 [get_ports FMC1_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK1_M2C_P]
set_property PACKAGE_PIN AL32 [get_ports FMC1_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK1_M2C_N]
set_property PACKAGE_PIN AD32 [get_ports FMC1_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK2_BIDIR_P]
set_property PACKAGE_PIN AD33 [get_ports FMC1_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK2_BIDIR_N]
set_property PACKAGE_PIN AC34 [get_ports FMC1_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK3_BIDIR_P]
set_property PACKAGE_PIN AD35 [get_ports FMC1_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK3_BIDIR_N]
#FMC1 LA
set_property PACKAGE_PIN AU38 [get_ports FMC1_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA00_CC_P]
set_property PACKAGE_PIN AV38 [get_ports FMC1_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA00_CC_N]
set_property PACKAGE_PIN AU39 [get_ports FMC1_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA01_CC_P]
set_property PACKAGE_PIN AV39 [get_ports FMC1_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA01_CC_N]
set_property PACKAGE_PIN AN38 [get_ports FMC1_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA02_P]
set_property PACKAGE_PIN AP38 [get_ports FMC1_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA02_N]
set_property PACKAGE_PIN AM41 [get_ports FMC1_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA03_P]
```

```
set_property PACKAGE_PIN AM42 [get_ports FMC1_LA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA03_N]
set_property PACKAGE_PIN AR38 [get_ports FMC1_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA04_P]
set_property PACKAGE_PIN AR39 [get_ports FMC1_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA04_N]
set_property PACKAGE_PIN AN40 [get_ports FMC1_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA05_P]
set_property PACKAGE_PIN AN41 [get_ports FMC1_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA05_N]
set_property PACKAGE_PIN AR37 [get_ports FMC1_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA06_P]
set_property PACKAGE_PIN AT37 [get_ports FMC1_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA06_N]
set_property PACKAGE_PIN AM39 [get_ports FMC1_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA07_P]
set_property PACKAGE_PIN AN39 [get_ports FMC1_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA07_N]
set_property PACKAGE_PIN AP40 [get_ports FMC1_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA08_P]
set_property PACKAGE_PIN AR40 [get_ports FMC1_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA08_N]
set_property PACKAGE_PIN AP41 [get_ports FMC1_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA09_P]
set_property PACKAGE_PIN AP42 [get_ports FMC1_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA09_N]
set_property PACKAGE_PIN AT39 [get_ports FMC1_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA10_P]
set_property PACKAGE_PIN AT40 [get_ports FMC1_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA10_N]
set_property PACKAGE_PIN AR42 [get_ports FMC1_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA11_P]
set_property PACKAGE_PIN AT42 [get_ports FMC1_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA11_N]
set_property PACKAGE_PIN AW37 [get_ports FMC1_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA12_P]
set_property PACKAGE_PIN AY37 [get_ports FMC1_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA12_N]
set_property PACKAGE_PIN BA37 [get_ports FMC1_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA13_P]
set_property PACKAGE_PIN BB37 [get_ports FMC1_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA13_N]
set_property PACKAGE_PIN AW38 [get_ports FMC1_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA14_P]
set_property PACKAGE_PIN AY38 [get_ports FMC1_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA14_N]
set_property PACKAGE_PIN BB38 [get_ports FMC1_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA15_P]
set_property PACKAGE_PIN BB39 [get_ports FMC1_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA15_N]
set_property PACKAGE_PIN BA39 [get_ports FMC1_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA16_P]
set_property PACKAGE_PIN BA40 [get_ports FMC1_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA16_N]
set_property PACKAGE_PIN AK34 [get_ports FMC1_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA17_CC_P]
set_property PACKAGE_PIN AL34 [get_ports FMC1_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA17_CC_N]
set_property PACKAGE_PIN AJ33 [get_ports FMC1_LA18_CC_P]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA18_CC_P]
set_property PACKAGE_PIN AK33 [get_ports FMC1_LA18_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA18_CC_N]
set_property PACKAGE_PIN AM36 [get_ports FMC1_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA19_P]
set_property PACKAGE_PIN AN36 [get_ports FMC1_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA19_N]
set_property PACKAGE_PIN AJ36 [get_ports FMC1_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA20_P]
set_property PACKAGE_PIN AJ37 [get_ports FMC1_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA20_N]
set_property PACKAGE_PIN AP36 [get_ports FMC1_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA21_P]
set_property PACKAGE_PIN AP37 [get_ports FMC1_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA21_N]
set_property PACKAGE_PIN AK37 [get_ports FMC1_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA22_P]
set_property PACKAGE_PIN AL37 [get_ports FMC1_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA22_N]
set_property PACKAGE_PIN AN35 [get_ports FMC1_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA23_P]
set_property PACKAGE_PIN AP35 [get_ports FMC1_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA23_N]
set_property PACKAGE_PIN AL36 [get_ports FMC1_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA24_P]
set_property PACKAGE_PIN AM37 [get_ports FMC1_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA24_N]
set_property PACKAGE_PIN AG33 [get_ports FMC1_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA25_P]
set_property PACKAGE_PIN AH33 [get_ports FMC1_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA25_N]
set_property PACKAGE_PIN AK35 [get_ports FMC1_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA26_P]
set_property PACKAGE_PIN AL35 [get_ports FMC1_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA26_N]
set_property PACKAGE_PIN AH31 [get_ports FMC1_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA27_P]
set_property PACKAGE_PIN AJ31 [get_ports FMC1_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA27_N]
set_property PACKAGE_PIN AH34 [get_ports FMC1_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA28_P]
set_property PACKAGE_PIN AJ35 [get_ports FMC1_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA28_N]
set_property PACKAGE_PIN AM34 [get_ports FMC1_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA29_P]
set_property PACKAGE_PIN AN34 [get_ports FMC1_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA29_N]
set_property PACKAGE_PIN AM31 [get_ports FMC1_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA30_P]
set_property PACKAGE_PIN AM32 [get_ports FMC1_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA30_N]
set_property PACKAGE_PIN AM33 [get_ports FMC1_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA31_P]
set_property PACKAGE_PIN AN33 [get_ports FMC1_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA31_N]
set_property PACKAGE_PIN AL29 [get_ports FMC1_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA32_P]
set_property PACKAGE_PIN AL30 [get_ports FMC1_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA32_N]
```

```
set_property PACKAGE_PIN AH29 [get_ports FMC1_LA33_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA33_P]
set_property PACKAGE_PIN AH30 [get_ports FMC1_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA33_N]
#FMC1 HA
set_property PACKAGE_PIN AV40 [get_ports FMC1_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA00_CC_P]
set_property PACKAGE_PIN AW40 [get_ports FMC1_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA00_CC_N]
set_property PACKAGE_PIN AY39 [get_ports FMC1_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA01_CC_P]
set_property PACKAGE_PIN AY40 [get_ports FMC1_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA01_CC_N]
set_property PACKAGE_PIN AT41 [get_ports FMC1_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA02_P]
set_property PACKAGE_PIN AU42 [get_ports FMC1_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA02_N]
set_property PACKAGE_PIN AY42 [get_ports FMC1_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA03_P]
set_property PACKAGE_PIN BA42 [get_ports FMC1_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA03_N]
set_property PACKAGE_PIN AU41 [get_ports FMC1_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA04_P]
set_property PACKAGE_PIN AV41 [get_ports FMC1_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA04_N]
set_property PACKAGE_PIN BA41 [get_ports FMC1_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA05_P]
set_property PACKAGE_PIN BB41 [get_ports FMC1_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA05_N]
set_property PACKAGE_PIN AW41 [get_ports FMC1_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA06_P]
set_property PACKAGE_PIN AW42 [get_ports FMC1_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA06_N]
set_property PACKAGE_PIN AJ30 [get_ports FMC1_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA07_P]
set_property PACKAGE_PIN AK30 [get_ports FMC1_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA07_N]
set_property PACKAGE_PIN AF29 [get_ports FMC1_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA08_P]
set_property PACKAGE_PIN AG29 [get_ports FMC1_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA08_N]
set_property PACKAGE_PIN AK28 [get_ports FMC1_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA09_P]
set_property PACKAGE_PIN AK29 [get_ports FMC1_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA09_N]
set_property PACKAGE_PIN AF30 [get_ports FMC1_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA10_P]
set_property PACKAGE_PIN AG31 [get_ports FMC1_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA10_N]
set_property PACKAGE_PIN AH28 [get_ports FMC1_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA11_P]
set_property PACKAGE_PIN AJ28 [get_ports FMC1_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA11_N]
set_property PACKAGE_PIN AC31 [get_ports FMC1_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA12_P]
set_property PACKAGE_PIN AD31 [get_ports FMC1_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA12_N]
set_property PACKAGE_PIN AA31 [get_ports FMC1_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA13_P]
```

```
set_property PACKAGE_PIN AA32 [get_ports FMC1_HA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA13_N]
set_property PACKAGE_PIN AC30 [get_ports FMC1_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA14_P]
set_property PACKAGE_PIN AD30 [get_ports FMC1_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA14_N]
set_property PACKAGE_PIN AA29 [get_ports FMC1_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA15_P]
set_property PACKAGE_PIN AA30 [get_ports FMC1_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA15_N]
set_property PACKAGE_PIN AB29 [get_ports FMC1_HA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA16_P]
set_property PACKAGE_PIN AC29 [get_ports FMC1_HA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA16_N]
#FMC1 HB
set_property PACKAGE_PIN AB33 [get_ports FMC1_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB00_CC_P]
set_property PACKAGE_PIN AC33 [get_ports FMC1_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB00_CC_N]
set_property PACKAGE_PIN AF35 [get_ports FMC1_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB01_P]
set_property PACKAGE_PIN AF36 [get_ports FMC1_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB01_N]
set_property PACKAGE_PIN AE37 [get_ports FMC1_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB02_P]
set_property PACKAGE_PIN AF37 [get_ports FMC1_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB02_N]
set_property PACKAGE_PIN AF34 [get_ports FMC1_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB03_P]
set_property PACKAGE_PIN AG34 [get_ports FMC1_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB03_N]
set_property PACKAGE_PIN AD36 [get_ports FMC1_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB04_P]
set_property PACKAGE_PIN AD37 [get_ports FMC1_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB04_N]
set_property PACKAGE_PIN AC35 [get_ports FMC1_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB05_P]
set_property PACKAGE_PIN AC36 [get_ports FMC1_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB05_N]
set_property PACKAGE_PIN AB31 [get_ports FMC1_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB06_CC_P]
set_property PACKAGE_PIN AB32 [get_ports FMC1_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB06_CC_N]
set_property PACKAGE_PIN AG36 [get_ports FMC1_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB07_P]
set_property PACKAGE_PIN AH36 [get_ports FMC1_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB07_N]
set_property PACKAGE_PIN Y37 [get_ports FMC1_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB08_P]
set_property PACKAGE_PIN AA37 [get_ports FMC1_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB08_N]
set_property PACKAGE_PIN Y35 [get_ports FMC1_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB09_P]
set_property PACKAGE_PIN AA36 [get_ports FMC1_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB09_N]
set_property PACKAGE_PIN AB36 [get_ports FMC1_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB10_P]
set_property PACKAGE_PIN AB37 [get_ports FMC1_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB10_N]
```

```
set_property PACKAGE_PIN AA34 [get_ports FMC1_HB11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB11_P]
set_property PACKAGE_PIN AA35 [get_ports FMC1_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB11_N]
set_property PACKAGE_PIN AE32 [get_ports FMC1_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB12_P]
set_property PACKAGE_PIN AE33 [get_ports FMC1_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB12_N]
set_property PACKAGE_PIN AF31 [get_ports FMC1_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB13_P]
set_property PACKAGE_PIN AF32 [get_ports FMC1_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB13_N]
set_property PACKAGE_PIN AE34 [get_ports FMC1_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB14_P]
set_property PACKAGE_PIN AE35 [get_ports FMC1_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB14_N]
set_property PACKAGE_PIN AE29 [get_ports FMC1_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB15_P]
set_property PACKAGE_PIN AE30 [get_ports FMC1_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB15_N]
set_property PACKAGE_PIN Y32 [get_ports FMC1_HB16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB16_P]
set_property PACKAGE_PIN Y33 [get_ports FMC1_HB16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB16_N]
#FMC2
set_property PACKAGE_PIN G31 [get_ports FMC2_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_PRSNT_M2C_L]
set_property PACKAGE_PIN E34 [get_ports FMC2_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK0_M2C_P]
set_property PACKAGE_PIN E35 [get_ports FMC2_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK0_M2C_N]
set_property PACKAGE_PIN D37 [get_ports FMC2_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK1_M2C_P]
set_property PACKAGE_PIN D38 [get_ports FMC2_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK1_M2C_N]
set_property PACKAGE_PIN M24 [get_ports FMC2_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK2_BIDIR_P]
set_property PACKAGE_PIN L24 [get_ports FMC2_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK2_BIDIR_N]
set_property PACKAGE_PIN K23 [get_ports FMC2_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK3_BIDIR_P]
set_property PACKAGE_PIN J23 [get_ports FMC2_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK3_BIDIR_N]
#FMC2 LA
set_property PACKAGE_PIN L31 [get_ports FMC2_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA00_CC_P]
set_property PACKAGE_PIN K32 [get_ports FMC2_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA00_CC_N]
set_property PACKAGE_PIN M32 [get_ports FMC2_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA01_CC_P]
set_property PACKAGE_PIN L32 [get_ports FMC2_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA01_CC_N]
set_property PACKAGE_PIN K35 [get_ports FMC2_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA02_P]
set_property PACKAGE_PIN J35 [get_ports FMC2_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA02_N]
set_property PACKAGE_PIN J32 [get_ports FMC2_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA03_P]
set_property PACKAGE_PIN J33 [get_ports FMC2_LA03_N]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA03_N]
set_property PACKAGE_PIN K33 [get_ports FMC2_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA04_P]
set_property PACKAGE_PIN K34 [get_ports FMC2_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA04_N]
set_property PACKAGE_PIN L34 [get_ports FMC2_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA05_P]
set_property PACKAGE_PIN L35 [get_ports FMC2_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA05_N]
set_property PACKAGE_PIN M33 [get_ports FMC2_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA06_P]
set_property PACKAGE_PIN M34 [get_ports FMC2_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA06_N]
set_property PACKAGE_PIN H34 [get_ports FMC2_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA07_P]
set_property PACKAGE_PIN H35 [get_ports FMC2_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA07_N]
set_property PACKAGE_PIN K29 [get_ports FMC2_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA08_P]
set_property PACKAGE_PIN K30 [get_ports FMC2_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA08_N]
set_property PACKAGE_PIN J30 [get_ports FMC2_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA09_P]
set_property PACKAGE_PIN H30 [get_ports FMC2_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA09_N]
set_property PACKAGE_PIN L29 [get_ports FMC2_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA10_P]
set_property PACKAGE_PIN L30 [get_ports FMC2_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA10_N]
set_property PACKAGE_PIN J31 [get_ports FMC2_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA11_P]
set_property PACKAGE_PIN H31 [get_ports FMC2_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA11_N]
set_property PACKAGE_PIN M28 [get_ports FMC2_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA12_P]
set_property PACKAGE_PIN M29 [get_ports FMC2_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA12_N]
set_property PACKAGE_PIN R28 [get_ports FMC2_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA13_P]
set_property PACKAGE_PIN P28 [get_ports FMC2_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA13_N]
set_property PACKAGE_PIN N28 [get_ports FMC2_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA14_P]
set_property PACKAGE_PIN N29 [get_ports FMC2_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA14_N]
set_property PACKAGE_PIN R30 [get_ports FMC2_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA15_P]
set_property PACKAGE_PIN P31 [get_ports FMC2_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA15_N]
set_property PACKAGE_PIN U31 [get_ports FMC2_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA16_P]
set_property PACKAGE_PIN T31 [get_ports FMC2_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA16_N]
set_property PACKAGE_PIN C35 [get_ports FMC2_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA17_CC_P]
set_property PACKAGE_PIN C36 [get_ports FMC2_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA17_CC_N]
set_property PACKAGE_PIN D35 [get_ports FMC2_LA18_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA18_CC_P]
```

```
set_property PACKAGE_PIN D36 [get_ports FMC2_LA18_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA18_CC_N]
set_property PACKAGE_PIN B36 [get_ports FMC2_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA19_P]
set_property PACKAGE_PIN A37 [get_ports FMC2_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA19_N]
set_property PACKAGE_PIN B34 [get_ports FMC2_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA20_P]
set_property PACKAGE_PIN A34 [get_ports FMC2_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA20_N]
set_property PACKAGE_PIN B39 [get_ports FMC2_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA21_P]
set_property PACKAGE_PIN A39 [get_ports FMC2_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA21_N]
set_property PACKAGE_PIN A35 [get_ports FMC2_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA22_P]
set_property PACKAGE_PIN A36 [get_ports FMC2_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA22_N]
set_property PACKAGE_PIN C38 [get_ports FMC2_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA23_P]
set_property PACKAGE_PIN C39 [get_ports FMC2_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA23_N]
set_property PACKAGE_PIN B37 [get_ports FMC2_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA24_P]
set_property PACKAGE_PIN B38 [get_ports FMC2_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA24_N]
set_property PACKAGE_PIN E32 [get_ports FMC2_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA25_P]
set_property PACKAGE_PIN D32 [get_ports FMC2_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA25_N]
set_property PACKAGE_PIN B32 [get_ports FMC2_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA26_P]
set_property PACKAGE_PIN B33 [get_ports FMC2_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA26_N]
set_property PACKAGE_PIN E33 [get_ports FMC2_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA27_P]
set_property PACKAGE_PIN D33 [get_ports FMC2_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA27_N]
set_property PACKAGE_PIN C33 [get_ports FMC2_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA28_P]
set_property PACKAGE_PIN C34 [get_ports FMC2_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA28_N]
set_property PACKAGE_PIN G32 [get_ports FMC2_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA29_P]
set_property PACKAGE_PIN F32 [get_ports FMC2_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA29_N]
set_property PACKAGE_PIN F36 [get_ports FMC2_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA30_P]
set_property PACKAGE_PIN F37 [get_ports FMC2_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA30_N]
set_property PACKAGE_PIN F34 [get_ports FMC2_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA31_P]
set_property PACKAGE_PIN F35 [get_ports FMC2_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA31_N]
set_property PACKAGE_PIN H33 [get_ports FMC2_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA32_P]
set_property PACKAGE_PIN G33 [get_ports FMC2_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA32_N]
set_property PACKAGE_PIN E37 [get_ports FMC2_LA33_P]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA33_P]
set_property PACKAGE_PIN E38 [get_ports FMC2_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA33_N]
#FMC2 HA
set_property PACKAGE_PIN N30 [get_ports FMC2_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA00_CC_P]
set_property PACKAGE_PIN M31 [get_ports FMC2_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA00_CC_N]
set_property PACKAGE_PIN P30 [get_ports FMC2_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA01_CC_P]
set_property PACKAGE_PIN N31 [get_ports FMC2_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA01_CC_N]
set_property PACKAGE_PIN V30 [get_ports FMC2_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA02_P]
set_property PACKAGE_PIN V31 [get_ports FMC2_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA02_N]
set_property PACKAGE_PIN T29 [get_ports FMC2_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA03_P]
set_property PACKAGE_PIN T30 [get_ports FMC2_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA03_N]
set_property PACKAGE_PIN W30 [get_ports FMC2_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA04_P]
set_property PACKAGE_PIN W31 [get_ports FMC2_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA04_N]
set_property PACKAGE_PIN V29 [get_ports FMC2_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA05_P]
set_property PACKAGE_PIN U29 [get_ports FMC2_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA05_N]
set_property PACKAGE_PIN Y29 [get_ports FMC2_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA06_P]
set_property PACKAGE_PIN Y30 [get_ports FMC2_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA06_N]
set_property PACKAGE_PIN G36 [get_ports FMC2_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA07_P]
set_property PACKAGE_PIN G37 [get_ports FMC2_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA07_N]
set_property PACKAGE_PIN F39 [get_ports FMC2_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA08_P]
set_property PACKAGE_PIN E39 [get_ports FMC2_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA08_N]
set_property PACKAGE_PIN J37 [get_ports FMC2_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA09_P]
set_property PACKAGE_PIN J38 [get_ports FMC2_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA09_N]
set_property PACKAGE_PIN H38 [get_ports FMC2_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA10_P]
set_property PACKAGE_PIN G38 [get_ports FMC2_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA10_N]
set_property PACKAGE_PIN J36 [get_ports FMC2_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA11_P]
set_property PACKAGE_PIN H36 [get_ports FMC2_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA11_N]
set_property PACKAGE_PIN P25 [get_ports FMC2_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA12_P]
set_property PACKAGE_PIN P26 [get_ports FMC2_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA12_N]
set_property PACKAGE_PIN P22 [get_ports FMC2_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA13_P]
set_property PACKAGE_PIN P23 [get_ports FMC2_HA13_N]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA13_N]
set_property PACKAGE_PIN N25 [get_ports FMC2_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA14_P]
set_property PACKAGE_PIN N26 [get_ports FMC2_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA14_N]
set_property PACKAGE_PIN N23 [get_ports FMC2_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA15_P]
set_property PACKAGE_PIN N24 [get_ports FMC2_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA15_N]
set_property PACKAGE_PIN M27 [get_ports FMC2_HA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA16_P]
set_property PACKAGE_PIN L27 [get_ports FMC2_HA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA16_N]
#FMC2 HB
set_property PACKAGE_PIN J25 [get_ports FMC2_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB00_CC_P]
set_property PACKAGE_PIN J26 [get_ports FMC2_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB00_CC_N]
set_property PACKAGE_PIN H24 [get_ports FMC2_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB01_P]
set_property PACKAGE_PIN G24 [get_ports FMC2_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB01_N]
set_property PACKAGE_PIN J21 [get_ports FMC2_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB02_P]
set_property PACKAGE_PIN H21 [get_ports FMC2_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB02_N]
set_property PACKAGE_PIN H25 [get_ports FMC2_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB03_P]
set_property PACKAGE_PIN H26 [get_ports FMC2_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB03_N]
set_property PACKAGE_PIN G21 [get_ports FMC2_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB04_P]
set_property PACKAGE_PIN G22 [get_ports FMC2_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB04_N]
set_property PACKAGE_PIN G26 [get_ports FMC2_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB05_P]
set_property PACKAGE_PIN G27 [get_ports FMC2_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB05_N]
set_property PACKAGE_PIN K24 [get_ports FMC2_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB06_CC_P]
set_property PACKAGE_PIN K25 [get_ports FMC2_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB06_CC_N]
set_property PACKAGE_PIN H23 [get_ports FMC2_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB07_P]
set_property PACKAGE_PIN G23 [get_ports FMC2_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB07_N]
set_property PACKAGE_PIN G28 [get_ports FMC2_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB08_P]
set_property PACKAGE_PIN G29 [get_ports FMC2_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB08_N]
set_property PACKAGE_PIN K28 [get_ports FMC2_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB09_P]
set_property PACKAGE_PIN J28 [get_ports FMC2_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB09_N]
set_property PACKAGE_PIN H28 [get_ports FMC2_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB10_P]
set_property PACKAGE_PIN H29 [get_ports FMC2_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB10_N]
set_property PACKAGE_PIN K27 [get_ports FMC2_HB11_P]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB11_P]
set_property PACKAGE_PIN J27 [get_ports FMC2_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB11_N]
set_property PACKAGE_PIN M22 [get_ports FMC2_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB12_P]
set_property PACKAGE_PIN L22 [get_ports FMC2_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB12_N]
set_property PACKAGE_PIN L25 [get_ports FMC2_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB13_P]
set_property PACKAGE_PIN L26 [get_ports FMC2_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB13_N]
set_property PACKAGE_PIN K22 [get_ports FMC2_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB14_P]
set_property PACKAGE_PIN J22 [get_ports FMC2_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB14_N]
set_property PACKAGE_PIN M21 [get_ports FMC2_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB15_P]
set_property PACKAGE_PIN L21 [get_ports FMC2_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB15_N]
set_property PACKAGE_PIN P21 [get_ports FMC2_HB16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB16_P]
set_property PACKAGE_PIN N21 [get_ports FMC2_HB16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB16_N]
#FMC3
set_property PACKAGE_PIN AR20 [get_ports FMC3_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_PRSNT_M2C_L]
set_property PACKAGE_PIN AY18 [get_ports FMC3_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK0_M2C_P]
set_property PACKAGE_PIN AY17 [get_ports FMC3_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK0_M2C_N]
set_property PACKAGE_PIN AW18 [get_ports FMC3_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK1_M2C_P]
set_property PACKAGE_PIN AW17 [get_ports FMC3_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK1_M2C_N]
set_property PACKAGE_PIN H15 [get_ports FMC3_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK2_BIDIR_P]
set_property PACKAGE_PIN H14 [get_ports FMC3_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK2_BIDIR_N]
set_property PACKAGE_PIN J13 [get_ports FMC3_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK3_BIDIR_P]
set_property PACKAGE_PIN H13 [get_ports FMC3_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK3_BIDIR_N]
#FMC3 LA
set_property PACKAGE_PIN AP13 [get_ports FMC3_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA00_CC_P]
set_property PACKAGE_PIN AR13 [get_ports FMC3_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA00_CC_N]
set_property PACKAGE_PIN AR14 [get_ports FMC3_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA01_CC_P]
set_property PACKAGE_PIN AT14 [get_ports FMC3_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA01_CC_N]
set_property PACKAGE_PIN AJ16 [get_ports FMC3_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA02_P]
set_property PACKAGE_PIN AJ15 [get_ports FMC3_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA02_N]
set_property PACKAGE_PIN AK14 [get_ports FMC3_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA03_P]
set_property PACKAGE_PIN AK13 [get_ports FMC3_LA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA03_N]
```

```
set_property PACKAGE_PIN AK15 [get_ports FMC3_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA04_P]
set_property PACKAGE_PIN AL14 [get_ports FMC3_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA04_N]
set_property PACKAGE_PIN AJ13 [get_ports FMC3_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA05_P]
set_property PACKAGE_PIN AJ12 [get_ports FMC3_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA05_N]
set_property PACKAGE_PIN AL16 [get_ports FMC3_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA06_P]
set_property PACKAGE_PIN AL15 [get_ports FMC3_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA06_N]
set_property PACKAGE_PIN AK12 [get_ports FMC3_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA07_P]
set_property PACKAGE_PIN AL12 [get_ports FMC3_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA07_N]
set_property PACKAGE_PIN AM13 [get_ports FMC3_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA08_P]
set_property PACKAGE_PIN AN13 [get_ports FMC3_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA08_N]
set_property PACKAGE_PIN AM12 [get_ports FMC3_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA09_P]
set_property PACKAGE_PIN AM11 [get_ports FMC3_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA09_N]
set_property PACKAGE_PIN AN15 [get_ports FMC3_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA10_P]
set_property PACKAGE_PIN AN14 [get_ports FMC3_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA10_N]
set_property PACKAGE_PIN AN11 [get_ports FMC3_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA11_P]
set_property PACKAGE_PIN AP11 [get_ports FMC3_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA11_N]
set_property PACKAGE_PIN AP12 [get_ports FMC3_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA12_P]
set_property PACKAGE_PIN AR12 [get_ports FMC3_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA12_N]
set_property PACKAGE_PIN AR15 [get_ports FMC3_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA13_P]
set_property PACKAGE_PIN AT15 [get_ports FMC3_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA13_N]
set_property PACKAGE_PIN AT12 [get_ports FMC3_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA14_P]
set_property PACKAGE_PIN AU12 [get_ports FMC3_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA14_N]
set_property PACKAGE_PIN AV15 [get_ports FMC3_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA15_P]
set_property PACKAGE_PIN AV14 [get_ports FMC3_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA15_N]
set_property PACKAGE_PIN AW15 [get_ports FMC3_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA16_P]
set_property PACKAGE_PIN AY15 [get_ports FMC3_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA16_N]
set_property PACKAGE_PIN AT17 [get_ports FMC3_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA17_CC_P]
set_property PACKAGE_PIN AU17 [get_ports FMC3_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA17_CC_N]
set_property PACKAGE_PIN AU18 [get_ports FMC3_LA18_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA18_CC_P]
set_property PACKAGE_PIN AV18 [get_ports FMC3_LA18_CC_N]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA18_CC_N]
set_property PACKAGE_PIN AL19 [get_ports FMC3_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA19_P]
set_property PACKAGE_PIN AM19 [get_ports FMC3_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA19_N]
set_property PACKAGE_PIN AK17 [get_ports FMC3_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA20_P]
set_property PACKAGE_PIN AL17 [get_ports FMC3_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA20_N]
set_property PACKAGE_PIN AM18 [get_ports FMC3_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA21_P]
set_property PACKAGE_PIN AM17 [get_ports FMC3_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA21_N]
set_property PACKAGE_PIN AK19 [get_ports FMC3_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA22_P]
set_property PACKAGE_PIN AK18 [get_ports FMC3_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA22_N]
set_property PACKAGE_PIN AM16 [get_ports FMC3_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA23_P]
set_property PACKAGE_PIN AN16 [get_ports FMC3_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA23_N]
set_property PACKAGE_PIN AJ18 [get_ports FMC3_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA24_P]
set_property PACKAGE_PIN AJ17 [get_ports FMC3_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA24_N]
set_property PACKAGE_PIN AP18 [get_ports FMC3_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA25_P]
set_property PACKAGE_PIN AP17 [get_ports FMC3_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA25_N]
set_property PACKAGE_PIN AP20 [get_ports FMC3_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA26_P]
set_property PACKAGE_PIN AR19 [get_ports FMC3_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA26_N]
set_property PACKAGE_PIN AN19 [get_ports FMC3_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA27_P]
set_property PACKAGE_PIN AN18 [get_ports FMC3_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA27_N]
set_property PACKAGE_PIN AR18 [get_ports FMC3_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA28_P]
set_property PACKAGE_PIN AR17 [get_ports FMC3_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA28_N]
set_property PACKAGE_PIN AU19 [get_ports FMC3_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA29_P]
set_property PACKAGE_PIN AV19 [get_ports FMC3_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA29_N]
set_property PACKAGE_PIN AT20 [get_ports FMC3_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA30_P]
set_property PACKAGE_PIN AT19 [get_ports FMC3_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA30_N]
set_property PACKAGE_PIN AV16 [get_ports FMC3_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA31_P]
set_property PACKAGE_PIN AW16 [get_ports FMC3_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA31_N]
set_property PACKAGE_PIN AT16 [get_ports FMC3_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA32_P]
set_property PACKAGE_PIN AU16 [get_ports FMC3_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA32_N]
set_property PACKAGE_PIN BB19 [get_ports FMC3_LA33_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA33_P]
```

```
set_property PACKAGE_PIN BB18 [get_ports FMC3_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA33_N]
#FMC2 HA
set_property PACKAGE_PIN AU14 [get_ports FMC3_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA00_CC_P]
set_property PACKAGE_PIN AU13 [get_ports FMC3_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA00_CC_N]
set_property PACKAGE_PIN AV13 [get_ports FMC3_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA01_CC_P]
set_property PACKAGE_PIN AW13 [get_ports FMC3_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA01_CC_N]
set_property PACKAGE_PIN AW12 [get_ports FMC3_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA02_P]
set_property PACKAGE_PIN AY12 [get_ports FMC3_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA02_N]
set_property PACKAGE_PIN BA15 [get_ports FMC3_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA03_P]
set_property PACKAGE_PIN BA14 [get_ports FMC3_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA03_N]
set_property PACKAGE_PIN AY14 [get_ports FMC3_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA04_P]
set_property PACKAGE_PIN AY13 [get_ports FMC3_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA04_N]
set_property PACKAGE_PIN BB14 [get_ports FMC3_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA05_P]
set_property PACKAGE_PIN BB13 [get_ports FMC3_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA05_N]
set_property PACKAGE_PIN AV20 [get_ports FMC3_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA06_P]
set_property PACKAGE_PIN AW20 [get_ports FMC3_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA06_N]
set_property PACKAGE_PIN BA17 [get_ports FMC3_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA07_P]
set_property PACKAGE_PIN BB17 [get_ports FMC3_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA07_N]
set_property PACKAGE_PIN AY20 [get_ports FMC3_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA08_P]
set_property PACKAGE_PIN BA20 [get_ports FMC3_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA08_N]
set_property PACKAGE_PIN BA16 [get_ports FMC3_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA09_P]
set_property PACKAGE_PIN BB16 [get_ports FMC3_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA09_N]
set_property PACKAGE_PIN AY19 [get_ports FMC3_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA10_P]
set_property PACKAGE_PIN BA19 [get_ports FMC3_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA10_N]
set_property PACKAGE_PIN C16 [get_ports FMC3_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA11_P]
set_property PACKAGE_PIN B16 [get_ports FMC3_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA11_N]
set_property PACKAGE_PIN B14 [get_ports FMC3_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA12_P]
set_property PACKAGE_PIN A14 [get_ports FMC3_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA12_N]
set_property PACKAGE_PIN C15 [get_ports FMC3_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA13_P]
set_property PACKAGE_PIN C14 [get_ports FMC3_HA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA13_N]
```

```
set_property PACKAGE_PIN D13 [get_ports FMC3_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA14_P]
set_property PACKAGE_PIN C13 [get_ports FMC3_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA14_N]
set_property PACKAGE_PIN D16 [get_ports FMC3_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA15_P]
set_property PACKAGE_PIN D15 [get_ports FMC3_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA15_N]
#FMC2 HB
set_property PACKAGE_PIN G14 [get_ports FMC3_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB00_CC_P]
set_property PACKAGE_PIN G13 [get_ports FMC3_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB00_CC_N]
set_property PACKAGE_PIN F16 [get_ports FMC3_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB01_P]
set_property PACKAGE_PIN E15 [get_ports FMC3_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB01_N]
set_property PACKAGE_PIN E14 [get_ports FMC3_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB02_P]
set_property PACKAGE_PIN E13 [get_ports FMC3_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB02_N]
set_property PACKAGE_PIN H16 [get_ports FMC3_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB03_P]
set_property PACKAGE_PIN G16 [get_ports FMC3_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB03_N]
set_property PACKAGE_PIN G12 [get_ports FMC3_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB04_P]
set_property PACKAGE_PIN F12 [get_ports FMC3_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB04_N]
set_property PACKAGE_PIN K12 [get_ports FMC3_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB05_P]
set_property PACKAGE_PIN J12 [get_ports FMC3_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB05_N]
set_property PACKAGE_PIN F15 [get_ports FMC3_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB06_CC_P]
set_property PACKAGE_PIN F14 [get_ports FMC3_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB06_CC_N]
set_property PACKAGE_PIN K15 [get_ports FMC3_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB07_P]
set_property PACKAGE_PIN J15 [get_ports FMC3_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB07_N]
set_property PACKAGE_PIN K14 [get_ports FMC3_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB08_P]
set_property PACKAGE_PIN K13 [get_ports FMC3_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB08_N]
set_property PACKAGE_PIN L16 [get_ports FMC3_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB09_P]
set_property PACKAGE_PIN L15 [get_ports FMC3_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB09_N]
set_property PACKAGE_PIN M14 [get_ports FMC3_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB10_P]
set_property PACKAGE_PIN L14 [get_ports FMC3_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB10_N]
set_property PACKAGE_PIN N16 [get_ports FMC3_HB11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB11_P]
set_property PACKAGE_PIN M16 [get_ports FMC3_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB11_N]
set_property PACKAGE_PIN N13 [get_ports FMC3_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB12_P]
```

```
set_property PACKAGE_PIN M13 [get_ports FMC3_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB12_N]
set_property PACKAGE_PIN N15 [get_ports FMC3_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB13_P]
set_property PACKAGE_PIN N14 [get_ports FMC3_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB13_N]
set_property PACKAGE_PIN M12 [get_ports FMC3_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB14_P]
set_property PACKAGE_PIN M11 [get_ports FMC3_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB14_N]
#SuperClock2_MODULE
set_property PACKAGE_PIN J20 [get_ports CM_RST]
set_property IOSTANDARD LVCMOS18 [get_ports CM_RST]
set_property PACKAGE_PIN C19 [get_ports CM_CTRL_0]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_0]
set_property PACKAGE_PIN B19 [get_ports CM_CTRL_1]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_1]
set_property PACKAGE_PIN A16 [get_ports CM_CTRL_2]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_2]
set_property PACKAGE_PIN A15 [get_ports CM_CTRL_3]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_3]
set_property PACKAGE_PIN A20 [get_ports CM_CTRL_4]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_4]
set_property PACKAGE_PIN A19 [get_ports CM_CTRL_5]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_5]
set_property PACKAGE_PIN B17 [get_ports CM_CTRL_6]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_6]
set_property PACKAGE_PIN A17 [get_ports CM_CTRL_7]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_7]
set_property PACKAGE_PIN B21 [get_ports CM_CTRL_8]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_8]
set_property PACKAGE_PIN A21 [get_ports CM_CTRL_9]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_9]
set_property PACKAGE_PIN C18 [get_ports CM_CTRL_10]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_10]
set_property PACKAGE_PIN B18 [get_ports CM_CTRL_11]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_11]
set_property PACKAGE_PIN D20 [get_ports CM_CTRL_12]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_12]
set_property PACKAGE_PIN C20 [get_ports CM_CTRL_13]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_13]
set_property PACKAGE_PIN F17 [get_ports CM_CTRL_14]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_14]
set_property PACKAGE_PIN E17 [get_ports CM_CTRL_15]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_15]
set_property PACKAGE_PIN D21 [get_ports CM_CTRL_16]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_16]
set_property PACKAGE_PIN C21 [get_ports CM_CTRL_17]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_17]
set_property PACKAGE_PIN D18 [get_ports CM_CTRL_18]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_18]
set_property PACKAGE_PIN D17 [get_ports CM_CTRL_19]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_19]
set_property PACKAGE_PIN F20 [get_ports CM_CTRL_20]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_20]
set_property PACKAGE_PIN E20 [get_ports CM_CTRL_21]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_21]
set_property PACKAGE_PIN K17 [get_ports CM_CTRL_22]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_22]
```

```
set_property PACKAGE_PIN J17 [get_ports CM_CTRL_23]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_23]
set_property PACKAGE_PIN E12 [get_ports CM_LVDS1_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS1_P]
set_property PACKAGE_PIN D12 [get_ports CM_LVDS1_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS1_N]
set_property PACKAGE_PIN L12 [get_ports CM_LVDS2_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS2_P]
set_property PACKAGE_PIN L11 [get_ports CM_LVDS2_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS2_N]
set_property PACKAGE_PIN BA12 [get_ports CM_LVDS3_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS3_P]
set_property PACKAGE_PIN BB12 [get_ports CM_LVDS3_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS3_N]
set_property PACKAGE_PIN K19 [get_ports CM_GCLK_P]
set_property IOSTANDARD LVCMOS18 [get_ports CM_GCLK_P]
set_property PACKAGE_PIN J18 [get_ports CM_GCLK_N]
set_property IOSTANDARD LVCMOS18 [get_ports CM_GCLK_N]
#SWITCHES
set_property PACKAGE_PIN E42 [get_ports USER_SW1]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW1]
set_property PACKAGE_PIN C40 [get_ports USER_SW2]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW2]
set_property PACKAGE_PIN C41 [get_ports USER_SW3]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW3]
set_property PACKAGE_PIN H40 [get_ports USER_SW4]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW4]
set_property PACKAGE_PIN H41 [get_ports USER_SW5]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW5]
set_property PACKAGE_PIN H39 [get_ports USER_SW6]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW6]
set_property PACKAGE_PIN G39 [get_ports USER_SW7]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW7]
set_property PACKAGE_PIN G41 [get_ports USER_SW8]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW8]
#BUTTONS
set_property PACKAGE_PIN P41 [get_ports USER_PB1]
set_property IOSTANDARD LVCMOS18 [get_ports USER_PB1]
set_property PACKAGE_PIN N41 [get_ports USER_PB2]
set_property IOSTANDARD LVCMOS18 [get_ports USER_PB2]
#SMAs
set_property PACKAGE_PIN H19 [get_ports CLK_DIFF_1_P]
set_property IOSTANDARD LVCMOS18 [get_ports CLK_DIFF_1_P]
set_property PACKAGE_PIN G18 [get_ports CLK_DIFF_1_N]
set_property IOSTANDARD LVCMOS18 [get_ports CLK_DIFF_1_N]
set_property PACKAGE_PIN K39 [get_ports CLK_DIFF_2_P]
set_property IOSTANDARD LVCMOS18 [get_ports CLK_DIFF_2_P]
set_property PACKAGE_PIN K40 [get_ports CLK_DIFF_2_N]
set_property IOSTANDARD LVCMOS18 [get_ports CLK_DIFF_2_N]
#SYSTEM CLOCKS
set_property PACKAGE_PIN E19 [get_ports LVDS_OSC_P]
set_property IOSTANDARD LVDS [get_ports LVDS_OSC_P]
set_property PACKAGE_PIN E18 [get_ports LVDS_OSC_N]
set_property IOSTANDARD LVDS [get_ports LVDS_OSC_N]
#LEDs
set_property PACKAGE_PIN M37 [get_ports APP_LED1]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED1]
set_property PACKAGE_PIN M38 [get_ports APP_LED2]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED2]
```

```
set_property PACKAGE_PIN R42 [get_ports APP_LED3]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED3]
set_property PACKAGE_PIN P42 [get_ports APP_LED4]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED4]
set_property PACKAGE_PIN N38 [get_ports APP_LED5]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED5]
set_property PACKAGE_PIN M39 [get_ports APP_LED6]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED6]
set_property PACKAGE_PIN R40 [get_ports APP_LED7]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED7]
set_property PACKAGE_PIN P40 [get_ports APP_LED8]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED8]
#IIC
set_property PACKAGE_PIN M41 [get_ports DUT_I2C_SCL]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_I2C_SCL]
set_property PACKAGE_PIN L41 [get_ports DUT_I2C_SDA]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_I2C_SDA]
#PMBUS
set_property PACKAGE_PIN E40 [get_ports DUT_PMB_ALERT]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_ALERT]
set_property PACKAGE_PIN D40 [get_ports DUT_PMB_CTRL]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_CTRL]
set_property PACKAGE_PIN A40 [get_ports DUT_PMB_CLK]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_CLK]
set_property PACKAGE_PIN A41 [get_ports DUT_PMB_DATA]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_DATA]
#USB_GPIOs
set_property PACKAGE_PIN B28 [get_ports USB_GPIO_0]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_0]
set_property PACKAGE_PIN B29 [get_ports USB_GPIO_1]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_1]
set_property PACKAGE_PIN A31 [get_ports USB_GPIO_2]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_2]
set_property PACKAGE_PIN A32 [get_ports USB_GPIO_3]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_3]
#UART
set_property PACKAGE_PIN A29 [get_ports USB_TXD_0]
set_property IOSTANDARD LVCMOS18 [get_ports USB_TXD_0]
set_property PACKAGE_PIN A30 [get_ports USB_RXD_I]
set_property IOSTANDARD LVCMOS18 [get_ports USB_RXD_I]
set_property PACKAGE_PIN C31 [get_ports USB_RTS_0_B]
set_property IOSTANDARD LVCMOS18 [get_ports USB_RTS_0_B]
set_property PACKAGE_PIN B31 [get_ports USB_CTS_I_B]
set_property IOSTANDARD LVCMOS18 [get_ports USB_CTS_I_B]
#SPI
set_property PACKAGE_PIN A24 [get_ports MGT_MOD_SPI_SCK]
set_property IOSTANDARD LVCMOS18 [get_ports MGT_MOD_SPI_SCK]
set_property PACKAGE_PIN A25 [get_ports MGT_MOD_SPI_D]
set_property IOSTANDARD LVCMOS18 [get_ports MGT_MOD_SPI_D]
set_property PACKAGE_PIN B22 [get_ports MGT_MOD_SPI_Q]
set_property IOSTANDARD LVCMOS18 [get_ports MGT_MOD_SPI_Q]
set_property PACKAGE_PIN A22 [get_ports GTX_MOD_SPI_CS]
set_property IOSTANDARD LVCMOS18 [get_ports GTX_MOD_SPI_CS]
#MGTs
set_property PACKAGE_PIN AW10 [get_ports 111_REFCLK0_P]
set_property PACKAGE_PIN AW9 [get_ports 111_REFCLK0_N]
set_property PACKAGE_PIN BA10 [get_ports 111_REFCLK1_P]
set_property PACKAGE_PIN BA9 [get_ports 111_REFCLK1_N]
set_property PACKAGE_PIN AW2 [get_ports 111_TX3_P]
```

```
set_property PACKAGE_PIN AW1 [get_ports 111_TX3_N]
set_property PACKAGE_PIN AW6 [get_ports 111_RX3_P]
set_property PACKAGE_PIN AW5 [get_ports 111_RX3_N]
set_property PACKAGE_PIN AY4 [get_ports 111_TX2_P]
set_property PACKAGE_PIN AY3 [get_ports 111_TX2_N]
set_property PACKAGE_PIN AY8 [get_ports 111_RX2_P]
set_property PACKAGE_PIN AY7 [get_ports 111_RX2_N]
set_property PACKAGE_PIN BA2 [get_ports 111_TX1_P]
set_property PACKAGE_PIN BA1 [get_ports 111_TX1_N]
set_property PACKAGE_PIN BA6 [get_ports 111_RX1_P]
set_property PACKAGE_PIN BA5 [get_ports 111_RX1_N]
set_property PACKAGE_PIN BB4 [get_ports 111_TX0_P]
set_property PACKAGE_PIN BB3 [get_ports 111_TX0_N]
set_property PACKAGE_PIN BB8 [get_ports 111_RX0_P]
set_property PACKAGE_PIN BB7 [get_ports 111_RX0_N]
set_property PACKAGE_PIN AT8 [get_ports 112_REFCLK0_P]
set_property PACKAGE_PIN AT7 [get_ports 112_REFCLK0_N]
set_property PACKAGE_PIN AU10 [get_ports 112_REFCLK1_P]
set_property PACKAGE_PIN AU9 [get_ports 112_REFCLK1_N]
set_property PACKAGE_PIN AR2 [get_ports 112_TX3_P]
set_property PACKAGE_PIN AR1 [get_ports 112_TX3_N]
set_property PACKAGE_PIN AP8 [get_ports 112_RX3_P]
set_property PACKAGE_PIN AP7 [get_ports 112_RX3_N]
set_property PACKAGE_PIN AT4 [get_ports 112_TX2_P]
set_property PACKAGE_PIN AT3 [get_ports 112_TX2_N]
set_property PACKAGE_PIN AR6 [get_ports 112_RX2_P]
set_property PACKAGE_PIN AR5 [get_ports 112_RX2_N]
set_property PACKAGE_PIN AU2 [get_ports 112_TX1_P]
set_property PACKAGE_PIN AU1 [get_ports 112_TX1_N]
set_property PACKAGE_PIN AU6 [get_ports 112_RX1_P]
set_property PACKAGE_PIN AU5 [get_ports 112_RX1_N]
set_property PACKAGE_PIN AV4 [get_ports 112_TX0_P]
set_property PACKAGE_PIN AV3 [get_ports 112_TX0_N]
set_property PACKAGE_PIN AV8 [get_ports 112_RX0_P]
set_property PACKAGE_PIN AV7 [get_ports 112_RX0_N]
set_property PACKAGE_PIN AH8 [get_ports 113_REFCLK0_P]
set_property PACKAGE_PIN AH7 [get_ports 113_REFCLK0_N]
set_property PACKAGE_PIN AK7 [get_ports 113_REFCLK1_N]
set_property PACKAGE_PIN AK8 [get_ports 113_REFCLK1_P]
set_property PACKAGE_PIN AL2 [get_ports 113_TX3_P]
set_property PACKAGE_PIN AL1 [get_ports 113_TX3_N]
set_property PACKAGE_PIN AJ6 [get_ports 113_RX3_P]
set_property PACKAGE_PIN AJ5 [get_ports 113_RX3_N]
set_property PACKAGE_PIN AM4 [get_ports 113_TX2_P]
set_property PACKAGE_PIN AL6 [get_ports 113_RX2_P]
set_property PACKAGE_PIN AM3 [get_ports 113_TX2_N]
set_property PACKAGE_PIN AL5 [get_ports 113_RX2_N]
set_property PACKAGE_PIN AN2 [get_ports 113_TX1_P]
set_property PACKAGE_PIN AM8 [get_ports 113_RX1_P]
set_property PACKAGE_PIN AN1 [get_ports 113_TX1_N]
set_property PACKAGE_PIN AM7 [get_ports 113_RX1_N]
set_property PACKAGE_PIN AP4 [get_ports 113_TX0_P]
set_property PACKAGE_PIN AN6 [get_ports 113_RX0_P]
set_property PACKAGE_PIN AP3 [get_ports 113_TX0_N]
set_property PACKAGE_PIN AN5 [get_ports 113_RX0_N]
set_property PACKAGE_PIN AD8 [get_ports 114_REFCLK0_P]
set_property PACKAGE_PIN AD7 [get_ports 114_REFCLK0_N]
set_property PACKAGE_PIN AF8 [get_ports 114_REFCLK1_P]
set_property PACKAGE_PIN AF7 [get_ports 114_REFCLK1_N]
```

```
set_property PACKAGE_PIN AG2 [get_ports 114_TX3_P]
set_property PACKAGE_PIN AG1 [get_ports 114_TX3_N]
set_property PACKAGE_PIN AD4 [get_ports 114_RX3_P]
set_property PACKAGE_PIN AD3 [get_ports 114_RX3_N]
set_property PACKAGE_PIN AH4 [get_ports 114_TX2_P]
set_property PACKAGE_PIN AH3 [get_ports 114_TX2_N]
set_property PACKAGE_PIN AE6 [get_ports 114_RX2_P]
set_property PACKAGE_PIN AE5 [get_ports 114_RX2_N]
set_property PACKAGE_PIN AJ2 [get_ports 114_TX1_P]
set_property PACKAGE_PIN AJ1 [get_ports 114_TX1_N]
set_property PACKAGE_PIN AF4 [get_ports 114_RX1_P]
set_property PACKAGE_PIN AF3 [get_ports 114_RX1_N]
set_property PACKAGE_PIN AK4 [get_ports 114_TX0_P]
set_property PACKAGE_PIN AK3 [get_ports 114_TX0_N]
set_property PACKAGE_PIN AG6 [get_ports 114_RX0_P]
set_property PACKAGE_PIN AG5 [get_ports 114_RX0_N]
set_property PACKAGE_PIN Y8 [get_ports 115_REFCLK0_P]
set_property PACKAGE_PIN Y7 [get_ports 115_REFCLK0_N]
set_property PACKAGE_PIN AB8 [get_ports 115_REFCLK1_P]
set_property PACKAGE_PIN AB7 [get_ports 115_REFCLK1_N]
set_property PACKAGE_PIN W2 [get_ports 115_TX3_P]
set_property PACKAGE_PIN W1 [get_ports 115_TX3_N]
set_property PACKAGE_PIN Y4 [get_ports 115_RX3_P]
set_property PACKAGE_PIN Y3 [get_ports 115_RX3_N]
set_property PACKAGE_PIN AA2 [get_ports 115_TX2_P]
set_property PACKAGE_PIN AA1 [get_ports 115_TX2_N]
set_property PACKAGE_PIN AA6 [get_ports 115_RX2_P]
set_property PACKAGE_PIN AA5 [get_ports 115_RX2_N]
set_property PACKAGE_PIN AC2 [get_ports 115_TX1_P]
set_property PACKAGE_PIN AC1 [get_ports 115_TX1_N]
set_property PACKAGE_PIN AB4 [get_ports 115_RX1_P]
set_property PACKAGE_PIN AB3 [get_ports 115_RX1_N]
set_property PACKAGE_PIN AE2 [get_ports 115_TX0_P]
set_property PACKAGE_PIN AE1 [get_ports 115_TX0_N]
set_property PACKAGE_PIN AC6 [get_ports 115_RX0_P]
set_property PACKAGE_PIN AC5 [get_ports 115_RX0_N]
set_property PACKAGE_PIN T8 [get_ports 116_REFCLK0_P]
set_property PACKAGE_PIN T7 [get_ports 116_REFCLK0_N]
set_property PACKAGE_PIN V8 [get_ports 116_REFCLK1_P]
set_property PACKAGE_PIN V7 [get_ports 116_REFCLK1_N]
set_property PACKAGE_PIN P4 [get_ports 116_TX3_P]
set_property PACKAGE_PIN P3 [get_ports 116_TX3_N]
set_property PACKAGE_PIN R6 [get_ports 116_RX3_P]
set_property PACKAGE_PIN R5 [get_ports 116_RX3_N]
set_property PACKAGE_PIN R2 [get_ports 116_TX2_P]
set_property PACKAGE_PIN R1 [get_ports 116_TX2_N]
set_property PACKAGE_PIN U6 [get_ports 116_RX2_P]
set_property PACKAGE_PIN U5 [get_ports 116_RX2_N]
set_property PACKAGE_PIN V4 [get_ports 116_RX1_P]
set_property PACKAGE_PIN T4 [get_ports 116_TX1_P]
set_property PACKAGE_PIN T3 [get_ports 116_TX1_N]
set_property PACKAGE_PIN V3 [get_ports 116_RX1_N]
set_property PACKAGE_PIN U2 [get_ports 116_TX0_P]
set_property PACKAGE_PIN U1 [get_ports 116_TX0_N]
set_property PACKAGE_PIN W6 [get_ports 116_RX0_P]
set_property PACKAGE_PIN W5 [get_ports 116_RX0_N]
set_property PACKAGE_PIN K8 [get_ports 117_REFCLK0_P]
set_property PACKAGE_PIN K7 [get_ports 117_REFCLK0_N]
set_property PACKAGE_PIN M8 [get_ports 117_REFCLK1_P]
```

```
set_property PACKAGE_PIN M7 [get_ports 117_REFCLK1_N]
set_property PACKAGE_PIN K4 [get_ports 117_TX3_P]
set_property PACKAGE_PIN K3 [get_ports 117_TX3_N]
set_property PACKAGE_PIN J6 [get_ports 117_RX3_P]
set_property PACKAGE_PIN J5 [get_ports 117_RX3_N]
set_property PACKAGE_PIN L2 [get_ports 117_TX2_P]
set_property PACKAGE_PIN L1 [get_ports 117_TX2_N]
set_property PACKAGE_PIN L6 [get_ports 117_RX2_P]
set_property PACKAGE_PIN L5 [get_ports 117_RX2_N]
set_property PACKAGE_PIN M4 [get_ports 117_TX1_P]
set_property PACKAGE_PIN M3 [get_ports 117_TX1_N]
set_property PACKAGE_PIN N6 [get_ports 117_RX1_P]
set_property PACKAGE_PIN N5 [get_ports 117_RX1_N]
set_property PACKAGE_PIN N2 [get_ports 117_TX0_P]
set_property PACKAGE_PIN N1 [get_ports 117_TX0_N]
set_property PACKAGE_PIN P8 [get_ports 117_RX0_P]
set_property PACKAGE_PIN P7 [get_ports 117_RX0_N]
set_property PACKAGE_PIN E10 [get_ports 118_REFCLK0_P]
set_property PACKAGE_PIN E9 [get_ports 118_REFCLK0_N]
set_property PACKAGE_PIN G10 [get_ports 118_REFCLK1_P]
set_property PACKAGE_PIN G9 [get_ports 118_REFCLK1_N]
set_property PACKAGE_PIN F4 [get_ports 118_TX3_P]
set_property PACKAGE_PIN F3 [get_ports 118_TX3_N]
set_property PACKAGE_PIN E6 [get_ports 118_RX3_P]
set_property PACKAGE_PIN E5 [get_ports 118_RX3_N]
set_property PACKAGE_PIN G2 [get_ports 118_TX2_P]
set_property PACKAGE_PIN G1 [get_ports 118_TX2_N]
set_property PACKAGE_PIN F8 [get_ports 118_RX2_P]
set_property PACKAGE_PIN F7 [get_ports 118_RX2_N]
set_property PACKAGE_PIN H4 [get_ports 118_TX1_P]
set_property PACKAGE_PIN H3 [get_ports 118_TX1_N]
set_property PACKAGE_PIN G6 [get_ports 118_RX1_P]
set_property PACKAGE_PIN G5 [get_ports 118_RX1_N]
set_property PACKAGE_PIN J2 [get_ports 118_TX0_P]
set_property PACKAGE_PIN H8 [get_ports 118_RX0_P]
set_property PACKAGE_PIN J1 [get_ports 118_TX0_N]
set_property PACKAGE_PIN H7 [get_ports 118_RX0_N]
set_property PACKAGE_PIN A10 [get_ports 119_REFCLK0_P]
set_property PACKAGE_PIN A9 [get_ports 119_REFCLK0_N]
set_property PACKAGE_PIN C10 [get_ports 119_REFCLK1_P]
set_property PACKAGE_PIN C9 [get_ports 119_REFCLK1_N]
set_property PACKAGE_PIN B4 [get_ports 119_TX3_P]
set_property PACKAGE_PIN B3 [get_ports 119_TX3_N]
set_property PACKAGE_PIN A6 [get_ports 119_RX3_P]
set_property PACKAGE_PIN A5 [get_ports 119_RX3_N]
set_property PACKAGE_PIN C2 [get_ports 119_TX2_P]
set_property PACKAGE_PIN C1 [get_ports 119_TX2_N]
set_property PACKAGE_PIN B8 [get_ports 119_RX2_P]
set_property PACKAGE_PIN B7 [get_ports 119_RX2_N]
set_property PACKAGE_PIN D4 [get_ports 119_TX1_P]
set_property PACKAGE_PIN D3 [get_ports 119_TX1_N]
set_property PACKAGE_PIN C6 [get_ports 119_RX1_P]
set_property PACKAGE_PIN C5 [get_ports 119_RX1_N]
set_property PACKAGE_PIN E2 [get_ports 119_TX0_P]
set_property PACKAGE_PIN E1 [get_ports 119_TX0_N]
set_property PACKAGE_PIN D8 [get_ports 119_RX0_P]
set_property PACKAGE_PIN D7 [get_ports 119_RX0_N]
```

XILINX

Appendix D

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC7203 kit and its documentation is available on these websites:

Virtex-7 FPGA VC7203 Characterization Kit

Virtex-7 FPGA VC7203 Characterization Kit documentation

Virtex-7 FPGA VC7203 Characterization Master Answer Record (AR 52383)

These documents and websites provide supplemental material useful with this guide:

1. *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
2. Information about the power system components used by the VC7203 board is available from the Texas Instruments digital power website at:

   www.ti.com/ww/en/analog/digital-power/index.html
3. Information about the 7 series GTX power supply modules included with the VC7203 Characterization Kit is available from the following vendors:

   Intersil: www.intersil.com/en/applications/computing/xlinx-fpga.html

   Texas Instruments: www.ti.com/tool/pmp6577.1

   General Electric: go.ge-energy.com/FPGA_2014_XiLinx_Download.html
4. *7 Series FPGAs Overview* (DS180)
5. *Vivado Design Suite User Guide: Using Constraints* (UG903)
6. *VC7203 IBERT Getting Started Guide (ISE Design Suite)* (UG846)
7. *Virtex-7 FPGA VC7203 Characterization Kit IBERT Getting Started Guide (Vivado Design Suite)* (UG847)

8. *Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics* (DS183)
9. *7 Series FPGAs Configuration User Guide* (UG470)
10. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
11. *7 Series FPGAs Clocking Resources User Guide* (UG472)
12. *7 Series FPGAs Configurable Logic Block User Guide* (UG474)
13. *7 Series FPGAs Packaging and Pinout Product Specification* (UG475)
14. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
15. *7 Series FPGAs Integrated Block for PCI Express v1.8 User Guide* (PG054)
16. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)

XILINX

Appendix E

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Declaration of Conformity

See the Virtex-7 FPGA VC703 Declaration of Conformity.

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product and can cause radio interference. In a domestic environment, the user might be required to take adequate corrective measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive.*

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Programmable Logic IC Development Tools ***category:***

Click to view products by Xilinx ***manufacturer:***

Other Similar products are found below :

DK-DEV-5SGXEA7N SLG4DVKADV 88980182 DEV-17526 DEV-17514 LCMXO3L-SMA-EVN 471-014 80-001005 iCE40UP5K-MDP-EVN ALTHYDRAC5GX ALTNITROC5GX 471-015 Hinj SnoMakrR10 DK-DEV-1SDX-P-A DK-DEV-1SDX-P-0ES DK-DEV-1SMC-H-A DK-DEV-1SMX-H-0ES DK-DEV-1SMX-H-A DK-DEV-4CGX150N DK-DEV-5CGTD9N DK-DEV-5CSXC6N DK-DEV-5M570ZN DK-MAXII-1270N DK-SI-1SGX-H-A DK-SI-1STX-E-0ES DK-SI-1STX-E-A DK-SI-5SGXEA7N ATF15XX-DK3-U SLG46824V-DIP SLG46826V-DIP 240-114-1 6003-410-017 ICE40UP5K-B-EVN DK-SOC-1SSX-L-D ICE5LP4K-WDEV-EVN L-ASC-BRIDGE-EVN LC4256ZE-B-EVN LCMXO2-7000HE-B-EVN LCMXO3D-9400HC-B-EVN LCMXO3L-6900C-S-EVN LF-81AGG-EVN LFE3-MEZZ-EVN LIF-MD6000-ML-EVN LPTM-ASC-B-EVN M2S-HELLO-FPGA-KIT VIDEO-DC-USXGMII 12GSDIFMCCD SFP+X4FMCCD NAE-CW305-04-7A100-0.10-X