100G IEEE 802.3bj Reed-Solomon FEC v2.0

PB028 April 4, 2018 **LogiCORE IP Product Brief**

Introduction

The Xilinx® LogiCORE™ IP IEEE 802.3bj Reed-Solomon Forward Error Correction (RS-FEC) core implements the RS-FEC sublayer as described in *IEEE 802.3bj-2014,* section 91.

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/ieee802-3bj-rs-fec/index.htm

Features

- IEEE 802.3bj-2014 TX and RX
- Low latency design
- Supports 100 Gb/s
- Supports RS(528,514) KR4 and RS(544,514) KP4
- Configuration and status bus
- Selectable AXI4-Lite interface for status output
- Transcode Bypass mode for direct access to RS-FEC encoder/decoder
- CAUI-4 support in Active mode
- CAUI-4 and CAUI-10 support in Bypass mode (KR4 mode only)
- Example reference design demonstrating integrated 100G Ethernet IP with RS-FEC
- ECC RAM option
- Status outputs for monitoring the core and for statistics generation

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™ Virtex® UltraScale™
Supported User Interfaces	AXI4-Lite, Configuration and Status bus
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog
Test Bench	Not Provided
Constraints File	Xilinx Constraints File
Simulation Model	Encrypted Verilog
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Design Suite
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The 100G IEEE 802.3bj RS-FEC core implements the OSI layer, RS-FEC, shown shaded in Figure 1.

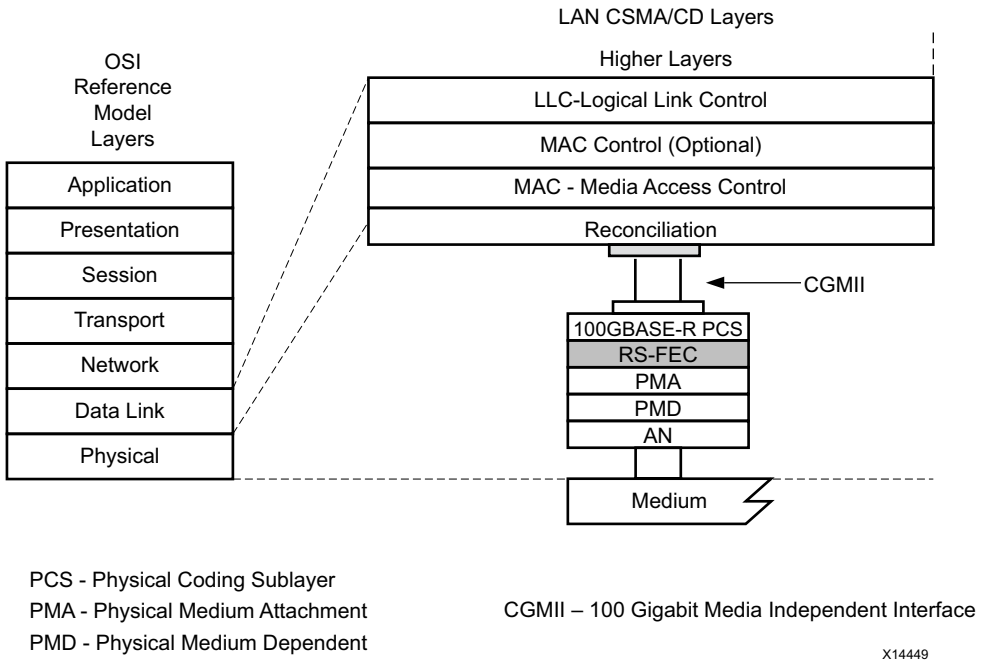

Figure 1: **IEEE Std 802.3-2014 Ethernet Model**

The RS-FEC layer of *IEEE Std 802.3bj-2014* defines more than just the RS encoder/decoder. It defines several stages of synchronization, alignment, and reordering which are necessary for the layer to communicate with preceding and subsequent layers. The IEEE 802.3-2014 block diagram is shown in Figure 2.

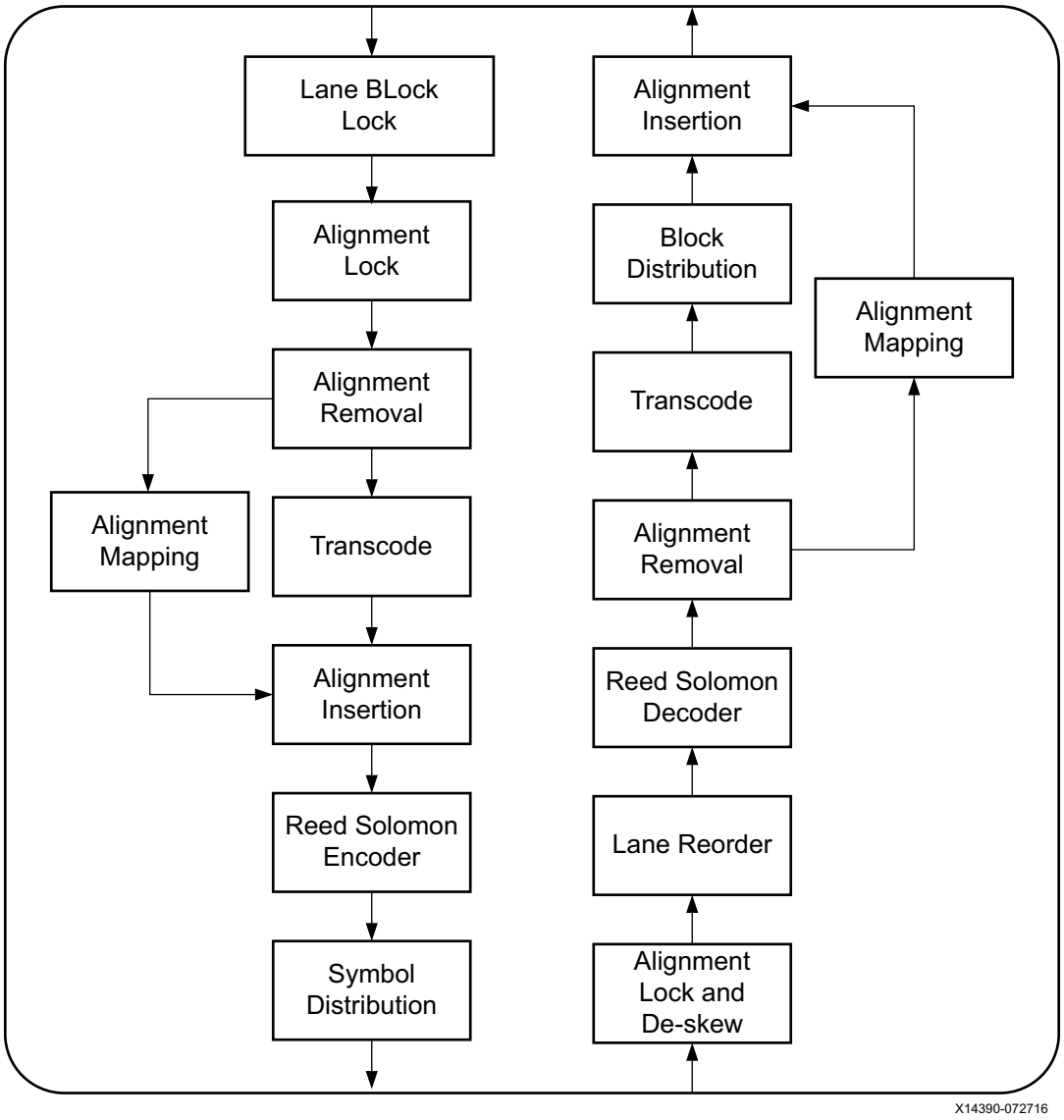

Figure 2: **Block Diagram of IEEE802bj RS-FEC Core**

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

License Type

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the IEEE 802.3bj Reed-Solomon Forward Error Correction web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Evaluation

A full system hardware evaluation license is available for this core. The evaluation version of the core operates in the same way as the full version for several hours, dependent on clock frequency. Operation is then disabled and the data output does not change. If you notice this behavior in hardware, it probably means you are using an evaluation version of the core. The Xilinx tools warn that an evaluation license is being used during netlist implementation. If a full license is installed for the core to run on hardware, delete the old files and recreate the core from new.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/04/2018	2.0	Aligned to Product Guide (PG197) updates.
10/05/2016	1.0	Aligned to Product Guide (PG197) updates.
04/01/2015	1.0	Initial Xilinx release.

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