LogiCORE IP Digital Pre-Distortion v9.0

PB006 (v9.0) January 29, 2018 **LogiCORE IP Product Brief**

Introduction

The LogiCORE™ IP Digital Pre-Distortion (DPD) IP negates the non-linear effects of a power amplifier (PA) when transmitting a wide-band signal. DPD allows a PA to achieve greater efficiency by operating at a higher output power while maintaining spectral compliance, and reducing system capital and operational expenditure.

Additional Documentation

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: https://www.xilinx.com/member/dpd_evaluation/index.htm.

Features

- Algorithm
  - DPD correction with up to 40 dB of adjacent channel leakage ratio (ACLR) improvement
- Physical Configuration Parameters
  - Selection of phase options for datapath implementation allowing a resource/sample rate trade-off
  - Selection of one, two, four, six or eight transmit antennas
  - Multiple filter and capture depth options for low cost solutions like macro Base stations, massive MIMO 5G RRH, micro Remote Radio Head (RRH), Distributed Antenna System (DAS), and low power PA applications.
  - Independent control of filter memory depth, capture memory depth and acceleration levels allowing for resource versus performance trade-off
- Software
  - Support for SMP mode under Linux Operating System

See Digital Pre-Distortion v9.0 Product Guide (PG076) for more detailed feature information.

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq®-7000, Zynq UltraScale+™, and Zynq UltraScale+ RFSoC
Supported User Interfaces	AXI4, AXI4-Lite, and AXI4-Stream
Resources	See the *Digital Pre-Distortion v9.0 Product Guide*
Provided with Core	
Design Files	Local Vivado® repository
Example Design	Not Provided
Test Bench	Test bench is provided. See Test Bench section in *Digital Pre-Distortion v9.0 Product Guide* (PG076) for more details. (registration required)
Constraints File	See Constraining the Core section in *Digital Pre-Distortion v9.0 Product Guide* (PG076) for more details. (registration required)
Simulation Model	Not Provided
Supported S/W Driver	Executable and linkable format files are now packaged along with the DFE Subsystem Reference Design which need to be downloaded separately.
Tested Design Flows[2]	
Design Entry	Vivado Design Suite 2018.3
Simulation	Supported. See Test Bench section in *Digital Pre-Distortion v9.0 Product Guide* (PG076) for more details. (registration required)
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information about this core, visit the Digital Pre-Distortion product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx® LogiCORE IP modules and tools, contact your local Xilinx sales representative.

The DPD v9.0 core is available as an evaluation version which operates for several hours, depending on the clock frequency. The data output is set to zero after the evaluation period ends. The host interface reports EVAL_LICENSE_TIMEOUT status value when the hardware times out.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
1/29/2018 Version 9.0	
General updates	Requirement changed to Vivado 2018.3 tools.
06/20/2018 Version 8.1	
General updates	• Requirement changed to Vivado 2018.1 tools. • Added support for Zynq UltraScale+ RFSoC devices.
07/03/2017 Version 8.1	
General updates	Requirement changed to Vivado 2017.2 tools. Demo test bench is provided with IP.
12/09/2016 Version 8.0	
General updates	Requirement changed to Vivado 2016.3 tools.
06/30/2016 Version 8.0	
General updates	Early Access Draft • Added support for Zynq UltraScale+ MPSoC devices. • Requirement changed to Vivado 2016.2 tools.
09/30/2015 Version 7.1	
General updates	• Added two features to the IP Facts table. • Updated the Licensing and Ordering Information and Support sections.
12/15/2014 Version 7.0	
General updates	• Synchronize document version with core version. • Updated the Introduction and Features sections. • Added IP Fact Table.
10/16/12 Version 2.0	
General updates	Updated for ISE® Design Suite 14.3.
08/15/11 Version 1.1	
General updates	Updated for ISE® Design Suite 14.3.
06/22/11 Version 1.0	
Initial Xilinx release.	ISE Design Suite 13.2. Previous version of this Product Brief is XMP143.

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