IP Facts

The LDPC Encoder/Decoder supports Low Density Parity Check (LDPC) decoding and encoding. The LDPC codes used are highly configurable, and the specific code used can be specified on a codeword-by-codeword basis.

Additional Documentation

A Product Guide is available for this core. Access to this material can be requested by clicking on this registration link: http://www.xilinx.com/member/ldpc-enc-dec.html.

Features

The soft IP core is a highly flexible soft-decision implementation for LDPC codes offering the following features.

- LDPC decode or encode of a range of customer specified Quasi-cyclic (QC) codes, including 5G New Radio codes
- Peak throughput up to:
  - 1.78 Gb/s LDPC decode @ 8 iterations
  - 12.5 Gb/s for LDPC encode
- High bandwidth AXI4-Stream interfaces

LDPC Decoding/Encoding

- Highly configurable codes
  - A range of quasi-cyclic codes can be configured over an AXI4-Lite interface
  - Code parameter memory can be shared across up to 128 codes
  - Codes can be selected on a block-by-block basis
  - 5G support mode where tables are pre-loaded
- Normalized min-sum or offset min-sum decoding algorithm
  - Normalization factor programmable (from 0.0625 to 1 in steps of 0.0625) for layers
  - Offset factor can be specified per block (from 0.25 to 3.75 in steps of 0.25)

- Number of iterations between 1 and 63
  - Specified for each block using the AXI4-Stream control interface
- Early termination
  - Specified for each block to be none, one, or both of the following:
    - Parity check passes
    - No change in hard information or parity bits since last iteration
- When configured as a decoder, soft or hard outputs
  - Specified for each block to include information and optional parity
  - 6-bit soft log-likelihood ratio (LLR) input (8-bit interface, two fractional bits, with external saturation before input to symmetric range -7.75 to +7.75 assumed) and 8-bit output
- In- or out-of-order execution of blocks, with user specified ID field to identify blocks
- Encoder and decoder variants, with optional support for improved throughput when sub-matrix size is small
- Optional final parity check to update parity pass/fail for final output
- Optional initialization of codes from device configuration, avoiding download using AXI4-Lite interface

Interfaces

- Wide data interfaces on input and output
- Ability to specify number of inputs and outputs on either a block-by-block basis or transfer basis
- Separate inputs to specify control parameters and receive status output on a block-by-block basis

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq® UltraScale+™ MPSoC, UltraScale™, UltraScale+™ 7 series Versal™ ACAP
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources	Performance and Resource Utilization web page (registration required)
Provided with Core	
Design Files	N/A
Example Design	IP integrator Block Diagram
Test Bench	Verilog
Constraints File	Not Provided
Simulation Model	System Verilog SecureIP model Bit-accurate C model MEX file for use with MATLAB
Supported S/W Driver[2]	Standalone
Tested Design Flows[3]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide
Synthesis	Vivado
Support	
Release Notes and Known Issues	Master Answer Record: 69399
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. Standalone driver details can be found in <Install Directory>/Vitis/2020.2/data/embeddedsw/XilinxProcessorIPLib/drivers/.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Forward Error Correction (FEC) codes such as Low Density Parity Check (LDPC) codes provide a means to control errors in data transmissions over unreliable or noisy communication channels. The LDPC Encoder/Decoder core provides an optimized block for encoding and soft-decision decoding of these codes. Custom and standardized LDPC codes are supported through the ability to specify the parity check matrix either through configuration of code memory or alternatively over an AXI4-Lite bus.

Applications

The LDPC Encoder/Decoder core is intended for use in applications requiring LDPC encode/decode, such as:

- 5G wireless (*3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; Multiplexing and channel coding (Release 15)* (3GPP Std TS 38.212 V15.0.0)).
- DOCSIS 3.1 cable modems (*Data-Over-Cable Service Interface Specifications DOCSIS 3.1, Physical Layer Specification* (DOCSIS 3.1)).
- WiFi 802.11ac-2012 High Throughput PHY (https://www.ieee802.org).
- Proprietary backhaul solutions.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

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Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the LDPC Encoder/Decoder product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help** → **Documentation and Tutorials**.
- On Windows, select **Start** → **All Programs** → **Xilinx Design Tools** → **DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

Revision History

Section	Revision Summary
02/08/2021 Version 2.0	
General updates	• Updated to align with Product Guide (PG281) updates. • Added Versal ACAP support.
12/04/2019 Version 2.0	
General updates	Updated to align with Product Guide (PG281) updates.
04/04/2018 Version 2.0	
General updates	Updated to align with Product Guide (PG281) updates.
10/04/2017 Version 1.0	
Initial release.	N/A

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