# LogiCORE IP 3GPP Mixed Mode Turbo Decoder v2.0

**PB009 (v2.0) February 4, 2021** **LogiCORE IP Product Brief**

## Introduction

The LogiCORE™ IP 3GPP Mixed Mode Turbo Decoder provides a flexible turbo convolutional decode function for both LTE and WCDMA air interfaces. The implementation is compliant with the requirements set out in both [Ref 1] and [Ref 2]. The core provides an optimized turbo decode function for base stations at all form factors, from femto to macrocells. The decoder, when used with a TCC encoder, provides an effective way of transmitting data reliably over noisy data channels.

## Additional Documentation

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/mm_tcc_dec_eval/index.htm

## Features

- Three versions of this core can be generated, each supporting different standard options:
  - LTE only
  - UMTS only
  - LTE and UMTS
- When UMTS and LTE are both supported the core can switch between different standards on a block by block basis.
- Each core is completely self contained, requiring nothing else to decode data.
- All 3GPP LTE block sizes supported: 188 different block sizes in the range 40–6144
- All 3GPP UMTS block sizes supported, that is block sizes in the range 40-5114.

See Feature Summary for additional features.

| LogiCORE IP Facts Table | |
|---|---|
| **Core Specifics** | |
| Supported Device Family(1) | Versal™ ACAP<br>UltraScale+™ Families<br>UltraScale™ Architecture<br>Zynq®-7000 SoC<br>7 Series |
| Supported User Interfaces | AXI4-Stream |
| **Provided with Core** | |
| Design Files | Encypted RTL |
| Example Design | VHDL |
| Test Bench | VHDL |
| Constraints File | Not Provided |
| Simulation Model | Encrypted VHDL<br>C Model and MATLAB® Model |
| Supported S/W Driver | N/A |
| **Tested Design Flows(2)** | |
| Design Entry | Vivado® Design Suite |
| Simulation | For supported simulators, see the Xilinx Design Tools: Release Notes Guide. |
| Synthesis | Vivado Synthesis |
| **Support** | |
| Release Notes and Known Issues | Master Answer Record: 54471 |
| All Vivado IP Change Logs | Master Vivado IP Change Logs: 72775 |
| Provided by Xilinx at the Xilinx Support web page | |

**Notes:**

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

# Feature Summary

- Configurable with either 1, 2, 4 or 8 decode units, allowing resource utilization to be optimized while meeting system performance requirements at all base station form factors.
- Dynamically selectable number of iterations 1-15.
- Support for MAX, MAX_SCALE and MAX_STAR algorithms.
- AXI4-Stream interfaces used for control and data input/output.
- C model and MATLAB MEX function available for bit accurate modelling of error correcting performance.
- Number representation: Twos complement fractional.
- Data Input: 7 or 8 bits (4 or 5 integer bits with 3 fractional bits)
- Hardware DSP units can be used instead of logic resources to tailor the core resource usage to specific user applications.
- Demonstration test bench to show an example of core usage.
- Integrated scheduler ensures that decode latency remains virtually constant with variable block sizes.

# Overview

The TCC decoder is used in conjunction with a TCC encoder to provide an effective way of transmitting data reliably over noisy data channels. The turbo decoder operates very well under low signal-to-noise conditions and provides a performance close to the theoretical optimal performance defined by the Shannon limit [Ref 3].

# References

1. 3GPP TS 25.212 "Multiplexing and channel coding (FDD)", v10.1.0
2. 3GPP TS 36.212 "Multiplexing and channel coding", v10.3.0
3. C. Berrou, A. Glavieux, and P. Thitimajshima, Near Shannon Limit Error-correcting Coding and Decoding Turbo Codes, IEEE Proc 1993 Int Conf. Comm., pp1064-1070

# Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

# Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided under the terms of the Xilinx Turbo Code LogiCORE IP License Terms.The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the 3GPP Mixed Mode Turbo Decoder product page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

*Disclaimer:* France Telecom, for itself and certain other parties, claims certain intellectual property rights covering Turbo Codes technology, and has decided to license these rights under a licensing program called the Turbo Codes Licensing Program. Supply of this IP core does not convey a license nor imply any right to use any Turbo Codes patents owned by France Telecom, TDF or GET. Contact France Telecom for information about its Turbo Codes Licensing Program at the following address:

France Telecom R&D,
VAT/TURBOCODES,
38, rue du Général Leclerc,
92794 Issy Moulineaux,
Cedex 9,
France.

## Evaluation License

An evaluation license is available for this core. The evaluation version of the core operates in the same way as the full version for several hours, depending on clock frequency. Operation is then disabled and the data output does not change. If you notice this behavior in hardware, it means that you are using an evaluation version of the core. The Xilinx tools warn that an evaluation license is being used during netlist implementation. If a full license is installed in order for the core to run on hardware, delete the old configuration file and re-create the core from new.

# Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 02/04/2021 | 2.0 | Versal device support added. |
| 11/18/2015 | 2.0 | UltraScale+ device support added. |
| 04/02/2014 | 2.0 | Characterization data added to PG030. |
| 12/18/2013 | 2.0 | Added UltraScale architecture support. |
| 03/20/2013 | 2.0 | Updated for Vivado design tools. |
| 01/18/2012 | 1.0 | Xilinx initial release. |

# Please Read: Important Legal Notices

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Development Software ***category:***

***Click to view products by*** Xilinx ***manufacturer:***

Other Similar products are found below :

RAPPID-567XFSW SRP004001-01 SW163052 SYSWINEV21 Core429-SA WS01NCTF1E W128E13 SW89CN0-ZCC IPS-EMBEDDED IP-UART-16550 MPROG-PRO535E AFLCF-08-LX-CE060-R21 WS02-CFSC1-EV3-UP SYSMAC-STUDIO-EIPCPLR LIB-PL-PC-N-1YR-DISKID LIB-PL-A-F SW006026-COV 1120270005 1120270006 MIKROBASIC PRO FOR FT90X (USB DONGLE) MIKROC PRO FOR FT90X (USB DONGLE) MIKROC PRO FOR PIC (USB DONGLE LICENSE) MIKROBASIC PRO FOR AVR (USB DONGLE LICEN MIKROBASIC PRO FOR FT90X MIKROC PRO FOR DSPIC30/33 (USB DONGLE LI MIKROPASCAL PRO FOR ARM (USB DONGLE LICE MIKROPASCAL PRO FOR FT90X MIKROPASCAL PRO FOR FT90X (USB DONGLE) MIKROPASCAL PRO FOR PIC32 (USB DONGLE LI SW006021-2H ATATMELSTUDIO 2400573 2702579 2988609 2702546 SW006022-DGL 2400303 2701356 VDSP-21XX-PCFLOAT VDSP-BLKFN-PC-FULL 88970111 DG-ACC-NET-CD 55195101-102 SW1A-W1C MDK-ARM PCI-EXP1-E3-US PCI-T32-E3-US SW006021-2NH SW006021-1H SW006021-2