

KCU105 Board

User Guide

UG917 (v1.10) February 6, 2019



Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|------------|---------|---|
| 02/06/2019 | 1.10 | Revised Electrostatic Discharge Caution . Added memory component information in DDR4 Component Memory . Replaced pin AM9 with D28 in Table 1-13 . Revised appendix title and removed constraints file listing in Appendix D, Xilinx Design Constraints . Updated Markings in Appendix G, Regulatory and Compliance Information . |
| 05/08/2018 | 1.9 | Updated System Clock Source and Table 1-19 . |
| 07/26/2017 | 1.8 | Updated Table 1-22 and Table 1-23 . Added Documentation Navigator and Design Hubs . |
| 01/12/2017 | 1.7 | Revised Programmable User Clock Source , FMC HPC Connector J22 , FMC LPC Connector J2 , and Switches . Revised Figure A-1 . |
| 03/31/2016 | 1.6 | Updated Table 1-11 . |
| 03/24/2016 | 1.5 | Updated Figure 1-21 . Changed the IOSTANDARD LVCMOS18 line in KCU105 Board Constraints File Listing on page 120. Added board thickness to Dimensions . Updated the Declaration of Conformity. |
| 09/25/2015 | 1.4 | Updated FMC HPC Connector J22 . Revised Figure 1-23 . Updated the binary format for I2C EEPROM in Table 1-19 . Updated the clocks constraints file listing in Appendix D, Master Constraints File Listing . |
| 06/27/2015 | 1.3 | Updated connectivity information for Quad 226, Quad 227, and Quad 228 in GTH Transceivers . Updated Figure 1-21 and Figure 1-36 . Updated HDMI Video Output , including updating Figure 1-22 and Table 1-18 . |
| 05/20/2015 | 1.2.1 | Made typographical edits. |
| 05/07/2015 | 1.2 | Updated Table 1-17 , Table 1-21 , and Figure 1-22 . |
| 04/07/2015 | 1.1 | Changed the Si5328C clock multiplier/jitter attenuator to Si5328B throughout, including updating the frequency range. Added impedance and insertion loss information to GTH SMA Clock Input , GTH TX and RX SMA Differential Pairs , PCI Express Endpoint Connectivity , SFP/SFP+ Module Connectors , FMC HPC Connector J22 , and FMC LPC Connector J2 . Updated Figure 1-2 , Figure 1-8 , Figure 1-9 , Figure 1-22 , Figure 1-23 , Figure 1-29 , Figure 1-34 , Figure 1-36 , Figure A-1 , Figure C-1 , and Figure C-2 . Changed IIC to I2C throughout. Updated Table 1-4 and Table 1-25 . Added Table 1-26 , Maxim Power Tool GUI Regulator Settings. Updated information for J11, J47, and J49 in Table A-2 . Updated callout number in KCU105 Board Zynq-7000 SoC XC7Z010 System Controller . Added instructions for accessing the system controller main menu in Appendix C, System Controller . Updated Clock Menu section. Updated the KCU105 Board Constraints File Listing in Appendix D . Updated the KCU105 evaluation kit master answer record number. |
| 12/18/2014 | 1.0 | Initial Xilinx release. |

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KCU105 Evaluation Board Features

Overview

The KCU105 evaluation board for the Xilinx® Kintex® UltraScale™ FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale XCKU040-2FFVA1156E device. The KCU105 evaluation board provides features common to many evaluation systems, including a DDR4 component memory, a high definition multimedia interface (HDMI™), two small form-factor pluggable (SFP+) connectors, an eight-lane PCI Express® interface, an Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be added by using VITA-57 FPGA mezzanine cards (FMCs) attached to the low pin count (LPC) FMC and high pin count (HPC) FMC connectors.

KCU105 Evaluation Board Features

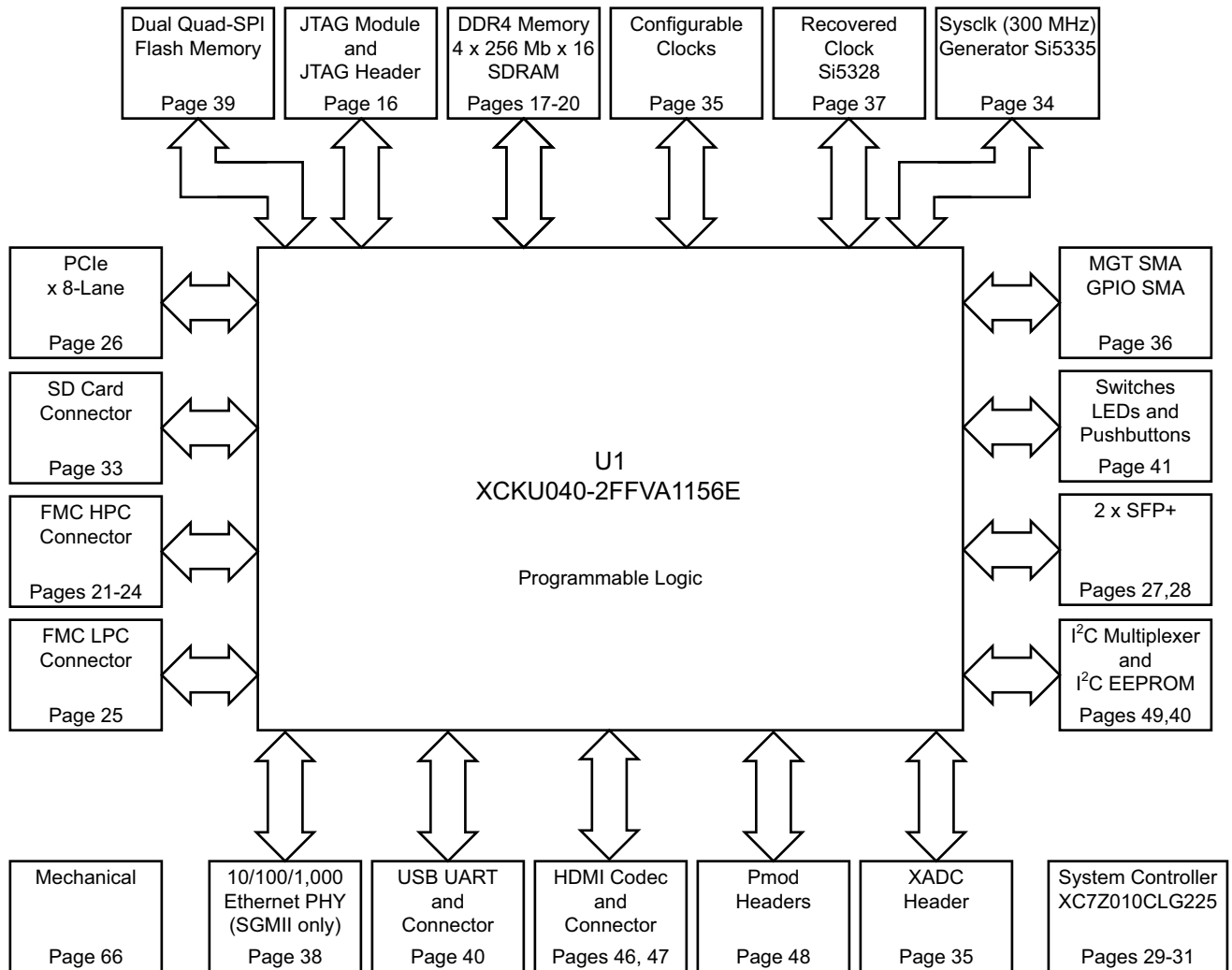
The KCU105 evaluation board features are listed here. Detailed information for each feature is provided in [Feature Descriptions](#).

- Kintex UltraScale XCKU040-2FFVA1156E device
- Zynq® SoC XC7Z010 based system controller
- 2 GB DDR4 component memory (four [256 Mb x 16] devices)
- Dual 256 Mb Quad serial peripheral interface flash memory (Dual Quad SPI)
- Micro secure digital (SD) connector
- USB JTAG interface via Digilent module with micro-B USB connector
- Clock sources:
 - Si5335A quad fixed frequency clock generator (300 MHz, 125 MHz, 90 MHz, 33.333 MHz)
 - Si5328B clock multiplier and jitter attenuator (8 kHz - 808 MHz)
 - Si570 I2C programmable LVDS clock generator (10 MHz - 810 MHz)
 - Subminiature version A (SMA) connectors (differential)
- 20 GTH transceivers (five Quads)
 - FMC HPC connector (eight GTH transceivers)

- FMC LPC connector (one GTH transceiver)
- 8-Lane PCI Express (eight GTH transceivers)
- Two SFP+ connectors (two GTH transceivers)
- TX and RX pair SMA connectors (one GTH transceiver)
- PCI Express endpoint connectivity
 - Gen1 8-lane (x8)
 - Gen2 8-lane (x8)
 - Gen3 8-lane (x8)
- Two SFP+ connectors
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector
- HDMI codec with HDMI connector
- I2C bus
- Status LEDs
- User I/O
- Program_B pushbutton
- Pmod Headers
- VITA 57.1 FMC HPC connector J22
- VITA 57.1 FMC LPC connector J2
- Power on/off slide switch SW1
- Power management with PMBus voltage monitoring through Maxim power controllers and GUI, current monitoring via the FPGA SYSMON block
- Single 10-bit 0.2 MSPS SYSMON analog-to-digital converter
- Configuration options:
 - Dual Quad-SPI flash memory
 - USB JTAG configuration port (Digilent module)
 - Platform cable header J3 JTAG configuration port
 - System controller micro-SD card

Board Diagram

The KCU105 board diagram is shown in [Figure 1-1](#)



Note: Page numbers reference the page number of schematic 0381556

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Figure 1-1: KCU105 Evaluation Board Block Diagram

Feature Descriptions

Figure 1-2 shows the KCU105 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 with a link to detailed information provided under Feature Descriptions.



IMPORTANT: Figure 1-2 is for visual reference only and might not reflect the current revision of the board.

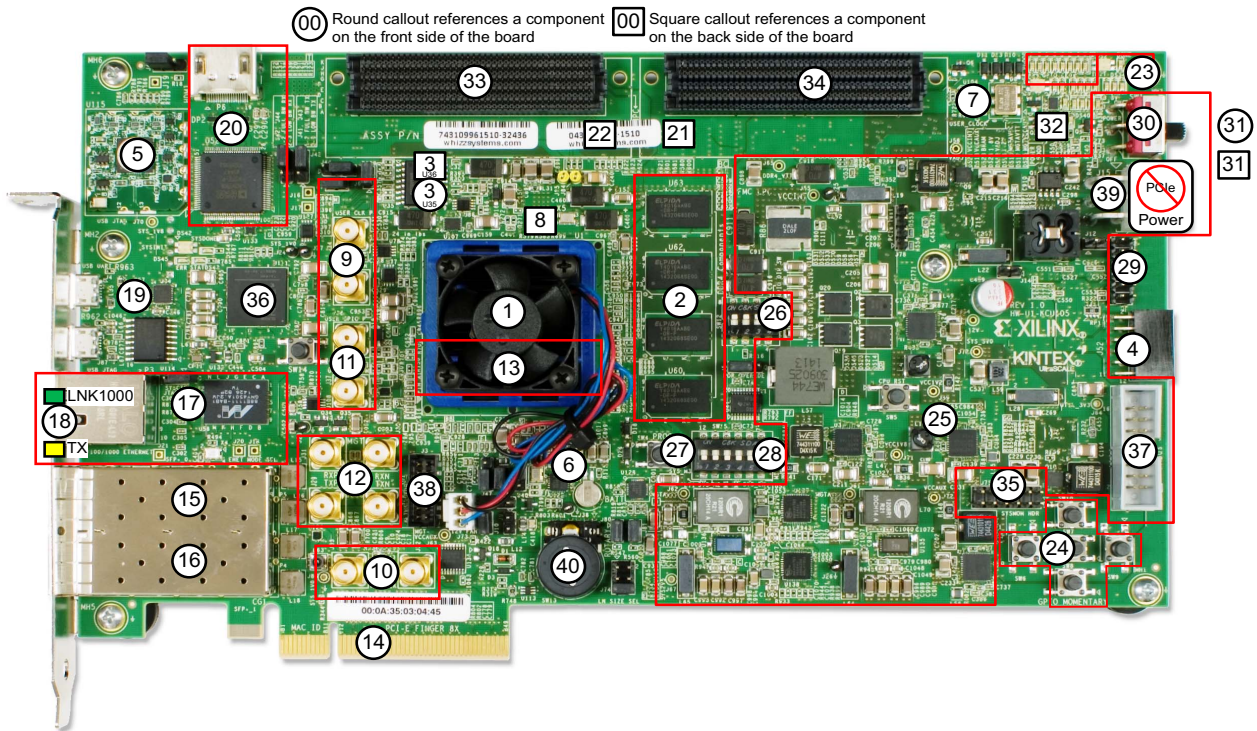
Electrostatic Discharge Caution



CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.



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Figure 1-2: KCU105 Evaluation Board Components

Table 1-1: KCU105 Board Component Descriptions

| Callout | Component Description | Notes | Schematic ⁽¹⁾ 0381556 Page Number |
|---------|---|--|--|
| 1 | Kintex UltraScale XCKU040-2FFVA1156E Device | XCKU040-2FFVA1156E | |
| | With fan-sink on top of the FPGA soldered on the board | Radian FB95+K52B+T710 | |
| 2 | DDR4 Component Memory , DDR4 Memory 2GB (4x512M U60-U63) | Micron MT40A256M16HA-083E | 17-20 |
| 3 | Dual Quad-SPI Flash Memory , Dual Quad-SPI Flash (2x256Mb) (U35-U36) | Micron N25Q256A11ESF40F U35 on top, U36 on bottom of board | 39 |
| 4 | Micro-SD Card Interface , Micro SD Card Interface Connector (J83) | Molex 5025700893 | 33 |
| 5 | USB JTAG Interface , w/Micro-B Connector | Digilent USB JTAG Module | 16 |
| 6 | Clock Generation , SYSCLK and other clocks, 1.8V LVDS (U122) | Si5335A-B02436-GM, 4 outputs: 300MHz, 125MHz, 90MHz, 33.33MHz | 34 |
| 7 | Programmable User Clock Source , I2C Prog. User Clock 3.3V LVDS (U32) with 1-to-2 LVDS buffer (U104) | Silicon Labs Si570BAB0000544DG (default 156.250MHz) with Si53340 buffer | 35 |
| 8 | Jitter Attenuated Clock , Jitter Attenuated Clock (U57) | Silicon Labs Si5328B-C-GM | 37 |
| 9 | User SMA Clock Input , User Differential SMA Clock P/N (J34/J35) | Rosenberger 32K10K-400L5 | 36 |
| 10 | GTH SMA Clock Input , SMA_MGT_REFCLK_P/N (J33/J32) | Rosenberger 32K10K-400L5 | 36 |
| 11 | User SMA GPIO , User SMA GPIO Connectors P/N (J36/J37) | Rosenberger 32K10K-400L5 | 36 |
| 12 | GTH TX and RX SMA Differential Pairs , User SMA TX and RX_P/N (J31/J30, J29/J28) | Rosenberger 32K10K-400L5 | 36 |
| 13 | GTH Transceivers | Embedded within FPGA U1 | 10 |
| 14 | PCI Express Endpoint Connectivity , PCI Express Connector (P1) | 8-lane card edge connector | 26 |
| 15 | SFP/SFP+ Module Connectors , SFP/SFP+ Module Connector SFP0(P5) | Molex 74441-0010 | 27 |
| 16 | SFP/SFP+ Module Connectors , SFP/SFP+ Module Connector SFP1 (P4) | Molex 74441-0010 | 28 |
| 17 | 10/100/1000 Mb/s Tri-Speed Ethernet PHY , SGMII Mode Only (U58,P3) | Marvell M88E1111-BAB1C000 with Halo HFJ11-1G01E-L12RL RJ45 | 38 |

Table 1-1: KCU105 Board Component Descriptions (Cont'd)

| Callout | Component Description | Notes | Schematic ⁽¹⁾ 0381556 Page Number |
|---------|--|--|--|
| 18 | Ethernet PHY Status LEDs, LEDs are integrated into P3 bezel | Halo HFJ11-1G01E-L12RL RJ45 integrated Status LEDs (Rev B) | 38 |
| 19 | Dual USB-to-UART Bridge, Bridge device (U34) with Mini-B Connector (J4) | Silicon Labs CP2105-F01-GM bridge, Hirose ZX62D-AB-5P8 connector | 40 |
| 20 | HDMI Video Output, HDMI Controller (U52), HDMI Connector (P6) | Analog Devices ADV7511KSTZ-P, Molex 47151-001 | 46, 47 |
| 21 | I2C Bus, Topology, and Switches, I2C Bus MUX (U28) | TI TCA9548APWR bottom of board | 49 |
| 22 | I2C Bus, Topology, and Switches, I2C Bus MUX (U80) | TI PCA9544ARGYR bottom of board | 50 |
| 23 | Status and User LEDs, User LEDs (DS6-DS10, DS31-DS33) | GPIO LEDs, GREEN 0603 Lumex SML-LX0603GW-TR | 41 |
| 24 | User Pushbuttons, User Pushbuttons, active-High (SW6-SW10) | E-Switch TL3301EF100QG in North, South, East, West, Center pattern | 41 |
| 25 | User Pushbuttons, User CPU RESET, active-High (SW5) | E-Switch TL3301EF100QG | 41 |
| 26 | GPIO DIP Switch, GPIO DIP Switch (SW12) | 4-pole C&K SDA04H1SBD | 41 |
| 27 | Program_B Pushbutton Switch, FPGA PROG Pushbutton (SW4) | E-Switch TL3301EF100QG | 41 |
| 28 | FPGA Configuration DIP Switch, DIP Switch (SW15) | 6-pole C&K SDA06H1SBD | 32 |
| 29 | User PMOD GPIO Headers, PMOD Hdrs. (J52,J53) w/Level-Shifters (U41,U42) | 2x6 0.1 inch male header Sullins PBC36DAAN; TI TXS0108EPWR | 48 |
| 30 | Power On/Off Slide Switch SW1, Power On/Off Switch (SW1) | C&K 1201M2S3AQE2 | 51 |
| 31 | KCU105 Board Power System, Power Management System (top and bottom) | Maxim MAX15301 and MAX15303 Digital P.O.L. Controllers | 52 - 65 |
| 32 | SYSMON Power System Measurement SYSMON External Circuitry | Analog Devices MUX ADG707BRUZ TI Op Amps INA333AIDGKR | 44 - 45 |
| 33 | FMC HPC Connector J22, FMC HPC connector (J22) | Samtec ASP_134486_01 | 21 - 24 |
| 34 | FMC LPC Connector J2, FMC LPC connector (J2) | Samtec ASP_134603_01 | 25 |

Table 1-1: KCU105 Board Component Descriptions (Cont'd)

| Callout | Component Description | Notes | Schematic ⁽¹⁾ 0381556 Page Number |
|---------|--|--|--|
| 35 | SYSMON Power System Measurement , SYSMON Header (J75) | 2x6 0.1inch male header, part of breakaway 2x36 Sullins PBC36DAAN | 43 |
| 36 | KCU105 Board Zynq-7000 SoC XC7Z010 System Controller , Zynq-7000 SoC XC7Z010CLG225 (U111) | XC7Z010CLG225 | 29 - 31 |
| 37 | 2x8 shrouded PMBus connector J39, see Monitoring Voltage and Current | ASSMAN AWHW16G-0202 | 50 |
| 38 | 2x7 2mm shrouded JTAG cable connector J82, see Monitoring Voltage and Current | MOLEX 87832-1420 | 32 |
| 39 | 12V power input 2x3 connector (J15), see Power On/Off Slide Switch SW1 | MOLEX-39-30-1060 | 51 |
| 40 | Rotary Switch , Active-High (SW13) | PANASONIC EVQ-WK4001 | 41 |

Notes:

1. The KCU105 board schematics are available for download. See the [KCU105 Evaluation Kit](#) website.
2. The KCU105 board jumper header locations are shown in [Figure A-1](#).

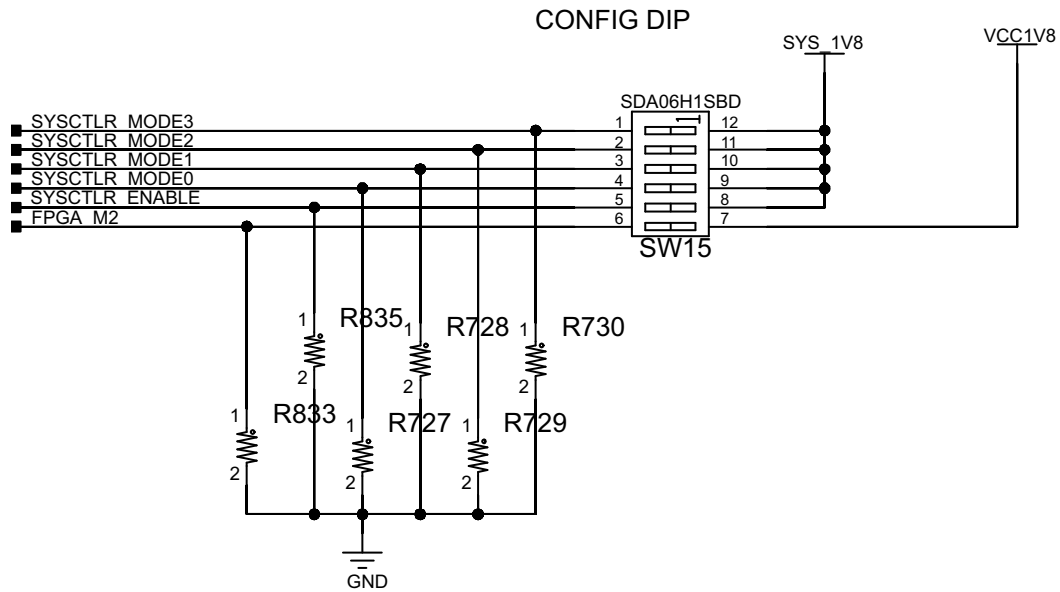
Kintex UltraScale XCKU040-2FFVA1156E Device

[[Figure 1-2](#), callout 1]

The KCU105 board is populated with the Kintex UltraScale XCKU040-2FFVA1156E device. For more information on Kintex UltraScale FPGAs, see *Kintex UltraScale Data Sheet: DC and AC Switching Characteristics* (DS892) [[Ref 1](#)].

FPGA Configuration

The UltraScale FPGA is configured using either the master SPI or JTAG mode as determined by the configuration DIP switch SW15.



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Figure 1-3: Configuration DIP Switch

Interfaces supporting these configuration modes are:

- Master SPI: Quad SPI flash memory (U35 and U36)
- JTAG:
 - Digilent USB-to-JTAG configuration module (U115)
 - Platform cable header (J3)
 - System controller (U111)

Each configuration interface corresponds to one or more configuration modes and bus widths, as listed in Table 1-2. The FPGA mode pins M1 and M0 are hard-wired to logic 0 and 1, respectively. FPGA mode pin M2 is wired to SW15 pin 6 position 6, which has a default setting of OPEN, enabling the M2 net to be pulled down to logic 0 (for example, the FPGA default mode setting $M[2:0] = 001$, selecting Quad SPI configuration mode).

Table 1-2: Configuration Modes

| Configuration Mode | M[2:0] | Bus Width | CCLK Direction |
|--------------------|--------|------------|----------------|
| Master SPI | 001 | x1, x2, x4 | Output |
| JTAG | 101 | x1 | Not Applicable |

Prior to KCU105 board power-up, the UltraScale FPGA U1 configuration method is selected with DIP switch SW15 switch settings:

- Master SPI Mode
 - With both SW15.6 (FPGA_M2) and SW15.5 (SYSCTLR_ENABLE) in the OFF (disable the SYSCTLR_ENABLE) position, a bitstream programmed into the dual-QSPI flash devices (U35, U36) is used to configure the UltraScale FPGA U1.
- JTAG Mode
 - With switch SW15.6 ON and SW15.5 in the OFF position, either the USB JTAG Digilent U115 or the JTAG cable header J3 can be used.

With both switches SW15.6 and SW15.5 in the ON position, the Xilinx integrated configuration engine is used to configure the UltraScale FPGA U1 over JTAG with one of several bitstreams stored on a micro-SD card inserted in to the SD card connector J83. Selecting the bitstream to use for this JTAG configuration is accomplished by setting SW15.1 (MSB) through SW15.4 (LSB) to one of the sixteen possible binary values. The technical reference design (TRD) files are available on the [KCU105 Evaluation Kit](#) website.

Once the board is powered up or when the system controller POR pushbutton (SW14) is pressed, the system controller menu, accessed through the USB UART (J4), is available for user initiated configuration of the UltraScale FPGA. The "Configure UltraScale FPGA from micro-SD card" option (see [CONFIG Menu Options](#)) utilizes the Xilinx integrated configuration engine to prompt for one of sixteen micro-SD card resident bitstreams to configure the UltraScale FPGA (U1). When configuration is initiated through the system controller menu, the bitstream number entered at the text prompt determines the selected bitstream. DIP switch SW15 positions 1 to 4 do not determine the selected bitstream.

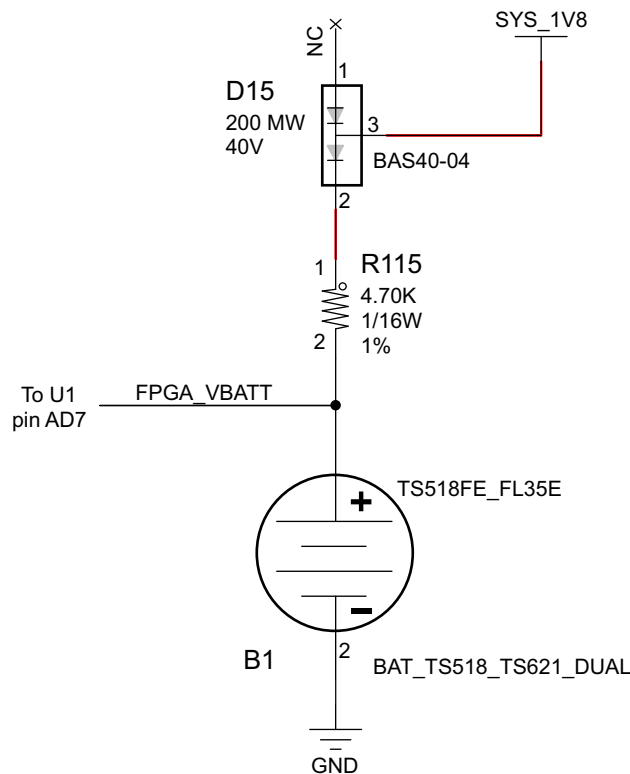
See [Appendix C, System Controller](#) for information on installing and using the user interface.

For complete details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [\[Ref 2\]](#).

Encryption Key Battery Backup Circuit

The XCKU040 device U1 implements bitstream encryption key technology. The KCU105 board provides the encryption key backup battery circuit shown in Figure 1-4. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCKU040 device U1 VBATT pin AD7. The battery supply current I_{BATT} specification is described in the *Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 1]. The battery provides backup power to a RAM-based encryption key when the board power is off. B1 is charged from the SYS_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 K Ω current limit resistor. The nominal charging voltage is 1.42V. The VBATT is only required for use with encrypted bitstreams as it provides backup power to a RAM-based encryption key in the absence of powering the entire FPGA. The stored key is used for decrypting an encrypted bitstream during configuration.

See *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2] for more details about Xilinx UltraScale bitstream encryption solutions.

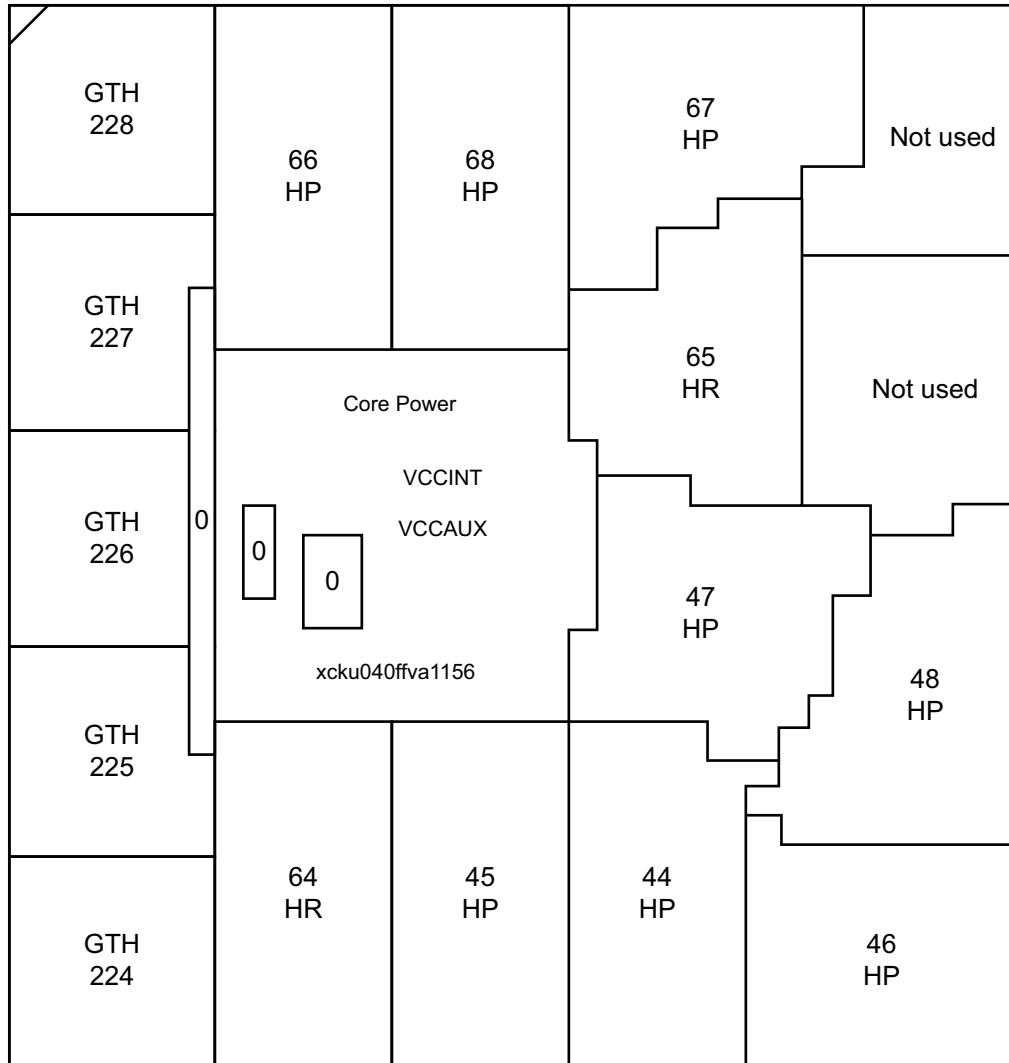


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Figure 1-4: Encryption Key Backup Circuit

I/O Voltage Rails

There are ten I/O banks available on the KCU040 device and the KCU105 board. The voltages applied to the FPGA I/O banks (shown in Figure 1-5) used by the KCU105 board are listed in Table 1-3.



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Figure 1-5: UltraScale XCKU040 Bank Locations

Table 1-3: I/O Bank Voltage Rails

| FPGA (U1) Bank | Power Supply Rail Net Name | Voltage |
|----------------|----------------------------|---------|
| Bank 0 | VCC1V8_FPGA | 1.8V |
| HP Bank 44 | VCC1V2_FPGA | 1.2V |
| HP Bank 45 | VCC1V2_FPGA | 1.2V |
| HP Bank 46 | VCC1V2_FPGA | 1.2V |
| HP Bank 47 | VADJ_1V8_FPGA | 1.8V |
| HP Bank 48 | VADJ_1V8_FPGA | 1.8V |
| HR Bank 64 | VCC1V8_FPGA | 1.8V |
| HR Bank 65 | VCC1V8_FPGA | 1.8V |
| HP Bank 66 | VADJ_1V8_FPGA | 1.8V |
| HP Bank 67 | VADJ_1V8_FPGA | 1.8V |
| HP Bank 68 | VADJ_1V8_FPGA | 1.8V |

DDR4 Component Memory

[Figure 1-2, callout 2]

The 2 GB DDR4 component memory system is comprised of four 256 Mb x 16 DDR4 SDRAM devices located at U60-U63.

- Part number: MT40A256M16GE-083E (Micron Technology)
- Configuration: 4Gb: 256 Mb x 16
- Supply voltage: 1.2V
- Datapath width: 64 bits
- Data rate: Up to 2400 MT/s

The KCU105 XCKU040 FPGA memory interface performance is documented in the *Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 1].

This memory system is connected to the XCKU040 HP banks 44, 45, and 46. The DDR4 0.6V VTT termination voltage (net DDR4_VTT) is sourced from the TI TPS51200DR linear regulator U24. The connections between the DDR4 component memories and the XCKU040 banks 44, 45, and 46 are listed in Table 1-4.

Table 1-4: DDR4 Memory Connections to the FPGA

| FPGA (U1) Pin | Schematic Net Name | I/O Standard | Component Memory | | |
|---------------|--------------------|----------------|------------------|--------------|-----------|
| | | | Pin # | Pin Name | Ref. Des. |
| AE23 | DDR4_DQ0 | POD12_DCI | G2 | DQL0 | U60 |
| AG20 | DDR4_DQ1 | POD12_DCI | F7 | DQL1 | U60 |
| AF22 | DDR4_DQ2 | POD12_DCI | H3 | DQL2 | U60 |
| AF20 | DDR4_DQ3 | POD12_DCI | H7 | DQL3 | U60 |
| AE22 | DDR4_DQ4 | POD12_DCI | H2 | DQL4 | U60 |
| AD20 | DDR4_DQ5 | POD12_DCI | H8 | DQL5 | U60 |
| AG22 | DDR4_DQ6 | POD12_DCI | J3 | DQL6 | U60 |
| AE20 | DDR4_DQ7 | POD12_DCI | J7 | DQL7 | U60 |
| AJ24 | DDR4_DQ8 | POD12_DCI | A3 | DQU0 | U60 |
| AG24 | DDR4_DQ9 | POD12_DCI | B8 | DQU1 | U60 |
| AJ23 | DDR4_DQ10 | POD12_DCI | C3 | DQU2 | U60 |
| AF23 | DDR4_DQ11 | POD12_DCI | C7 | DQU3 | U60 |
| AH23 | DDR4_DQ12 | POD12_DCI | C2 | DQU4 | U60 |
| AF24 | DDR4_DQ13 | POD12_DCI | C8 | DQU5 | U60 |
| AH22 | DDR4_DQ14 | POD12_DCI | D3 | DQU6 | U60 |
| AG25 | DDR4_DQ15 | POD12_DCI | D7 | DQU7 | U60 |
| AG21 | DDR4_DQS0_T | DIFF_POD12_DCI | G3 | DQSL_T | U60 |
| AH21 | DDR4_DQS0_C | DIFF_POD12_DCI | F3 | DQSL_C | U60 |
| AH24 | DDR4_DQS1_T | DIFF_POD12_DCI | B7 | DQSU_T | U60 |
| AJ25 | DDR4_DQS1_C | DIFF_POD12_DCI | A7 | DQSU_C | U60 |
| AD21 | DDR4_DM0 | POD12_DCI | E7 | DML_B/DBIL_B | U60 |
| AE25 | DDR4_DM1 | POD12_DCI | E2 | DMU_B/DBIU_B | U60 |
| AL22 | DDR4_DQ16 | POD12_DCI | G2 | DQL0 | U61 |
| AL25 | DDR4_DQ17 | POD12_DCI | F7 | DQL1 | U61 |
| AM20 | DDR4_DQ18 | POD12_DCI | H3 | DQL2 | U61 |
| AK23 | DDR4_DQ19 | POD12_DCI | H7 | DQL3 | U61 |
| AK22 | DDR4_DQ20 | POD12_DCI | H2 | DQL4 | U61 |
| AL24 | DDR4_DQ21 | POD12_DCI | H8 | DQL5 | U61 |
| AL20 | DDR4_DQ22 | POD12_DCI | J3 | DQL6 | U61 |
| AL23 | DDR4_DQ23 | POD12_DCI | J7 | DQL7 | U61 |
| AM24 | DDR4_DQ24 | POD12_DCI | A3 | DQU0 | U61 |
| AN23 | DDR4_DQ25 | POD12_DCI | B8 | DQU1 | U61 |
| AN24 | DDR4_DQ26 | POD12_DCI | C3 | DQU2 | U61 |

Table 1-4: DDR4 Memory Connections to the FPGA (Cont'd)

| FPGA (U1) Pin | Schematic Net Name | I/O Standard | Component Memory | | |
|---------------|--------------------|----------------|------------------|--------------|-----------|
| | | | Pin # | Pin Name | Ref. Des. |
| AP23 | DDR4_DQ27 | POD12_DCI | C7 | DQU3 | U61 |
| AP25 | DDR4_DQ28 | POD12_DCI | C2 | DQU4 | U61 |
| AN22 | DDR4_DQ29 | POD12_DCI | C8 | DQU5 | U61 |
| AP24 | DDR4_DQ30 | POD12_DCI | D3 | DQU6 | U61 |
| AM22 | DDR4_DQ31 | POD12_DCI | D7 | DQU7 | U61 |
| AJ20 | DDR4_DQS2_T | DIFF_POD12_DCI | G3 | DQSL_T | U61 |
| AK20 | DDR4_DQS2_C | DIFF_POD12_DCI | F3 | DQSL_C | U61 |
| AP20 | DDR4_DQS3_T | DIFF_POD12_DCI | B7 | DQSU_T | U61 |
| AP21 | DDR4_DQS3_C | DIFF_POD12_DCI | A7 | DQSU_C | U61 |
| AJ21 | DDR4_DM2 | POD12_DCI | E7 | DML_B/DBIL_B | U61 |
| AM21 | DDR4_DM3 | POD12_DCI | E2 | DMU_B/DBIU_B | U61 |
| AH28 | DDR4_DQ32 | POD12_DCI | G2 | DQL0 | U62 |
| AK26 | DDR4_DQ33 | POD12_DCI | F7 | DQL1 | U62 |
| AK28 | DDR4_DQ34 | POD12_DCI | H3 | DQL2 | U62 |
| AM27 | DDR4_DQ35 | POD12_DCI | H7 | DQL3 | U62 |
| AJ28 | DDR4_DQ36 | POD12_DCI | H2 | DQL4 | U62 |
| AH27 | DDR4_DQ37 | POD12_DCI | H8 | DQL5 | U62 |
| AK27 | DDR4_DQ38 | POD12_DCI | J3 | DQL6 | U62 |
| AM26 | DDR4_DQ39 | POD12_DCI | J7 | DQL7 | U62 |
| AL30 | DDR4_DQ40 | POD12_DCI | A3 | DQU0 | U62 |
| AP29 | DDR4_DQ41 | POD12_DCI | B8 | DQU1 | U62 |
| AM30 | DDR4_DQ42 | POD12_DCI | C3 | DQU2 | U62 |
| AN28 | DDR4_DQ43 | POD12_DCI | C7 | DQU3 | U62 |
| AL29 | DDR4_DQ44 | POD12_DCI | C2 | DQU4 | U62 |
| AP28 | DDR4_DQ45 | POD12_DCI | C8 | DQU5 | U62 |
| AM29 | DDR4_DQ46 | POD12_DCI | D3 | DQU6 | U62 |
| AN27 | DDR4_DQ47 | POD12_DCI | D7 | DQU7 | U62 |
| AL27 | DDR4_DQS4_T | DIFF_POD12_DCI | G3 | DQSL_T | U62 |
| AL28 | DDR4_DQS4_C | DIFF_POD12_DCI | F3 | DQSL_C | U62 |
| AN29 | DDR4_DQS5_T | DIFF_POD12_DCI | B7 | DQSU_T | U62 |
| AP30 | DDR4_DQS5_C | DIFF_POD12_DCI | A7 | DQSU_C | U62 |
| AH26 | DDR4_DM4 | POD12_DCI | E7 | DML_B/DBIL_B | U62 |
| AN26 | DDR4_DM5 | POD12_DCI | E2 | DMU_B/DBIU_B | U62 |
| AH31 | DDR4_DQ48 | POD12_DCI | G2 | DQL0 | U63 |

Table 1-4: DDR4 Memory Connections to the FPGA (Cont'd)

| FPGA (U1) Pin | Schematic Net Name | I/O Standard | Component Memory | | |
|---------------|--------------------|----------------|------------------|--------------|-----------|
| | | | Pin # | Pin Name | Ref. Des. |
| AH32 | DDR4_DQ49 | POD12_DCI | F7 | DQL1 | U63 |
| AJ34 | DDR4_DQ50 | POD12_DCI | H3 | DQL2 | U63 |
| AK31 | DDR4_DQ51 | POD12_DCI | H7 | DQL3 | U63 |
| AJ31 | DDR4_DQ52 | POD12_DCI | H2 | DQL4 | U63 |
| AJ30 | DDR4_DQ53 | POD12_DCI | H8 | DQL5 | U63 |
| AH34 | DDR4_DQ54 | POD12_DCI | J3 | DQL6 | U63 |
| AK32 | DDR4_DQ55 | POD12_DCI | J7 | DQL7 | U63 |
| AN33 | DDR4_DQ56 | POD12_DCI | A3 | DQU0 | U63 |
| AP33 | DDR4_DQ57 | POD12_DCI | B8 | DQU1 | U63 |
| AM34 | DDR4_DQ58 | POD12_DCI | C3 | DQU2 | U63 |
| AP31 | DDR4_DQ59 | POD12_DCI | C7 | DQU3 | U63 |
| AM32 | DDR4_DQ60 | POD12_DCI | C2 | DQU4 | U63 |
| AN31 | DDR4_DQ61 | POD12_DCI | C8 | DQU5 | U63 |
| AL34 | DDR4_DQ62 | POD12_DCI | D3 | DQU6 | U63 |
| AN32 | DDR4_DQ63 | POD12_DCI | D7 | DQU7 | U63 |
| AH33 | DDR4_DQS6_T | DIFF_POD12_DCI | G3 | DQSL_T | U63 |
| AJ33 | DDR4_DQS6_C | DIFF_POD12_DCI | F3 | DQSL_C | U63 |
| AN34 | DDR4_DQS7_T | DIFF_POD12_DCI | B7 | DQSU_T | U63 |
| AP34 | DDR4_DQS7_C | DIFF_POD12_DCI | A7 | DQSU_C | U63 |
| AJ29 | DDR4_DM6 | POD12_DCI | E7 | DML_B/DBIL_B | U63 |
| AL32 | DDR4_DM7 | POD12_DCI | E2 | DMU_B/DBIU_B | U63 |
| AE17 | DDR4_A0 | SSTL12_DCI | P3 | A0 | U60-U62 |
| AH17 | DDR4_A1 | SSTL12_DCI | P7 | A1 | U60-U62 |
| AE18 | DDR4_A2 | SSTL12_DCI | R3 | A2 | U60-U62 |
| AJ15 | DDR4_A3 | SSTL12_DCI | N7 | A3 | U60-U62 |
| AG16 | DDR4_A4 | SSTL12_DCI | N3 | A4 | U60-U62 |
| AL17 | DDR4_A5 | SSTL12_DCI | P8 | A5 | U60-U62 |
| AK18 | DDR4_A6 | SSTL12_DCI | P2 | A6 | U60-U62 |
| AG17 | DDR4_A7 | SSTL12_DCI | R8 | A7 | U60-U62 |
| AF18 | DDR4_A8 | SSTL12_DCI | R2 | A8 | U60-U62 |
| AH19 | DDR4_A9 | SSTL12_DCI | R7 | A9 | U60-U62 |
| AF15 | DDR4_A10 | SSTL12_DCI | M3 | A10/AP | U60-U62 |
| AD19 | DDR4_A11 | SSTL12_DCI | T2 | A11 | U60-U62 |
| AJ14 | DDR4_A12 | SSTL12_DCI | M7 | A12/BC_B | U60-U62 |

Table 1-4: DDR4 Memory Connections to the FPGA (Cont'd)

| FPGA (U1) Pin | Schematic Net Name | I/O Standard | Component Memory | | |
|---------------|--------------------|-----------------|------------------|-----------|-----------|
| | | | Pin # | Pin Name | Ref. Des. |
| AG19 | DDR4_A13 | SSTL12_DCI | T8 | A13 | U60-U62 |
| AD16 | DDR4_A14_WE_B | SSTL12_DCI | L2 | WE_B/A14 | U60-U62 |
| AG14 | DDR4_A15_CAS_B | SSTL12_DCI | M8 | CAS_B/A15 | U60-U62 |
| AF14 | DDR4_A16_RAS_B | SSTL12_DCI | L8 | RAS_B/A16 | U60-U62 |
| AF17 | DDR4_BA0 | SSTL12_DCI | N2 | BA0 | U60-U62 |
| AL15 | DDR4_BA1 | SSTL12_DCI | N8 | BA1 | U60-U62 |
| AG15 | DDR4_BG0 | SSTL12_DCI | M2 | BG0 | U60-U62 |
| AH14 | DDR4_ACT_B | SSTL12_DCI | L3 | ACT_B | U60-U62 |
| AH16 | DDR4_TEN | SSTL12_DCI | N9 | TEN | U60-U62 |
| AJ16 | DDR4_ALERT_B | SSTL12_DCI | P9 | ALERT_B | U60-U62 |
| AD18 | DDR4_PAR | SSTL12_DCI | T3 | PAR | U60-U62 |
| AJ18 | DDR4_ODT | SSTL12_DCI | K3 | ODT | U60-U62 |
| AL19 | DDR4_CS_B | SSTL12_DCI | L7 | CS_B | U60-U62 |
| AD15 | DDR4_CKE | SSTL12_DCI | K2 | CKE | U60-U62 |
| AL18 | DDR4_RESET_B | LVC MOS12 | P1 | RESET_B | U60-U62 |
| AE16 | DDR4_CK_T | DIFF_SSTL12_DCI | K7 | CK_T | U60-U62 |
| AE15 | DDR4_CK_C | DIFF_SSTL12_DCI | K8 | CK_C | U60-U62 |

The KCU105 board DDR4 memory component interface adheres to the constraints guidelines documented in the DDR4 Design Guidelines section of *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 3] and in *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (Vivado Design Suite)* (PG150) [Ref 4]. The KCU105 board DDR4 memory component interface is a 40Ω impedance implementation. For more details about the Micron DDR4 component memory, see the Micron EDY4016AABG-DR-F-D data sheet at the Micron website [Ref 5].

Dual Quad-SPI Flash Memory

[Figure 1-2, callout 3]

The Quad-SPI flash memory located at U35 and U36 provides 2 x 256 Mb of nonvolatile storage that can be used for configuration and data storage. For details on FPGA configuration operation and implementation related to the dual Quad-SPI interfaces, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

- Part number: N25Q256A11ESF40F (Micron)
- Supply voltage: 1.8V

- Datapath width: 4 bits
- Data rate: various depending on single/dual/quad mode

The connections between the SPI flash memories and the XCKU040 device are listed in [Table 1-5](#).

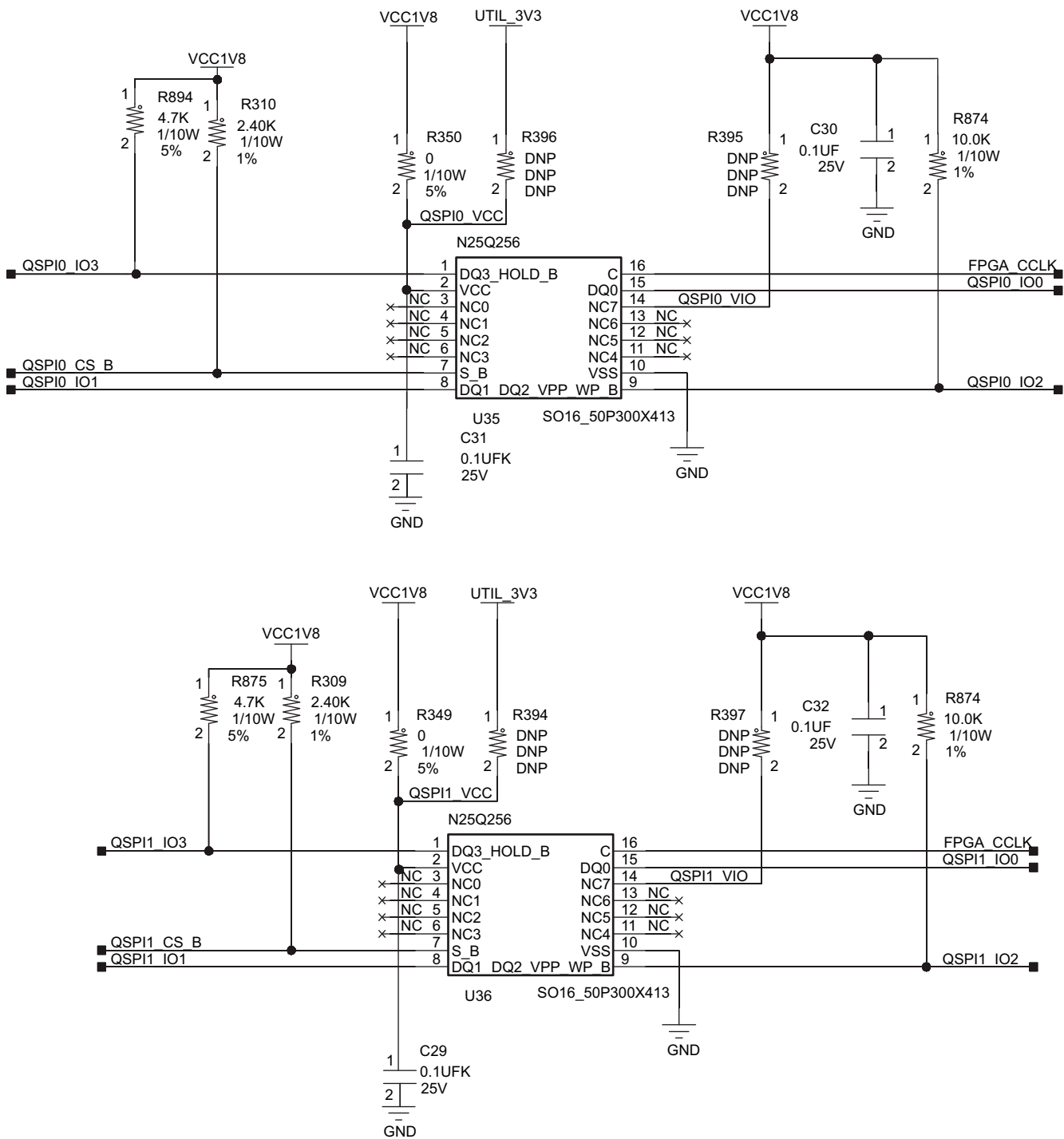
Table 1-5: Quad-SPI Flash Memory Connections to FPGA U1

| FPGA (U1) Pin | Schematic Net Name | I/O Standard | Pin # | Pin Name | Ref. Des. |
|---------------|--------------------|-------------------|-------|----------|-----------|
| AC7 | QSPI0_IO0 | LVC MOS18 | 15 | SI_IO0 | U35 |
| AB7 | QSPI0_IO1 | LVC MOS18 | 8 | SI_IO1 | U35 |
| AA7 | QSPI0_IO2 | LVC MOS18 | 9 | SI_IO2 | U35 |
| Y7 | QSPI0_IO3 | LVC MOS18 | 1 | SI_IO3 | U35 |
| AA9 | FPGA_CCLK | NA ⁽¹⁾ | 16 | SCK | U35, U36 |
| U7 | QSPI0_CSB | LVC MOS18 | 7 | CS_B | U35 |
| M20 | QSPI1_IO0 | LVC MOS18 | 15 | SI_IO0 | U36 |
| L20 | QSPI1_IO1 | LVC MOS18 | 8 | SI_IO1 | U36 |
| R21 | QSPI1_IO2 | LVC MOS18 | 9 | SI_IO2 | U36 |
| R22 | QSPI1_IO3 | LVC MOS18 | 1 | SI_IO3 | U36 |
| G26 | QSPI1_CSB | LVC MOS18 | 7 | CS_B | U36 |

Notes:

1. CCLK is a dedicated pin and does not require an IOSTANDARD or LOC attribute.

[Figure 1-6](#) shows the connections of the linear Quad-SPI flash memory on the KCU105 evaluation board. For more details, see the Micron N25Q256A11ESF40F data sheet at the Micron website [\[Ref 5\]](#).



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Figure 1-6: Dual Quad-SPI 256 Mb Flash Memory

Micro-SD Card Interface

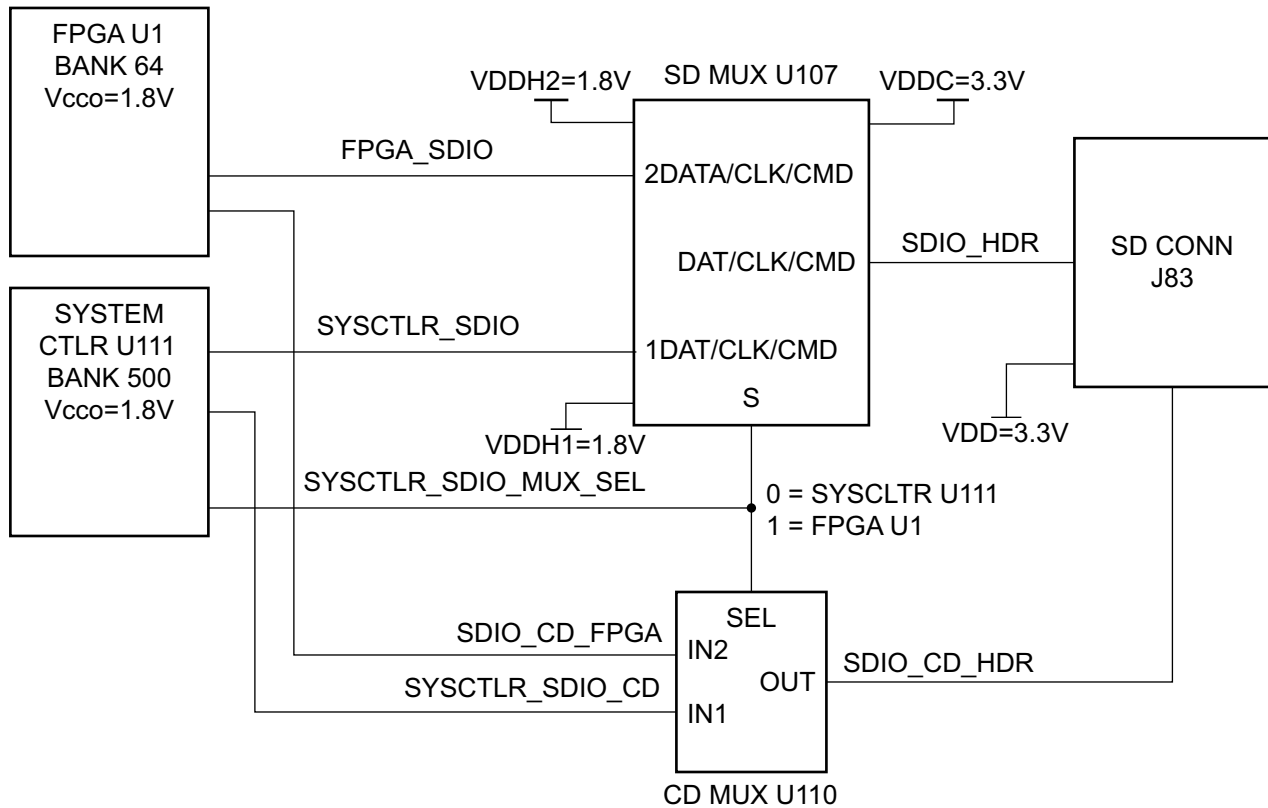
[Figure 1-2, callout 4]

The KCU105 board includes a secure digital input/output (SDIO) interface to provide access to general purpose nonvolatile micro-SD memory cards and peripherals. The micro-SD card slot supports 50 MHz high-speed micro-SD cards. The SDIO signals are connected to I/O bank 64, which has its VCCO set to 1.8V. Fairchild FSSD07 (U107) and STMicroelectronics STG3220 (U110) 2:1 multiplexers are used between the FPGA and the micro-SD card connector (J83), and the XC7Z010 system controller (U111), and the micro-SD card connector (J83). Table 1-6 shows the connections of the SD card interface to the FPGA (U1) on the KCU105 board.

Table 1-6: SDIO Connections to FPGA U1

| FPGA (U1) Pin | Schematic Net Name | I/O Standard | SD MUX/Level-Shifter (U107) | | | | Schematic Net Name | SDIO Connector (J83) | | |
|---------------|--------------------|--------------|------------------------------|----------|-------|----------|--------------------|----------------------|----------|--|
| | | | Pin # | Pin Name | Pin # | Pin Name | | Pin # | Pin Name | |
| AD9 | SDIO_CMD_FPGA | LVC MOS18 | 13 | 2CMD | 2 | CMD | SDIO_CMD_HDR | 3 | CMD | |
| AL10 | SDIO_CLK_FPGA | LVC MOS18 | 11 | 2CLK | 5 | CLK | SDIO_CLK_HDR | 5 | CLK | |
| AH9 | SDIO_DATA2_FPGA | LVC MOS18 | 15 | 2DAT_2 | 24 | DAT_2 | SDIO_DATA2_HDR | 1 | DAT2 | |
| AN9 | SDIO_DATA1_FPGA | LVC MOS18 | 9 | 2DAT_1 | 7 | DAT_1 | SDIO_DATA1_HDR | 8 | DAT1 | |
| AP9 | SDIO_DATA0_FPGA | LVC MOS18 | 10 | 2DAT_0 | 6 | DAT_0 | SDIO_DATA0_HDR | 7 | DAT0 | |
| AH8 | SDIO_DATA3_FPGA | LVC MOS18 | 14 | 2DAT_3 | 1 | DAT_3 | SDIO_DATA3_HDR | 2 | CD_DAT3 | |
| | | | DUAL SPDT CMOS SWITCH (U110) | | | | | | | |
| | | | Pin # | Pin Name | Pin # | Pin Name | | | | |
| AM10 | SDIO_CD_FPGA | LVC MOS18 | 4 | 2S1 | 6 | D2 | SDIO_CD_HDR | 13 | DETECT | |

Figure 1-7 shows the connections of the SD card interface on the KCU105 board.



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Figure 1-7: SD Connector Circuit Topology

For more details about the multiplexer devices, see the Fairchild FSSD07 data sheet at the Fairchild Semiconductor website [Ref 6] and the STMicroelectronics STG3220 data sheet at the STMicroelectronics website [Ref 7]. For more information on Secure Digital nonvolatile memory card technology, see the SanDisk Corporation website [Ref 8] and the SD Association website [Ref 9].

USB JTAG Interface

[Figure 1-2, callout 5]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U115) where a host computer accesses the KCU105 board JTAG chain through a type-A (host side) to micro-B (KCU105 board side J87) USB cable.

A 2-mm JTAG header (J3) is also provided in parallel for access by Xilinx download cables such as the platform cable USB II and the parallel cable IV. The JTAG chain of the KCU105 board is illustrated in Figure 1-8. JTAG configuration is allowed at any time regardless of FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin M2 (which is wired to SW15 pin 6, position 6).



IMPORTANT: The KCU105 board JTAG chain implementation supports up to 15 MHz TCK operation. When using the Vivado Design Suite Hardware Manager to configure the KCU105 board, 15 MHz or lower must be used for the TCK frequency setting. If the JTAG TCK is set to >15 MHz, the Vivado tools display an unknown device instead of detecting the UltraScale Kintex KU040 device.

For more details about the Digilent USB JTAG Module, see the Digilent website [Ref 10].

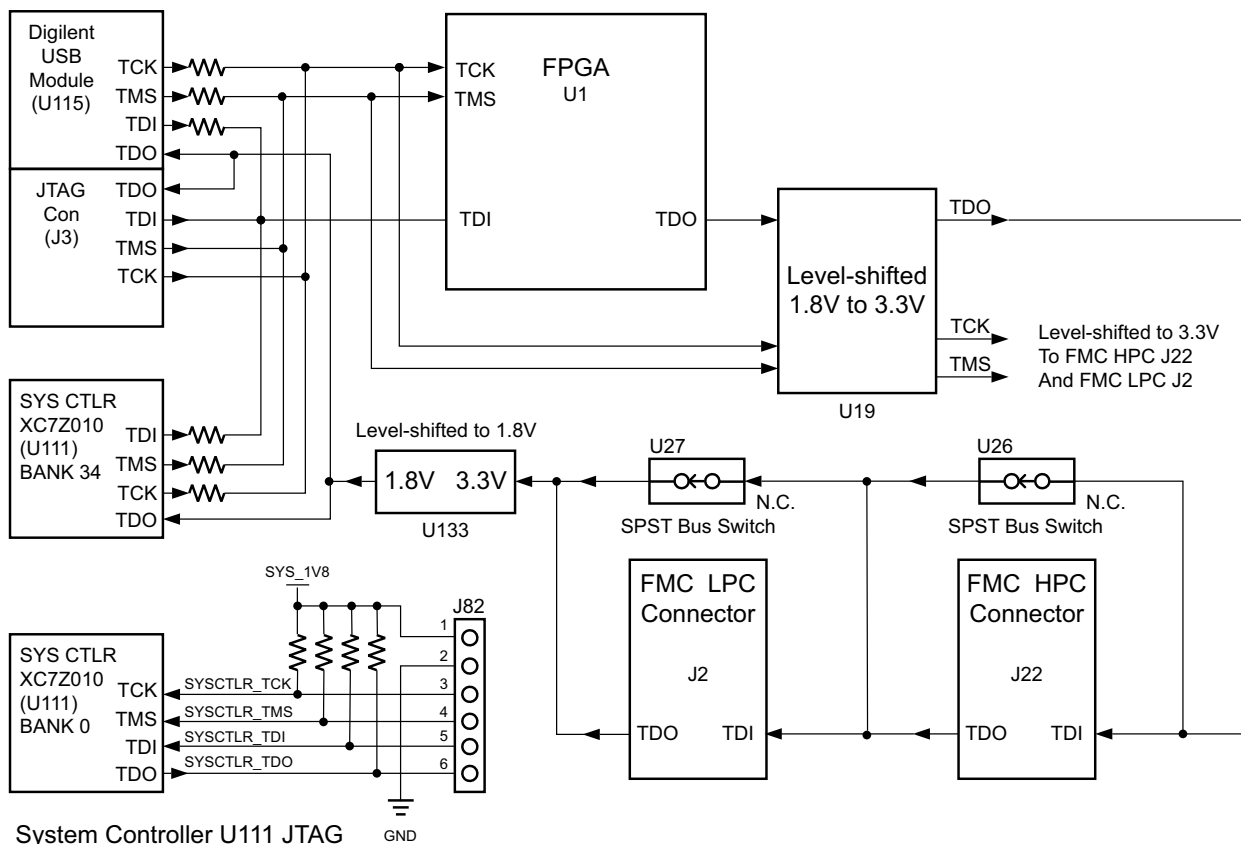


Figure 1-8: JTAG Chain Block Diagram

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IMPORTANT: *The Digilent USB module, Xilinx platform USB cable interface header (J3), and the system controller (U111) bank 34 JTAG interface cannot be operated simultaneously. Make sure that only one JTAG configuration interface is selected.*

FMC Connector JTAG Bypass

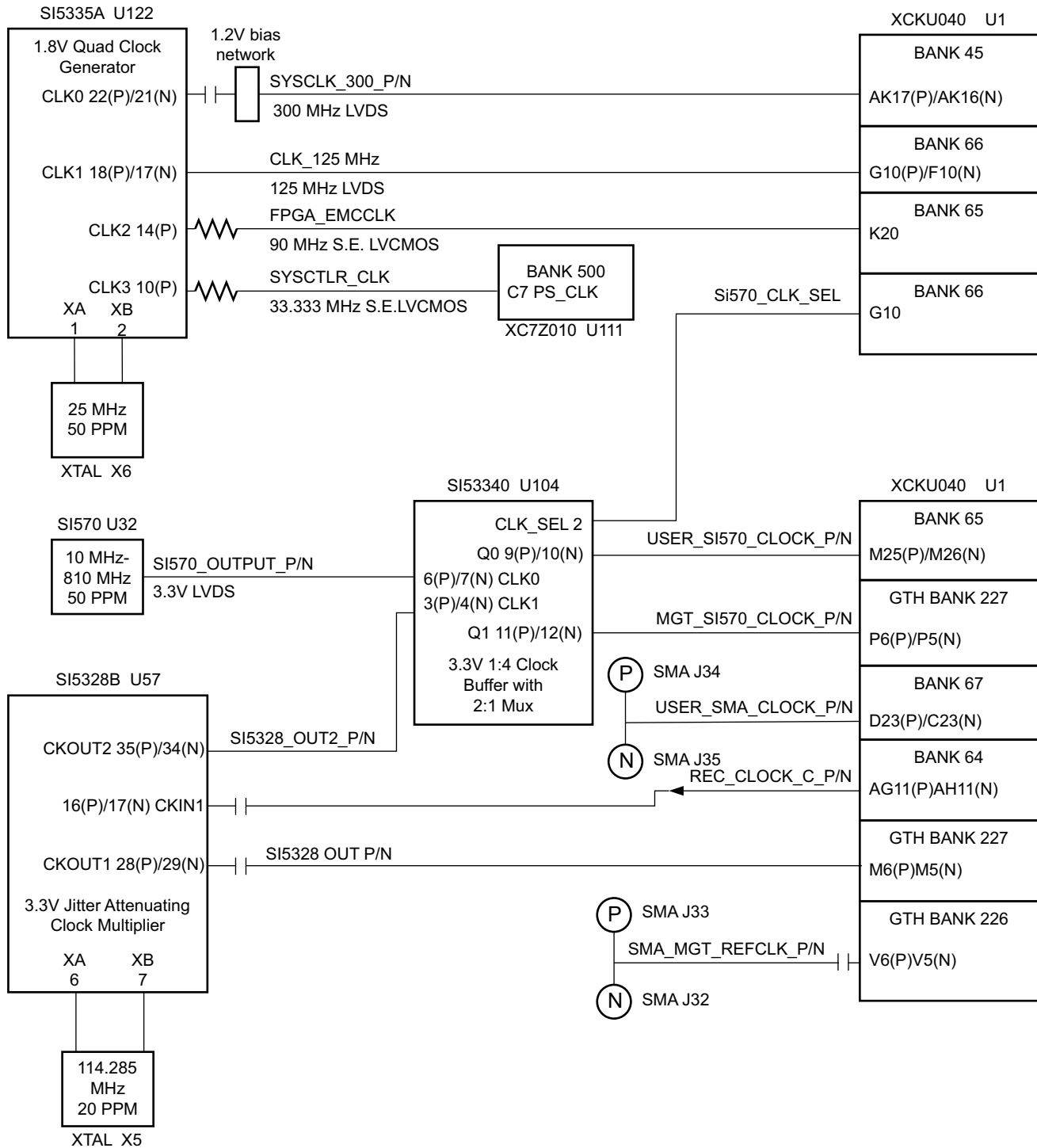
When an FMC mezzanine card is attached to the KCU105 board, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U26 (HPC) and U27 (LPC). The SPST switches are in a normally closed state and transition to an open state when an FMC mezzanine card is attached. Switch U26 adds an attached HPC FMC mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC_PRSENT_M2C_B signal (active-Low). Switch U27 adds an attached LPC FMC mezzanine card to the FPGAs JTAG chain as determined by the FMC_LPC_PRSENT_M2C_B signal (active-Low). The attached FMC card must implement a TDI-to-TDO connection via a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.

The JTAG connectivity on the KCU105 board allows a host computer to download bitstreams to the FPGA using the Vivado design tools. In addition, the JTAG connector allows debug tools such as the Vivado serial I/O analyzer or a software debugger to access the FPGA. The Vivado design tools can also be used to program the dual Quad-SPI Flash memory.

Clock Generation

[Figure 1-2, callout 6]

The KCU105 evaluation board provides nine clock sources for the XCKU040 device. The KCU105 board clocking system is illustrated in [Figure 1-9](#).



X18373-113016

Figure 1-9: KCU105 Board Clocking Block Diagram

Table 1-7 lists the source devices for each clock.

Table 1-7: KCU105 Board Clock Sources

| Clock Name | Clock Ref. Des. | Description |
|-----------------------------------|-----------------|--|
| System Clock 300 MHz | U122 | <ul style="list-style-type: none"> • Silicon Labs Si5335A 1.8V LVDS Any Frequency Quad Clock Generator CLK0. • See Clock Generation (SYSCLK_300_P and SYSCLK_300_N). |
| System Clock 125 MHz | U122 | <ul style="list-style-type: none"> • Silicon Labs Si5335A 1.8V LVDS Any Frequency Quad Clock Generator CLK1. • See Clock Generation (CLK_125MHZ). |
| EMC Clock 90 MHz | U122 | <ul style="list-style-type: none"> • Silicon Labs Si5335A 1.8V LVCMOS Single-Ended Any Frequency Quad Clock Generator CLK2. • See Clock Generation (FPGA_EMCCLK). |
| System Ctlr. Clock 33.333 MHz | U122 | <ul style="list-style-type: none"> • Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency quad clock generator CLK3. • See Clock Generation (SYSCTLR_CLK). |
| User Clock 10 MHz-810 MHz | U32 | <ul style="list-style-type: none"> • Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. Available from the output Q0 of Silicon Labs Si53340 clock buffer. • See Programmable User Clock Source (USER_SI570_CLOCK_P and USER_SI570_CLOCK_N). |
| GTH SMA REF Clock | J33(P), J32(N) | <ul style="list-style-type: none"> • User clock input SMAs. • See GTH TX and RX SMA Differential Pairs (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N). |
| User SMA Clock | J34(P), J35(N) | <ul style="list-style-type: none"> • User clock input SMAs. • See User SMA Clock Input (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N). |
| Jitter Attenuated Clock CKOUT1 | U57 | <ul style="list-style-type: none"> • Silicon Labs Si5328B LVDS precision clock multiplier/jitter attenuator. • See Jitter Attenuated Clock (SI5328_OUT_P and SI5328_OUT_N). |
| Jitter Attenuated Clock CKOUT2 | U57 | <ul style="list-style-type: none"> • Silicon Labs Si5328B LVDS precision clock multiplier/jitter attenuator. • See Jitter Attenuated Clock (SI5328_OUT2_P and SI5328_OUT2_N). |

Table 1-8 lists the KCU105 board clock sources to the XCKU040 device U1 connections.

Table 1-8: KCU105 Board Clock Sources to XCKU040 Device U1 Connections

| Clock Source Ref. Des. and Pin | Schematic Net Name | I/O Standard | XCKU040 Device (U1) Pin |
|--------------------------------|--------------------|-------------------|-------------------------|
| U122.22 | SYSCLK_300_P | LVDS | AK17 |
| U122.21 | SYSCLK_300_N | LVDS | AK16 |
| U122.18 | CLK_125MHZ_P | LVDS | G10 |
| U122.17 | CLK_125MHZ_N | LVDS | F10 |
| U122.14 | FPGA_EMCCCLK | LVC MOS18 | K20 |
| U122.10 | SYSCTLR_CLK | LVC MOS18 | C7 |
| U104.9 | USER_SI570_CLOCK_P | LVDS_25 | M25 |
| U104.10 | USER_SI570_CLOCK_N | LVDS_25 | M26 |
| U104.11 | MGT_SI570_CLOCK_P | NA ⁽¹⁾ | P6 |
| U104.12 | MGT_SI570_CLOCK_N | NA ⁽¹⁾ | P5 |
| J33.1 | SMA_MGT_REFCLK_P | NA ⁽¹⁾ | V6 |
| J32.1 | SMA_MGT_REFCLK_N | NA ⁽¹⁾ | V5 |
| J34.1 | USER_SMA_CLOCK_P | LVDS | D23 |
| J35.1 | USER_SMA_CLOCK_N | LVDS | C23 |
| U57.28 | SI5328_OUT_P | NA ⁽¹⁾ | M6 |
| U57.29 | SI5328_OUT_N | NA ⁽¹⁾ | M5 |

Notes:

1. Capacitively coupled, serial transceiver connections I/O standard not applicable.

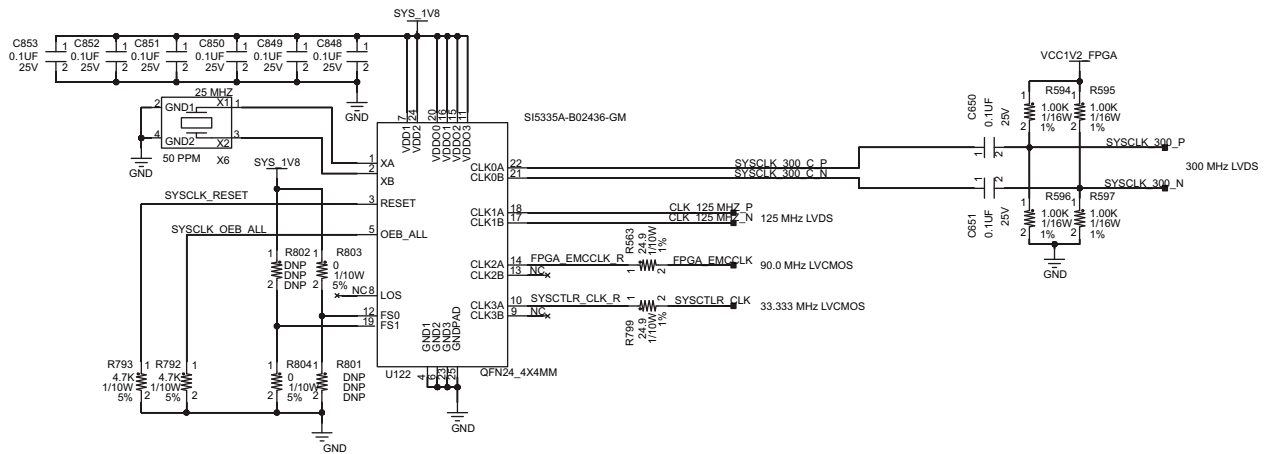
System Clock Source

[Figure 1-2, callout 6]

The system clock source is a Silicon Labs Si5335A quad clock generator/buffer at U122. The system clock (SYSCLK) is a LVDS 300 MHz clock sourced from the CLK0A output pair of U122. SYSCLK is wired to a clock capable (GC) input on programmable logic bank 45. The signal pair is named SYSCLK_300_P and SYSCLK_300_N connected to the XCKU040 device U1 (bank 45 pins AK17 and AK16, respectively).

- Clock Generator: Silicon Labs Si5335A-B02436-GM (CLK0A 300 MHz)
- Low phase jitter of 0.7 pS RMS
- LVDS Differential Output

The system clock circuit is shown in Figure 1-10.



X18374-020519

Figure 1-10: KCU105 Board System Clock

Three additional clocks are sourced from the U122 quad clock generator:

- 125 MHz LVDS signal pair CLK_125MHZ_P and CLK_125MHZ_N, connected to the XCKU040 device U1 bank 66 pins G10 and F10, respectively.
- 90.0 MHz single-ended 1.8V LVC MOS, series resistor coupled FPGA_EMCCLK, connected to the XCKU040 device U1 bank 65 dedicated EMCCLK input pin K20.
- 33.3333 MHz single-ended 1.8V LVC MOS, series resistor coupled SYSCTLR_CLK, connected to system controller XC7Z010 Zynq-7000 SoC U111 bank 500 dedicated PS_CLK input pin C7.

Programmable User Clock Source

[Figure 1-2, callout 7]

The KCU105 evaluation board has a Si570 programmable low-jitter 3.3V LVDS differential oscillator (U32) connected to the CLK0 P/N inputs (pin 6 (P) and 7 (N)) of clock buffer Si53340 U104, a 3.3V 1:4 LOW-JITTER LVDS CLOCK BUFFER WITH 2:1 INPUT MUX.

U104 CLK1 P/N inputs (pin 3 (P) and 4 (N)) are driven from the Si5328B clock multiplier/jitter attenuator U57 CLKOUT2 pins 35 (P) and 34 (N). The Si5328B is discussed in [Jitter Attenuated Clock](#).

The 3.3V Si53340 U104 has four LVDS output clock pairs, two (Q2, Q3) unused. U104 output Q0 drives clock pair USER_SI570_CLOCK_P and USER_SI570_CLOCK_N, connected to the XCKU040 device U1 bank 65 GC pins M25 and M26, respectively.

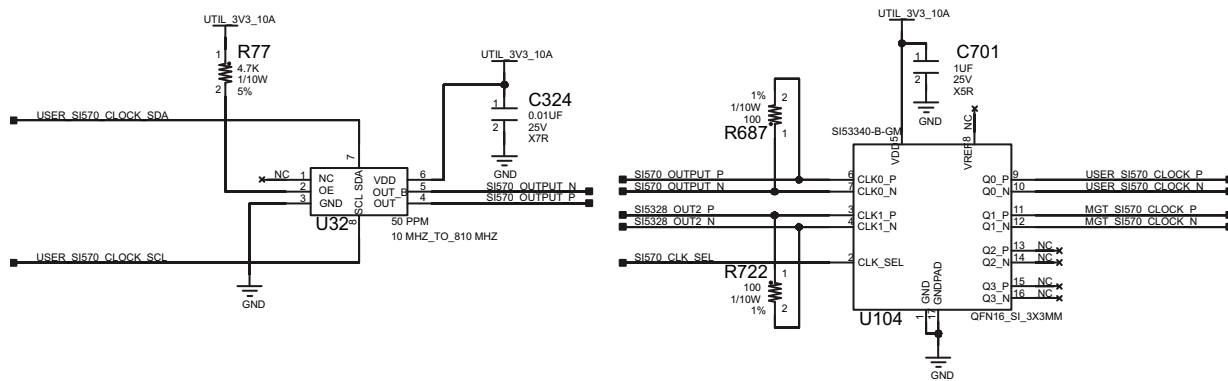
U104 output Q1 drives clock pair MGT_SI570_CLOCK_P and MGT_SI570_CLOCK_N, which are connected to the XCKU040 device U1 GTH BANK 227 MGTREFCLK0P/N pins P6 and P5, respectively.

The U104 2:1 pin 2 MUX select net SI570_CLK_SEL is connected to the XCKU040 device U1 bank 66 pin F12 via 3.3V-to-1.8V level-shifter U43. USER_SI570_CLOCK_P/N and MGT_SI570_CLOCK_P/N are sourced by U32 SI570 when SI570_CLK_SEL = 0 and by U57 SI5328 CKOUT2 output when SI570_CLK_SEL = 1.

On power-up, the Si570 user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the KCU105 evaluation board resets the user clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

The system clock circuit is shown in [Figure 1-11](#).



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Figure 1-11: KCU105 Board User Clock

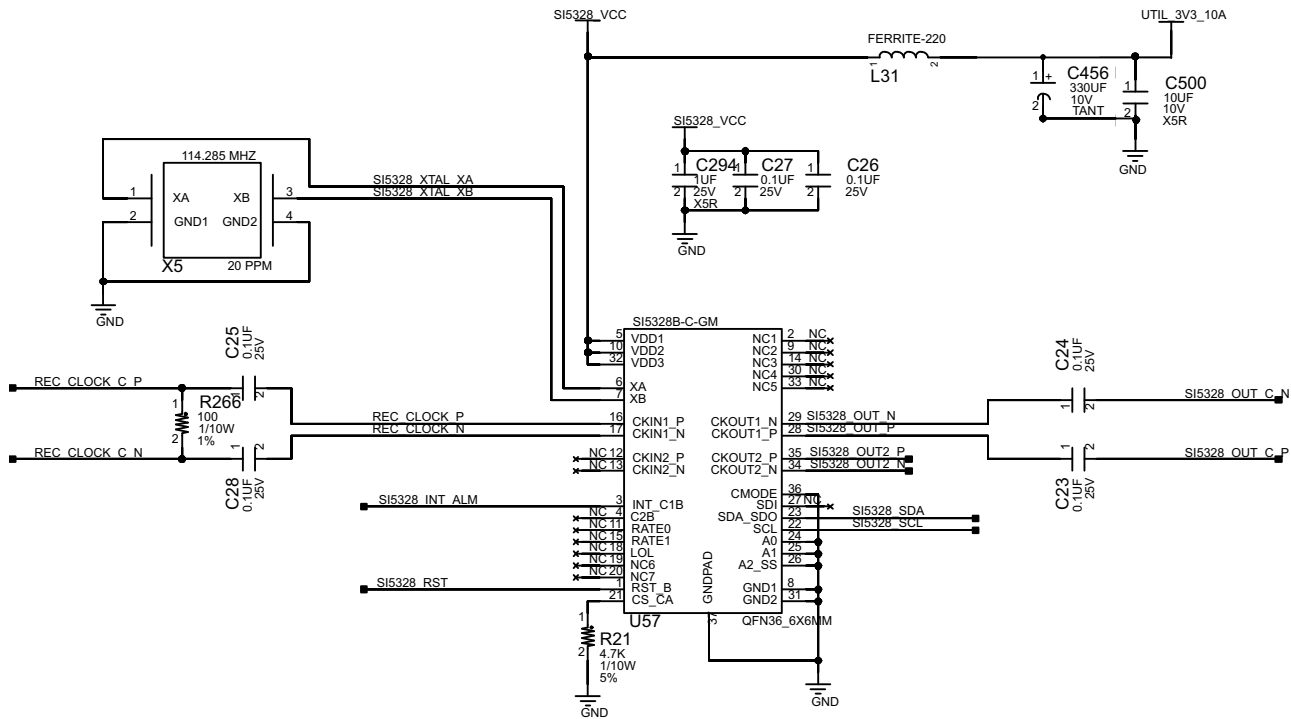
Jitter Attenuated Clock

[[Figure 1-2](#), callout 8]

The KCU105 board includes a Silicon Labs Si5328B jitter attenuator U57 (8 kHz - 808 MHz) on the back side of the board. The GTH transceiver can output the RX recovered clock to a differential I/O pair on I/O bank 64 (REC_CLOCK_C_P, pin AG11 and REC_CLOCK_C_N, pin AH11) for jitter attenuation. The jitter attenuated clock (Si5328_OUT_C_P (U57 pin 28), Si5328_OUT_C_N (U57 pin 29)) is then routed as a reference clock to GTH Quad 227 inputs MGTREFCLK0P (U1 pin P6) and MGTREFCLK0N (U1 pin P5).

The primary purpose of this clock is to support synchronous protocols such as CPRI or OBSAI that perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTH transceiver. The system controller configures the Si5328B in free-run mode (see [KCU105 Board Zynq-7000 SoC XC7Z010 System Controller](#)). Enabling the jitter attenuation feature requires additional user programming from the FPGA through the I2C bus.

The jitter attenuated clock circuit is shown in Figure 1-12.



X18376-113016

Figure 1-12: KCU105 Board Jitter Attenuated Clock



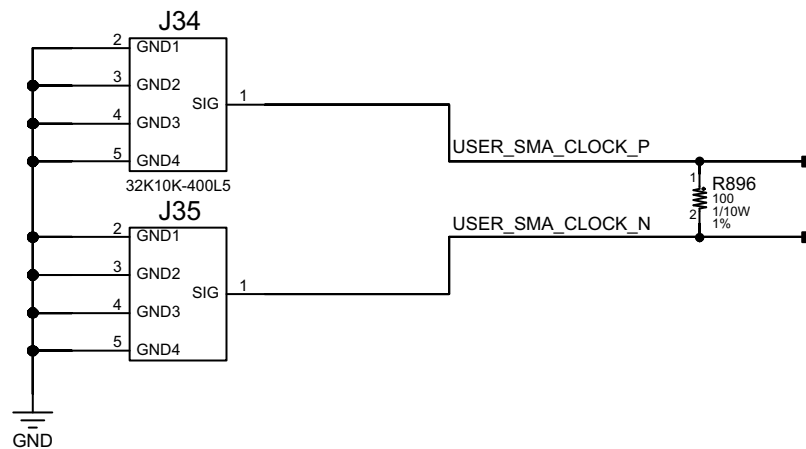
IMPORTANT: The Silicon Labs Si5328 U57 pin 1 reset net SI5328_RST must be driven High to enable the device. U57 pin 1 net SI5328_RST is level-shifted to 1.8V by U47 and is connected to FPGA U1 bank 65 pin K23.

An active-Low input at U57 pin 1 RST_B performs an external hardware reset of this device. This resets all internal logic to a known state and forces the device registers to their default value. The clock outputs are disabled during reset. The part must be programmed after a reset or power on to get a clock output. The reset pin 1 has a weak internal pull-up. For more details on the Silicon Labs Si5335A, Si570, Si53340, and Si5328B devices, see the Silicon Labs website [Ref 11]. For more information on UltraScale FPGA clocking, see *UltraScale Architecture Clocking Resources User Guide* (UG572) [Ref 12].

User SMA Clock Input

[Figure 1-2, callout 9]

The KCU105 board provides a pair of SMAs for differential user clock input into FPGA U1 bank 67 (see Figure 1-13). The P-side SMA J34 signal USER_SMA_CLOCK_P is connected to U1 GC pin D23, with the N-side SMA J35 signal USER_SMA_CLOCK_N connected to U1 GC pin C23. Bank 67 VCCO is nominally 1.8V VADJ_1V8_FPGA. The USER_SMA_CLOCK input voltage swing should not exceed VADJ. Any signal connected to the USER_SMA_CLOCK connector inputs must be equal to or less than the VCCO for bank 67. Valid values for the VADJ rail VADJ_1V8_FPGA are 1.5V and 1.8V. This value must be confirmed prior to applying signals to the USER_SMA_CLOCK connectors.



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Figure 1-13: User SMA Clock

GTH SMA Clock Input

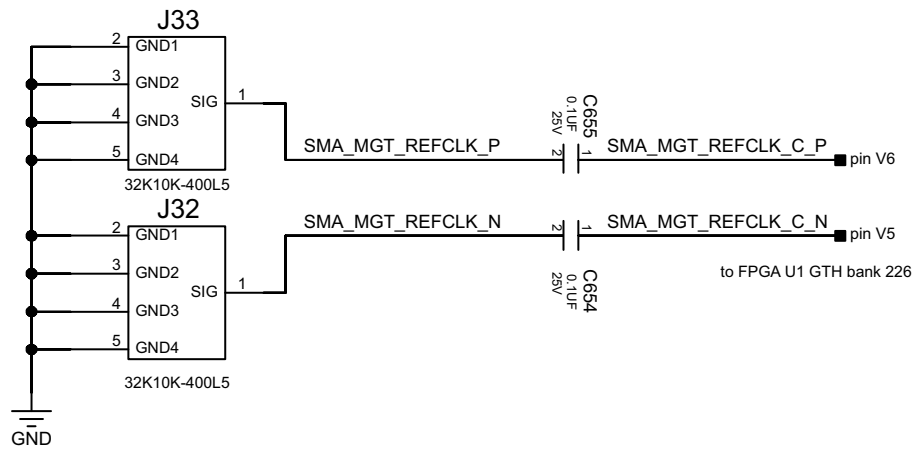
[Figure 1-2, callout 10]

The KCU105 board includes a pair of SMA connectors for a GTH clock wired to GTH Quad bank 226. This differential clock has signal names SMA_MGT_REFCLK_P and SMA_REFCLK_N, which are capacitively connected to FPGA U1 GTH bank 226 pins V6 and V5, respectively.

- External user-provided GTH reference clock on SMA input connectors
- Differential Input

The GTH SMA REFCLK signal data paths are routed with a differential characteristic impedance of 100Ω (±10%).

Figure 1-14 shows this AC-coupled clock circuit.



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Figure 1-14: User GTH REF Clock

GTH TX and RX SMA Differential Pairs

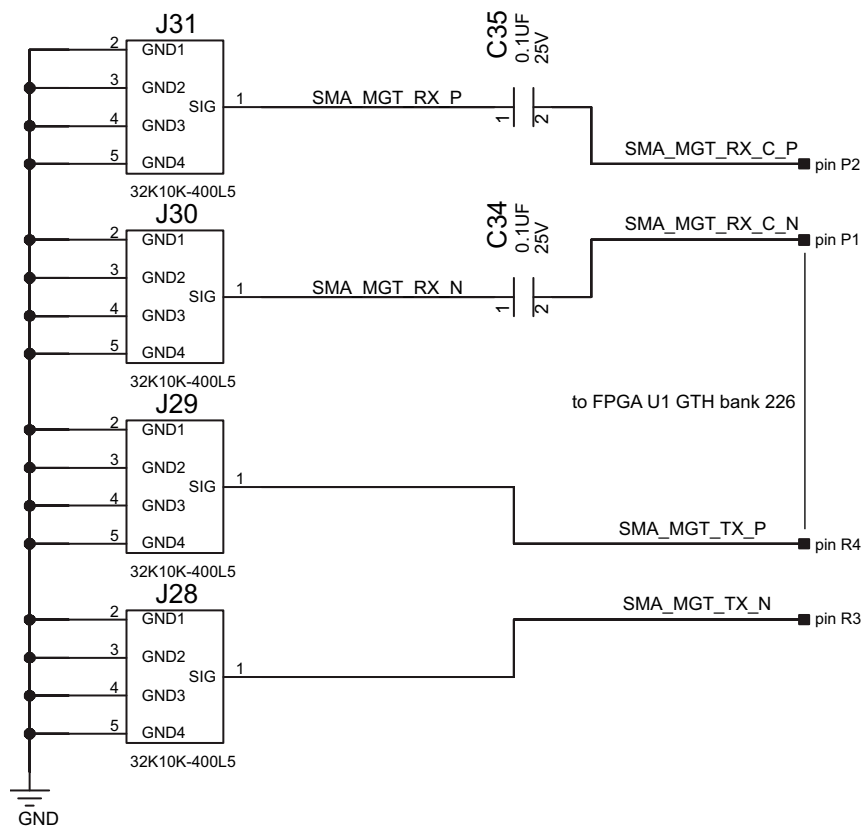
[Figure 1-2, callout 12]

The KCU105 board includes two pairs (TX and RX) of SMA connectors wired to GTH Quad bank 226. These differential SMA pairs have signal names SMA_MGT_TX_P, SMA_MGT_TX_N and SMA_MGT_RX_P, SMA_MGT_RX_N (RX are capacitively coupled) and are connected to FPGA U1 GTH bank 226 pins R4, R3 and P2, P1, respectively.

- External user-provided GTH TX and RX on SMA connectors
- Differential SMA pairs

The GTH TX and RX SMA transmit and receive signal data paths are routed with a differential characteristic impedance of 100Ω (±10%) with an insertion loss of <4 dB up to 8 GHz.

Figure 1-15 shows the TX SMA pair and the AC-coupled RX SMA pair.



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Figure 1-15: User GTH TX and RX SMA Pairs

GTH Transceivers

[Figure 1-2, callout 13]

The KCU105 board provides access to 20 GTH transceivers:

- Eight of the GTH transceivers are wired to the PCI Express x8 edge connector (P1)
- Eight of the GTH transceivers are wired to the FMC HPC connector (J22)
- One GTH transceiver is wired to the FMC LPC connector (J2)
- One GTH transceiver is wired to SMA connectors (RX: J31, J30 TX: J29, J28)
- Two GTH transceivers are wired to SFP/SFP+ Module connectors (P4, P5)

The GTH transceivers in the XCKU040 device are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTH Quad of interest. There are five GTH Quads on the KCU105 board with connectivity as shown here:

Quad 224:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Contains 4 GTH transceivers allocated to PCIe lanes 4-7

Quad 225:

- MGTREFCLK0 - PCIE_CLK_Q0_P/N PCIe edge connector clock
- MGTREFCLK1 - not connected
- Contains 4 GTH transceivers allocated to PCIe lanes 0-3

Quad 226:

- MGTREFCLK0 - SMA_MGT_REFCLK_C_P/N SMA GTH clock input
- MGTREFCLK1 - FMC_LPC_GBTCLK0_M2C_C_P/N
- Contains one GTH transceiver allocated to FMC_LPC_DP0_C2M_P/N
- Contains two GTH transceivers allocated to SFP_TX_P/N and RX_P/N SFP/SFP+ connectors SFP0 and SFP1
- Contains one GTH transceiver allocated to SMA_MGT_TX_P/N and SMA_MGT_RX_P/N SMA connector pairs

Quad 227:

- MGTREFCLK0 - MGT_SI570_CLOCK_C_P/N clock
- MGTREFCLK1 - SI5328_OUT_C_P/N jitter attenuator clock
- Contains four GTH transceivers allocated to FMC_HPC_DP[7:4]_C2M_P/N

Quad 228:

- MGTREFCLK0 - FMC_HPC_GBTCLK0_M2C_C_P/N clock
- MGTREFCLK1 - FMC_HPC_GBTCLK1_M2C_C_P/N clock
- Contains four GTH transceivers allocated to FMC_HPC_DP[3:0]_C2M/M2C_P/N

Table 1-9 lists the GTH banks 224 and 225 interface connections between FPGA U1 and 8-lane PCIe connector P1.

Table 1-9: KCU105 Board FPGA U1 GTH Banks 224 and 225 Connections to PCIe Connector P1

| Transceiver Bank | FPGA (U1) Pin | FPGA (U1) Pin Name | Schematic Net Name | Connected Pin | Connected Pin Name | Connected Device |
|------------------|-----------------|--------------------|--------------------|---------------|--------------------|------------------------|
| GTH Bank 224 | AN4 | MGTHTXP0_224 | PCIE_TX7_P | A47 | PERp7 | PCIe Edge Connector P1 |
| | AN3 | MGTHTXN0_224 | PCIE_TX7_N | A48 | PERn7 | |
| | AP2 | MGTHRXP0_224 | PCIE_RX7_P | B45 | PETp7 | |
| | AP1 | MGTHRXN0_224 | PCIE_RX7_N | B46 | PETn7 | |
| | AM6 | MGTHTXP1_224 | PCIE_TX6_P | A43 | PERp6 | |
| | AM5 | MGTHTXN1_224 | PCIE_TX6_N | A44 | PERn6 | |
| | AM2 | MGTHRXP1_224 | PCIE_RX6_P | B41 | PETp6 | |
| | AM1 | MGTHRXN1_224 | PCIE_RX6_N | B42 | PETn6 | |
| | AL4 | MGTHTXP2_224 | PCIE_TX5_P | A39 | PERp5 | |
| | AL3 | MGTHTXN2_224 | PCIE_TX5_N | A40 | PERn5 | |
| | AK2 | MGTHRXP2_224 | PCIE_RX5_P | B37 | PETp5 | |
| | AK1 | MGTHRXN2_224 | PCIE_RX5_N | B38 | PETn5 | |
| | AK6 | MGTHTXP3_224 | PCIE_TX4_P | A35 | PERp4 | |
| | AK5 | MGTHTXN3_224 | PCIE_TX4_N | A36 | PERn4 | |
| | AJ4 | MGTHRXP3_224 | PCIE_RX4_P | B33 | PETp4 | |
| | AJ3 | MGTHRXN3_224 | PCIE_RX4_N | B34 | PETn4 | |
| | AF6 | MGTREFCLK0P_224 | NC | NA | NA | |
| | AF5 | MGTREFCLK0N_224 | NC | NA | NA | |
| AD6 | MGTREFCLK1P_224 | NC | NA | NA | | |
| AD5 | MGTREFCLK1N_224 | NC | NA | NA | | |

Table 1-9: KCU105 Board FPGA U1 GTH Banks 224 and 225 Connections to PCIe Connector P1 (Cont'd)

| Transceiver Bank | FPGA (U1) Pin | FPGA (U1) Pin Name | Schematic Net Name | Connected Pin | Connected Pin Name | Connected Device |
|------------------|-----------------|--------------------|--------------------|---------------|--------------------|------------------------|
| GTH Bank 225 | AH6 | MGTHTXP0_225 | PCIE_TX3_P | A29 | PERp3 | PCIe Edge Connector P1 |
| | AH5 | MGTHTXN0_225 | PCIE_TX3_N | A30 | PERn3 | |
| | AH2 | MGTHRXP0_225 | PCIE_RX3_P | B27 | PETp3 | |
| | AH1 | MGTHRXN0_225 | PCIE_RX3_N | B28 | PETn3 | |
| | AG4 | MGTHTXP1_225 | PCIE_TX2_P | A25 | PERp2 | |
| | AG3 | MGTHTXN1_225 | PCIE_TX2_N | A26 | PERn2 | |
| | AF2 | MGTHRXP1_225 | PCIE_RX2_P | B23 | PETp2 | |
| | AF1 | MGTHRXN1_225 | PCIE_RX2_N | B24 | PETn2 | |
| | AE4 | MGTHTXP2_225 | PCIE_TX1_P | A21 | PERp1 | |
| | AE3 | MGTHTXN2_225 | PCIE_TX1_N | A22 | PERn1 | |
| | AD2 | MGTHRXP2_225 | PCIE_RX1_P | B19 | PETp1 | |
| | AD1 | MGTHRXN2_225 | PCIE_RX1_N | B20 | PETn1 | |
| | AC4 | MGTHTXP3_225 | PCIE_TX0_P | A16 | PERp0 | |
| | AC3 | MGTHTXN3_225 | PCIE_TX0_N | A17 | PERn0 | |
| | AB2 | MGTHRXP3_225 | PCIE_RX0_P | B14 | PETp0 | |
| | AB1 | MGTHRXN3_225 | PCIE_RX0_N | B15 | PETn0 | |
| | AB6 | MGTREFCLK0P_225 | PCIE_CLK_QO_P | A13 | REFCLK+ | |
| | AB5 | MGTREFCLK0N_225 | PCIE_CLK_QO_N | A14 | REFCLK- | |
| | Y6 | MGTREFCLK1P_225 | NC | NA | NA | |
| Y5 | MGTREFCLK1N_225 | NC | NA | NA | | |

Table 1-10 lists the GTH bank 226 interface connections between FPGA U1, FMC LPC connector J2, SFP0 connector P5, SFP1 connector P4 and MGT TX SMA connectors J29/J28, MGT RX SMA connectors J31/J30 and MGT REFCLK SMA connectors J33/J32.

Table 1-10: KCU105 Board FPGA U1 GTH Bank 226 Connections

| Transceiver Bank | FPGA (U1) Pin | FPGA (U1) Pin Name | Schematic Net Name | Connected Pin | Connected Pin Name | Connected Device |
|------------------|---------------|--------------------|-------------------------|---------------|--------------------|------------------|
| GTH Bank 226 | AA4 | MGHTXP0_226 | FMC_LPC_DP0_C2M_P | C2 | DP0_C2M_P | FMC LPC J2 |
| | AA3 | MGHTXN0_226 | FMC_LPC_DP0_C2M_N | C3 | DP0_C2M_N | |
| | Y2 | MGTHRXP0_226 | FMC_LPC_DP0_M2C_P | C6 | DP0_M2C_P | |
| | Y1 | MGTHRXN0_226 | FMC_LPC_DP0_M2C_N | C7 | DP0_M2C_N | |
| | W4 | MGHTXP1_226 | SFP1_TX_P | 18 | TD_P | SFP1 P4 |
| | W3 | MGHTXN1_226 | SFP1_TX_N | 19 | TD_N | |
| | V2 | MGTHRXP1_226 | SFP1_RX_P | 13 | RD_P | |
| | V1 | MGTHRXN1_226 | SFP1_RX_N | 12 | RD_N | |
| | U4 | MGHTXP2_226 | SFP0_TX_P | 18 | TD_P | SFP0 P5 |
| | U3 | MGHTXN2_226 | SFP0_TX_N | 19 | TD_N | |
| | T2 | MGTHRXP2_226 | SFP0_RX_P | 13 | RD_P | |
| | T1 | MGTHRXN2_226 | SFP0_RX_N | 12 | RD_N | |
| | R4 | MGHTXP3_226 | SMA_MGT_TX_P | 1 | SIG | SMA J29 |
| | R3 | MGHTXN3_226 | SMA_MGT_TX_N | 1 | SIG | SMA J28 |
| | P2 | MGTHRXP3_226 | SMA_MGT_RX_C_P | 1 | SIG | SMA J31 |
| | P1 | MGTHRXN3_226 | SMA_MGT_RX_C_N | 1 | SIG | SMA J30 |
| | V6 | MGTREFCLK0P_226 | SMA_MGT_REFCLK_C_P | 1 | SIG | SMA J33 |
| | V5 | MGTREFCLK0N_226 | SMA_MGT_REFCLK_C_N | 1 | SIG | SMA J32 |
| | T6 | MGTREFCLK1P_226 | FMC_LPC_GBTCLK0_M2C_C_P | D4 | GBTCLK0_M2C_P | FMC LPC J2 |
| | T5 | MGTREFCLK1N_226 | FMC_LPC_GBTCLK0_M2C_C_N | D5 | GBTCLK0_M2C_N | |

Table 1-11 lists the GTH banks 227 and 228 interface connections between FPGA U1 and the FMC HPC J22 connector.

Table 1-11: KCU105 Board FPGA U1 GTH Bank 227 and 228 Connections

| Transceiver Bank | FPGA (U1) Pin | FPGA (U1) Pin Name | Schematic Net Name | Connected Pin | Connected Pin Name | Connected Device |
|------------------|-----------------|--------------------|---------------------|---------------|--------------------|------------------|
| GTH Bank 227 | N4 | MGTHTXP0_227 | FMC_HPC_DP4_C2M_P | A34 | DP4_C2M_P | FMC HPC J22 |
| | N3 | MGTHTXN0_227 | FMC_HPC_DP4_C2M_N | A35 | DP4_C2M_N | |
| | M2 | MGTHRXP0_227 | FMC_HPC_DP4_M2C_P | A14 | DP4_M2C_P | |
| | M1 | MGTHRXN0_227 | FMC_HPC_DP4_M2C_N | A15 | DP4_M2C_N | |
| | L4 | MGTHTXP1_227 | FMC_HPC_DP6_C2M_P | B36 | DP6_C2M_P | |
| | L3 | MGTHTXN1_227 | FMC_HPC_DP6_C2M_N | B37 | DP6_C2M_N | |
| | K2 | MGTHRXP1_227 | FMC_HPC_DP6_M2C_P | B16 | DP6_M2C_P | |
| | K1 | MGTHRXN1_227 | FMC_HPC_DP6_M2C_N | B17 | DP6_M2C_N | |
| | J4 | MGTHTXP2_227 | FMC_HPC_DP5_C2M_P | A38 | DP5_C2M_P | |
| | J3 | MGTHTXN2_227 | FMC_HPC_DP5_C2M_N | A39 | DP5_C2M_N | |
| | H2 | MGTHRXP2_227 | FMC_HPC_DP5_M2C_P | A18 | DP5_M2C_P | |
| | H1 | MGTHRXN2_227 | FMC_HPC_DP5_M2C_N | A19 | DP5_M2C_N | |
| | G4 | MGTHTXP3_227 | FMC_HPC_DP7_C2M_P | B32 | DP7_C2M_P | |
| | G3 | MGTHTXN3_227 | FMC_HPC_DP7_C2M_N | B33 | DP7_C2M_N | |
| | F2 | MGTHRXP3_227 | FMC_HPC_DP7_M2C_P | B12 | DP7_M2C_P | |
| | F1 | MGTHRXN3_227 | FMC_HPC_DP7_M2C_N | B13 | DP7_M2C_N | |
| | P6 | MGTREFCLK0P_227 | MGT_SI570_CLOCK_C_P | 11 | Q1_P | Si53340 U104 |
| | P5 | MGTREFCLK0N_227 | MGT_SI570_CLOCK_C_N | 12 | Q1_N | |
| M6 | MGTREFCLK1P_227 | SI5328_OUT_C_P | 28 | CKOUT1_P | Si5328B U57 | |
| M5 | MGTREFCLK1N_227 | SI5328_OUT_C_N | 29 | CKOUT1_N | | |

Table 1-11: KCU105 Board FPGA U1 GTH Bank 227 and 228 Connections (Cont'd)

| Transceiver Bank | FPGA (U1) Pin | FPGA (U1) Pin Name | Schematic Net Name | Connected Pin | Connected Pin Name | Connected Device |
|------------------|-----------------|-------------------------|-------------------------|---------------|--------------------|------------------|
| GTH Bank 228 | F6 | MGTHTXP0_228 | FMC_HPC_DP0_C2M_P | C2 | DP0_C2M_P | FMC HPC J22 |
| | F5 | MGTHTXN0_228 | FMC_HPC_DP0_C2M_N | C3 | DP0_C2M_N | |
| | E4 | MGTHRXP0_228 | FMC_HPC_DP0_M2C_P | C6 | DP0_M2C_P | |
| | E3 | MGTHRXN0_228 | FMC_HPC_DP0_M2C_N | C7 | DP0_M2C_N | |
| | D6 | MGTHTXP1_228 | FMC_HPC_DP1_C2M_P | A22 | DP1_C2M_P | |
| | D5 | MGTHTXN1_228 | FMC_HPC_DP1_C2M_N | A23 | DP1_C2M_N | |
| | D2 | MGTHRXP1_228 | FMC_HPC_DP1_M2C_P | A2 | DP1_M2C_P | |
| | D1 | MGTHRXN1_228 | FMC_HPC_DP1_M2C_N | A3 | DP1_M2C_N | |
| | C4 | MGTHTXP2_228 | FMC_HPC_DP2_C2M_P | A26 | DP2_C2M_P | |
| | C3 | MGTHTXN2_228 | FMC_HPC_DP2_C2M_N | A27 | DP2_C2M_N | |
| | B2 | MGTHRXP2_228 | FMC_HPC_DP2_M2C_P | A6 | DP2_M2C_P | |
| | B1 | MGTHRXN2_228 | FMC_HPC_DP2_M2C_N | A7 | DP2_M2C_N | |
| | B6 | MGTHTXP3_228 | FMC_HPC_DP3_C2M_P | A30 | DP3_C2M_P | |
| | B5 | MGTHTXN3_228 | FMC_HPC_DP3_C2M_N | A31 | DP3_C2M_N | |
| | A4 | MGTHRXP3_228 | FMC_HPC_DP3_M2C_P | A10 | DP3_M2C_P | |
| | A3 | MGTHRXN3_228 | FMC_HPC_DP3_M2C_N | A11 | DP3_M2C_N | |
| | K6 | MGTREFCLK0P_228 | FMC_HPC_GBTCLK0_M2C_C_P | D4 | GBTCLK0_M2C_P | |
| | K5 | MGTREFCLK0N_228 | FMC_HPC_GBTCLK0_M2C_C_N | D5 | GBTCLK0_M2C_N | |
| | H6 | MGTREFCLK1P_228 | FMC_HPC_GBTCLK1_M2C_C_P | B20 | GBTCLK1_M2C_P | |
| H5 | MGTREFCLK1N_228 | FMC_HPC_GBTCLK1_M2C_C_N | B21 | GBTCLK1_M2C_N | | |

For additional information on GTH transceivers, see *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 13] and *UltraScale FPGAs Transceivers Wizard Product Guide for Vivado Design Suite* (PG182) [Ref 14]. For additional information about UltraScale FPGA PCIe functionality, see *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156) [Ref 15]. Additional information about the PCI Express standard is available at the PCI Express website [Ref 16].

PCI Express Endpoint Connectivity

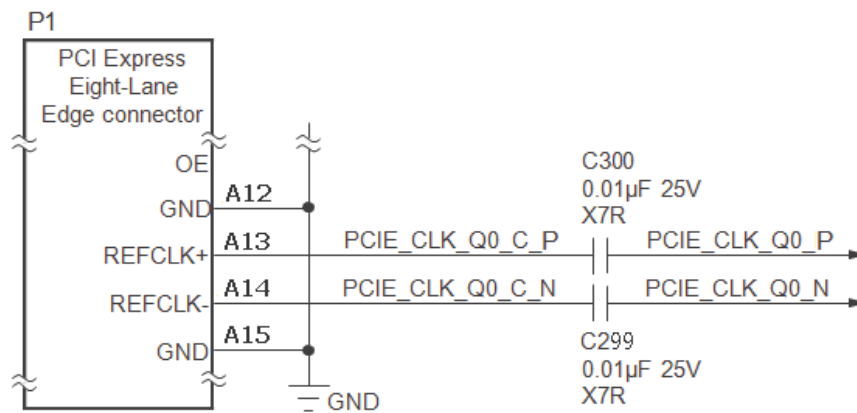
[Figure 1-2, callout 14]

The 8-lane PCI Express edge connector P1 performs data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal datapaths have a characteristic impedance of $85\Omega \pm 10\%$. The PCIe clock is routed as a 100 Ω differential pair.

The PCIe transmit and receive signal data paths are routed with a differential characteristic impedance of $85\Omega (\pm 10\%)$ with an insertion loss of <4 dB up to 8 GHz.

The XCKU040-2FFVA1156E (-2 speed grade) device included with the KCU105 board supports up to Gen3 x8.

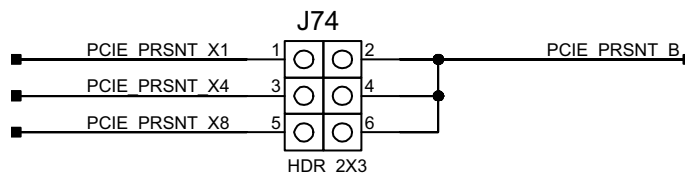
The PCIe reference clock input is from the P1 edge connector. It is AC coupled to FPGA U1 through the MGTREFCLK0 pins of Quad 225. PCIE_CLK_Q0_P is connected to U1 pin AB6, and the _N net is connected to pin AB5. The PCIe Express clock circuit is shown in Figure 1-16.



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Figure 1-16: PCI Express Clock

PCIe lane width/size is selected by jumper J74 (Figure 1-17). The default lane size selection is 8-lane (J74 pins 5 and 6 jumpered).



X18381-113016

Figure 1-17: PCI Express Lane Size Select Jumper J74

Table 1-12 details the PCIe P1 edge connector wiring to FPGA U1.

Table 1-12: KCU105 Board FPGA U1 to PCIe Edge P1 Connections

| FPGA (U1) Pin | Schematic Net Name | PCIe Edge P1 | |
|---------------|--------------------|--------------|----------|
| | | Pin Number | Pin Name |
| AN4 | PCIE_TX7_P | A47 | PERp7 |
| AN3 | PCIE_TX7_N | A48 | PERn7 |
| AP2 | PCIE_RX7_P | B45 | PETp7 |
| AP1 | PCIE_RX7_N | B46 | PETn7 |
| AM6 | PCIE_TX6_P | A43 | PERp6 |
| AM5 | PCIE_TX6_N | A44 | PERn6 |
| AM2 | PCIE_RX6_P | B41 | PETp6 |
| AM1 | PCIE_RX6_N | B42 | PETn6 |
| AL4 | PCIE_TX5_P | A39 | PERp5 |
| AL3 | PCIE_TX5_N | A40 | PERn5 |
| AK2 | PCIE_RX5_P | B37 | PETp5 |
| AK1 | PCIE_RX5_N | B38 | PETn5 |
| AK6 | PCIE_TX4_P | A35 | PERp4 |
| AK5 | PCIE_TX4_N | A36 | PERn4 |
| AJ4 | PCIE_RX4_P | B33 | PETp4 |
| AJ3 | PCIE_RX4_N | B34 | PETn4 |
| AH6 | PCIE_TX3_P | A29 | PERp3 |
| AH5 | PCIE_TX3_N | A30 | PERn3 |
| AH2 | PCIE_RX3_P | B27 | PETp3 |
| AH1 | PCIE_RX3_N | B28 | PETn3 |
| AG4 | PCIE_TX2_P | A25 | PERp2 |
| AG3 | PCIE_TX2_N | A26 | PERn2 |
| AF2 | PCIE_RX2_P | B23 | PETp2 |
| AF1 | PCIE_RX2_N | B24 | PETn2 |
| AE4 | PCIE_TX1_P | A21 | PERp1 |
| AE3 | PCIE_TX1_N | A22 | PERn1 |
| AD2 | PCIE_RX1_P | B19 | PETp1 |
| AD1 | PCIE_RX1_N | B20 | PETn1 |
| AC4 | PCIE_TX0_P | A16 | PERp0 |
| AC3 | PCIE_TX0_N | A17 | PERn0 |
| AB2 | PCIE_RX0_P | B14 | PETp0 |
| AB1 | PCIE_RX0_N | B15 | PETn0 |

Table 1-12: KCU105 Board FPGA U1 to PCIe Edge P1 Connections (Cont'd)

| FPGA (U1) Pin | Schematic Net Name | PCIe Edge P1 | |
|---------------|--------------------|--------------|----------|
| | | Pin Number | Pin Name |
| AB6 | PCIE_CLK_QO_P | A13 | REFCLK+ |
| AB5 | PCIE_CLK_QO_N | A14 | REFCLK- |

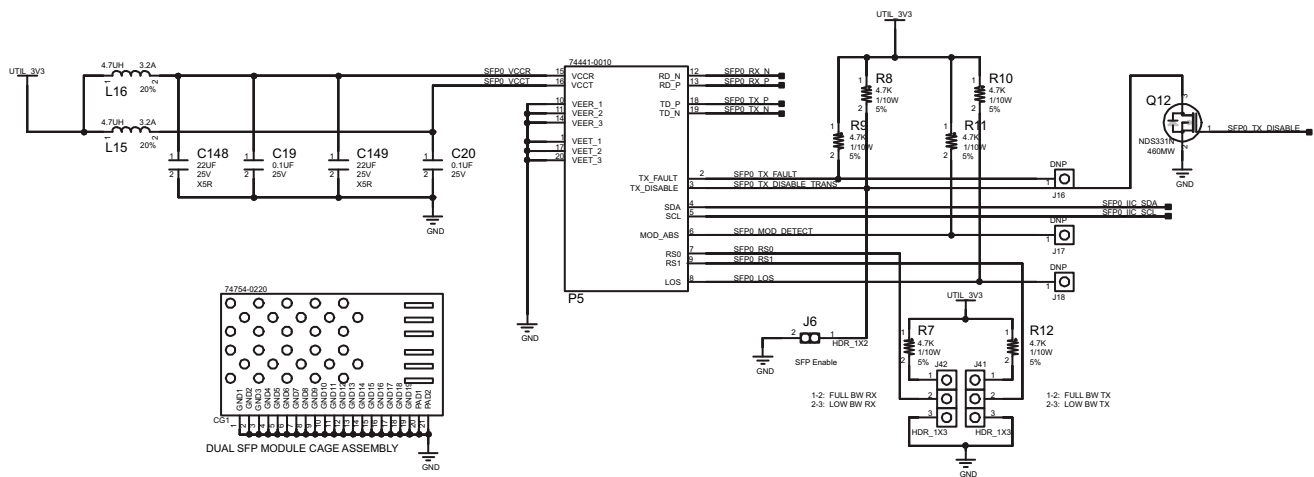
SFP/SFP+ Module Connectors

[Figure 1-2, callout 15]

The KCU105 board hosts two small form-factor pluggable (SFP/SFP+) P4 and P5 that accept SFP or SFP+ modules. The connectors are housed within a single dual SFP cage assembly.

The SFP transmit and receive signal data paths are routed with a differential characteristic impedance of 100Ω (±10%) with an insertion loss of <4 dB up to 8 GHz.

Figure 1-18 shows SFP/SFP+ module connector circuitry typical of the two implementations.



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Figure 1-18: SFP/SFP+ Module Connector

Table 1-13 lists the SFP+ module connections to FPGA U1.

Table 1-13: KCU105 Board FPGA U1 to SFP0 and SFP1 Module Connections

| FPGA (U1) Pin | Schematic Net Name | FPGA (U1) Direction | Pin Number | Pin Name | SFP/SFP+ Module |
|---------------|--------------------|---------------------|------------|------------|-----------------|
| T2 | SFP0_RX_P | Input | 13 | RD_P | SFP0 P5 |
| T1 | SFP0_RX_N | Input | 12 | RD_N | |
| U4 | SFP0_TX_P | Output | 18 | TD_P | |
| U3 | SFP0_TX_N | Output | 19 | TD_N | |
| AL8 | SFP0_TX_DISABLE | Output | 3 | TX_DISABLE | |
| V2 | SFP1_RX_P | Input | 13 | RD_P | SFP1 P4 |
| V1 | SFP1_RX_N | Input | 12 | RD_N | |
| W4 | SFP1_TX_P | Output | 18 | TD_P | |
| W3 | SFP1_TX_N | Output | 19 | TD_N | |
| D28 | SFP1_TX_DISABLE | Output | 3 | TX_DISABLE | |

Notes:

1. SFP0_TX_DISABLE, SFP1_TX_DISABLE I/O standard LVCMOS18; MGT connections I/O standard not applicable.

Table 1-14: SFP0 and SFP1 Module Control and Status Connections

| SFP Control/Status Signal | Board Connection | | SFP Module |
|---------------------------|------------------|--|------------|
| SFP_TX_FAULT | Test Point J16 | High = Fault | SFP0 P5 |
| | | Low = Normal operation | |
| SFP_TX_DISABLE | Jumper J6 | Off = SFP Disabled | |
| | | On = SFP Enabled | |
| SFP_MOD_DETECT | Test Point J17 | High = Module not present | |
| | | Low = Module present | |
| SFP_RS0 | Jumper J42 | Jumper pins 1-2 = Full RX bandwidth | |
| | | Jumper pins 2-3 = Reduced RX bandwidth | |
| SFP_RS1 | Jumper J41 | Jumper pins 1-2 = Full RX bandwidth | |
| | | Jumper pins 2-3 = Reduced RX bandwidth | |
| SFP_LOS | Test Point J18 | High = Loss of receiver signal | |
| | | Low = Normal operation | |

Table 1-14: SFP0 and SFP1 Module Control and Status Connections (Cont'd)

| SFP Control/Status Signal | Board Connection | | SFP Module |
|---------------------------|------------------|--|------------|
| SFP_TX_FAULT | Test Point J19 | High = Fault | SFP1 P4 |
| | | Low = Normal operation | |
| SFP_TX_DISABLE | Jumper J7 | Off = SFP Disabled | |
| | | On = SFP Enabled | |
| SFP_MOD_DETECT | Test Point J20 | High = Module not present | |
| | | Low = Module present | |
| SFP_RS0 | Jumper J44 | Jumper pins 1-2 = Full RX bandwidth | |
| | | Jumper pins 2-3 = Reduced RX bandwidth | |
| SFP_RS1 | Jumper J43 | Jumper pins 1-2 = Full RX bandwidth | |
| | | Jumper pins 2-3 = Reduced RX bandwidth | |
| SFP_LOS | Test Point J21 | High = Loss of receiver signal | |
| | | Low = Normal operation | |

For additional information about the enhanced Small Form Factor Pluggable (SFP+) module, see the SFF-8431 specification [Ref 17].

10/100/1000 Mb/s Tri-Speed Ethernet PHY

[Figure 1-2, callout 17]

The KCU105 evaluation board uses the Marvell Alaska PHY device (M88E1111) at U58 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through RJ-45 connector P3, a Halo HFJ11-1G01E-L12RL with built-in magnetics and status LEDs.

On power-up, or on reset, the PHY is configured to operate in SGMII mode with PHY address 0b00111 using the settings shown in Table 1-15. These settings can be over written via software commands passed over the MDIO interface.

Table 1-15: Board Connections for PHY Configuration Pins

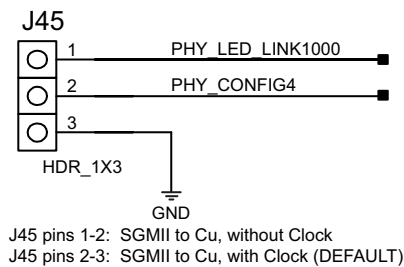
| Pin | Bit[2] | Bit[1] | Bit[0] | Default Values for Bit[2:0] | Setting Description |
|------|-------------|-------------|-------------|-----------------------------|---|
| CFG0 | PHYADR[2] | PHYADR[1] | PHYADR[0] | 111 | PHYAddr 00111. Do not advertise the PAUSE bit. |
| CFG1 | ENA_PAUSE | PHYADR[4] | PHYADR[3] | 000 | |
| CFG2 | ANEG[3] | ANEG[2] | ANEG[1] | 111 | Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 MHz CLK option disabled. |
| CFG3 | ANEG[0] | ENA_XC | DIS_125 | 111 | |
| CFG4 | HWCFG_MD[2] | HWCFG_MD[1] | HWCFG_MD[0] | 100 | SGMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled. |
| CFG5 | DIS_FC | DIS_SLEEP | HWCFG_MD[3] | 110 | |
| CFG6 | SEL_BDT | INT_POL | 75/50Ω | 010 | MDC/MDIO selected. Active-Low interrupt. 50Ω SERDES option. |

Table 1-16: FPGA U1 to Ethernet PHY U58 Connections

| FPGA (U1) Pin | Net Name | I/O Standard | M88E1111 PHY U58 | |
|---------------|-----------|--------------|------------------|----------|
| | | | Pin | Name |
| H26 | PHY_MDIO | LVC MOS18 | M1 | MDIO_SDA |
| L25 | PHY_MDC | LVC MOS18 | L3 | MDC_SCL |
| K25 | PHY_INT | LVC MOS18 | L1 | INT_B |
| J23 | PHY_RESET | LVC MOS18 | K3 | RESET_B |

Notes:

Ethernet PHY_ U58 signals are level-shifted to 1.8V for interface to FPGA U1 bank 65.



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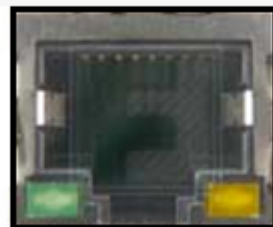
Figure 1-19: Ethernet PHY J45 Configuration Jumper J45

★ Ethernet PHY Status LEDs

[Figure 1-2, callout 17]

The Ethernet PHY status LEDs are integrated into the metal frame of the P3 RJ-45 connector. These LEDs are visible on the left edge of the KCU105 board when it is installed into a PCIe slot in a PC chassis. The two PHY status LEDs are integrated within the frame of the RJ45 Ethernet jack as shown in [Figure 1-20](#).

FastJack Single Port RJ45 Right Angle LED
Green/Yellow Ethernet Modular Jack



Link Rate
1000
(Mbps)

TX
Direction
Indicator

X18385-113016

Figure 1-20: Ethernet PHY Status LEDs

Details about the tri-mode Ethernet MAC core are provided in *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051) [\[Ref 18\]](#).

The product brief for the Marvell M88E1111 Alaska Gigabit Ethernet Transceiver is available on the Marvell Semiconductor website [\[Ref 19\]](#). The data sheet can be obtained under NDA from Marvell. The contact information is on the Marvell Semiconductor website [\[Ref 19\]](#).

Dual USB-to-UART Bridge

[Figure 1-2, callout 19]

The KCU105 evaluation board contains a Silicon Labs CP2105GM dual USB-to-UART bridge device (U34) which allows a connection to a host computer with a USB port. The USB cable is supplied in the KCU105 evaluation board kit (Standard Type-A end to host computer, Type Micro-B end to KCU105 evaluation board connector J4). The CP2105GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the KCU105 evaluation board.

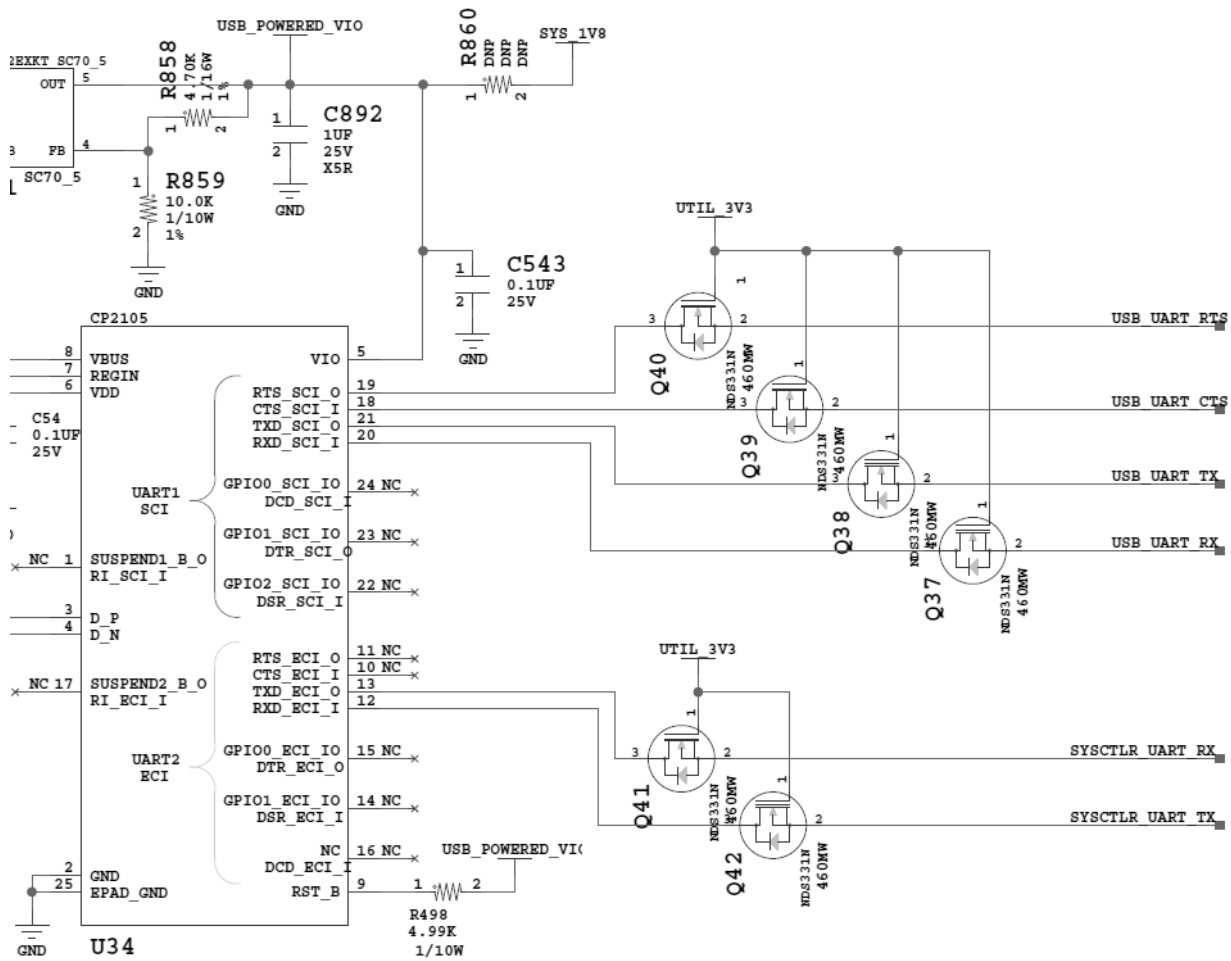
The dual UART interface connections are split between two components:

- UART1 SCI (standard) 4-wire interface is connected to the XCKU040 U1 device
- UART2 ECI (enhanced) 2-wire interface is connected to the XC7Z010 U111 Zynq-7000 SoC system controller

Table 1-17 lists the dual-UART U34 connections to FPGA U1.

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART bridge to appear as a pair of COM ports to communications application software (for example, Tera Term or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the KCU105 evaluation board. The driver assigns the higher PC COM port number to UART1 (SCI) and the lower PC COM port number to UART2 (ECI).

The Silicon Labs CP2105GM dual USB-to-UART bridge circuit is shown in Figure 1-21.



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Figure 1-21: KCU105 Board Dual UART CP2105GM U34

Table 1-17 lists the CP2105GM connections to FPGA U1.

Table 1-17: FPGA U1 to CP2105GM U34 Connections

| FPGA (U1) Pin | Function | Direction | I/O Standard | Schematic Net Name | CP2105GM Device (U34) | | |
|--|----------|-----------|--------------|--------------------|-----------------------|----------|-----------|
| | | | | | Pin | Function | Direction |
| XCKU040 FPGA (U1) - UART1 SCI ⁽¹⁾ | | | | | | | |
| G25 | RX | Input | LVC MOS18 | USB_UART_TX | 21 | TXD | Output |
| K26 | TX | Output | LVC MOS18 | USB_UART_RX | 20 | RXD | Input |
| L23 | CTS | Output | LVC MOS18 | USB_UART_CTS | 18 | CTS | Input |
| K27 | RTS | Input | LVC MOS18 | USB_UART_RTS | 19 | RTS | Output |

Notes:

1. The USB_UART_sig nets are named from the perspective of the CP2105GM device (U34).

For more technical information on the CP2105GM and the VCP drivers, see the Silicon Labs website [\[Ref 11\]](#).

Xilinx UART IP is expected to be implemented in the FPGA logic using IP as described in the *LogiCORE IP AXI UART Lite Product Guide* (PG142) [\[Ref 20\]](#).

HDMI Video Output

[Figure 1-2, callout 20]

The KCU105 evaluation board provides a HDMI video output using an Analog Devices ADV7511KSTZ-P HDMI transmitter at U52. The HDMI transmitter U52 is connected to the XCKU040 device bank 64 and its output is provided on a Molex 500254-1927 HDMI type-A receptacle at P6. The ADV7511 supports 1080P 60 Hz, YCbCr 4:2:2 encoding via 16-bit input data mapping.

The KCU105 evaluation board supports these HDMI device interfaces:

- 16 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out Pin to FPGA
- I2C
- SPDIF

The HDMI U52 circuit is shown in Figure 1-22.

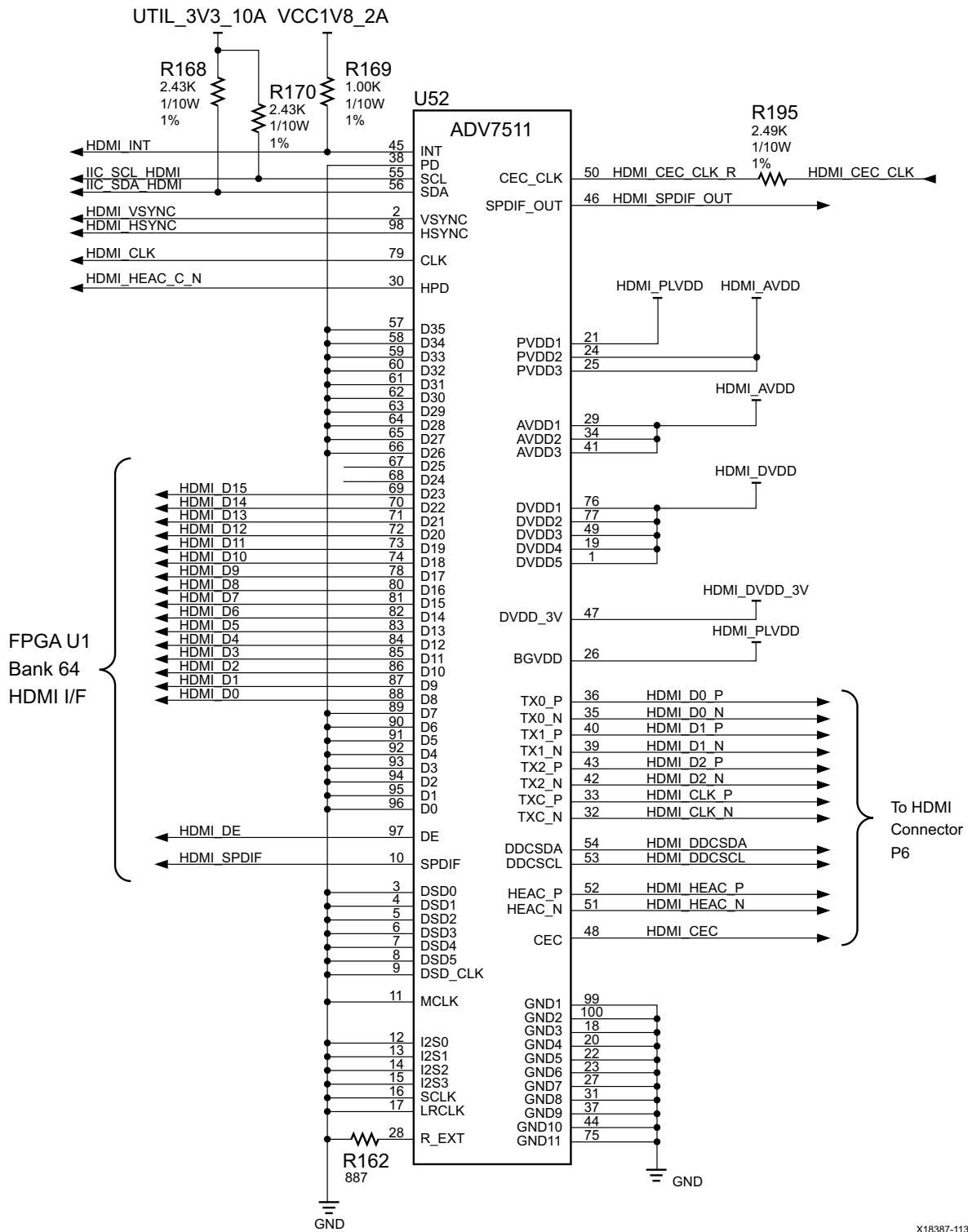


Figure 1-22: HDMI Codec Circuit

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Table 1-18 lists the HDMI Codec U52 to the XCKU040 device U1 connections. All HDMI nets in this table are series resistor coupled.

Table 1-18: HDMI Codec U52 to XCKU040 Device U1 Connections

| FPGA (U1) Pin | Schematic Net Name | FPGA (U1) Direction | I/O Standard | ADV7511 U52 | |
|------------------|-------------------------|------------------------|--------------|-------------|-----------|
| | | | | Pin Number | Name |
| AK11 | HDMI_D0 | Output | LVC MOS18 | 88 | D8 |
| AP11 | HDMI_D1 | Output | LVC MOS18 | 87 | D9 |
| AP13 | HDMI_D2 | Output | LVC MOS18 | 86 | D10 |
| AN13 | HDMI_D3 | Output | LVC MOS18 | 85 | D11 |
| AN11 | HDMI_D4 | Output | LVC MOS18 | 84 | D12 |
| AM11 | HDMI_D5 | Output | LVC MOS18 | 83 | D13 |
| AN12 | HDMI_D6 | Output | LVC MOS18 | 82 | D14 |
| AM12 | HDMI_D7 | Output | LVC MOS18 | 81 | D15 |
| AL12 | HDMI_D8 | Output | LVC MOS18 | 80 | D16 |
| AK12 | HDMI_D9 | Output | LVC MOS18 | 78 | D17 |
| AL13 | HDMI_D10 | Output | LVC MOS18 | 74 | D18 |
| AK13 | HDMI_D11 | Output | LVC MOS18 | 73 | D19 |
| AD11 | HDMI_D12 | Output | LVC MOS18 | 72 | D20 |
| AH12 | HDMI_D13 | Output | LVC MOS18 | 71 | D21 |
| AG12 | HDMI_D14 | Output | LVC MOS18 | 70 | D22 |
| AJ11 | HDMI_D15 | Output | LVC MOS18 | 69 | D23 |
| AE11 | HDMI_DE | Output | LVC MOS18 | 97 | DE |
| AE12 | HDMI_SPDIF | Output | LVC MOS18 | 10 | SPDIF |
| AF13 | HDMI_CLK | Output | LVC MOS18 | 79 | CLK |
| AH13 | HDMI_VSYNC | Output | LVC MOS18 | 2 | VSYNC |
| AE13 | HDMI_HSYNC | Output | LVC MOS18 | 98 | HSYNC |
| AJ13 | HDMI_INT ⁽¹⁾ | Input | LVC MOS18 | 45 | INT |
| AF12 | HDMI_SPDIF_OUT | Input | LVC MOS18 | 46 | SPDIF_OUT |

Notes:

1. The HDMI_INT net is direct coupled (no series resistor).

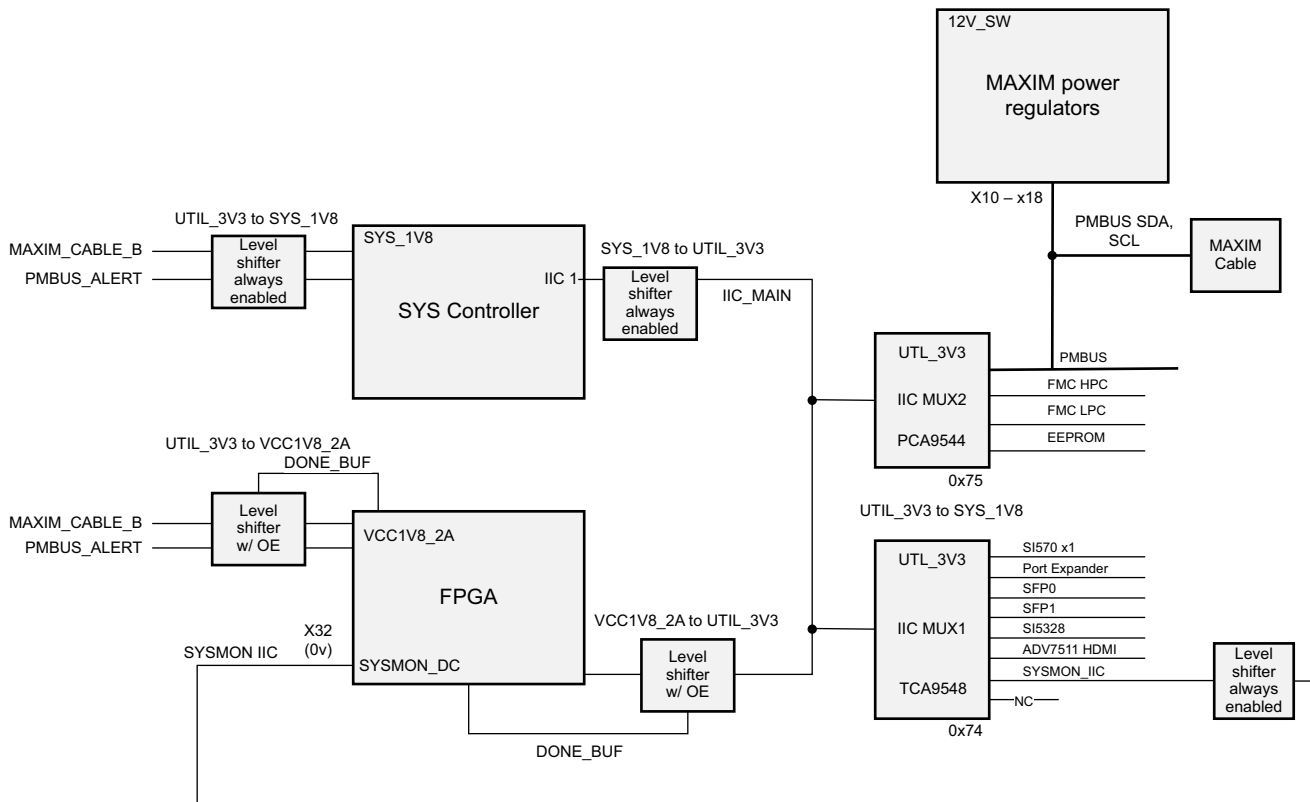
For more information about the Analog Devices ADV7511KSTZ-P, see the Analog Devices website [Ref 21]. For additional information about HDMI IP options, see the *DisplayPort LogiCORE Product Guide* (PG064) [Ref 22].

I2C Bus, Topology, and Switches

[Figure 1-2, callouts 21, 22]

The KCU105 evaluation board implements a 2-to-1 I2C bus arrangement. A single I2C bus from the FPGA U1 XCKU040 (IIC_MAIN_SCL/SDA_LS) and system controller Zynq-7000 SoC U111 (SYSCTLR_I2C_SCL/SDA) is wired to the main I2C bus via level-shifters. FPGA U1 is wired through level-shifter U77 and system controller U111 is wired through level-shifter U108. The output sides of U77 and U108 are wired in parallel to the main I2C bus (IIC_SDA and _SCL_MAIN). This common main I2C bus is then routed to a pair of bus switches, a TI TCA9548 1-to-8 channel I2C bus switch (U28) and a TI PCA9544 1-to-4 channel I2C bus switch (U80). The bus switches can operate at speeds up to 400 kHz.

The KCU105 evaluation board I2C bus topology overview is shown in Figure 1-23 and Table 1-19 lists the address for each device on the I2C bus.



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Figure 1-23: I2C Bus Topology Overview

Note: See Table 1-19 for device I2C address assignments.



IMPORTANT: The TCA9548 U28 RESET_B pin 3 is connected to FPGA U1 bank 64 pin AP10 via level-shifter U44. The PCA9544 does not have a reset pin. FPGA pin AP10 LVCMOS18 net IIC_MUX_RESET_B_LS must be driven High to enable I2C bus transactions with the devices connected to U28.

User FPGA applications that communicate with devices on one of the downstream I2C buses must first set up a path to the desired target bus through the U28 or U80 bus switch at I2C address 0x74 (0b1110100) or 0x75 (0b1110101), respectively. Table 1-19 lists the address for each device on the I2C bus.

Table 1-19: I2C Devices

| I2C Devices | I2C Switch Position | I2C Address | | Device |
|------------------------------|---------------------|--------------------------|-------------|----------------|
| | | Binary Format | Hex Format | |
| TCA9548 8-channel bus switch | N/A | 0b1110100 | 0x74 | U28 TCA9548 |
| Si570 clock | 0 | 0b1011101 | 0x5D | U32 Si570 |
| I2C port expander | 1 | 0b0100001 | 0x21 | U89 TCA6416 |
| SFP module 0 (SFP0) | 2 | 0b1010000 | 0x50 | P5 SFP0 |
| SFP module 1 (SFP1) | 3 | 0b1010000 | 0x50 | P4 SFP1 |
| Si5328 clock | 4 | 0b1101000 | 0x68 | U57 Si5328B |
| ADV7511 HDMI | 5 | 0b0111001 | 0x39 | U52 ADV7511 |
| FPGA SYSMON | 6 | 0b0110010 | 0x32 | U1 SYSMON |
| Not used | 7 | N/A | N/A | N/A |
| | | | | |
| PCA9544 4-channel bus switch | N/A | 0b1110101 | 0x75 | U80 PCA9544 |
| PMBUS regulators | 0 | 0b0010000 - 0b0011000 | 0x10 - 0x18 | MAX15301/3 (1) |
| FMC HPC | 1 | 0bXXXXXXXX | 0x## | J22 FMC HPC |
| FMC LPC | 2 | 0bXXXXXXXX | 0x## | J2 FMC LPC |
| I2C EEPROM | 3 | 0b1010100 | 0x54 | U12 M24C08 |

Notes:

MAX15301: U29,U30,U31; MAX15303: U3,U4,U6,U7,U8,U9,U10.

Information on the TCA9548 and PCA9544 is available on the Texas Instruments website [\[Ref 23\]](#).

For additional information on the Zynq-7000 SoC device I2C controller, see *Zynq-7000 SoC Overview Data Sheet (DS190)* [\[Ref 24\]](#) and *Zynq-7000 SoC Technical Reference Manual (UG585)* [\[Ref 25\]](#).

Status and User LEDs

Table 1-20 defines KCU105 board status and user LEDs.

Table 1-20: KCU105 Board Status and User LEDs

| Reference Designator | Description |
|----------------------|-------------------------------|
| DS2 | INIT |
| DS3 | OR'D POWER GOOD |
| DS4 | CP2105 DUAL UART GPIO0_ECI_IO |
| DS5 | CP2105 DUAL UART GPIO0_SCI_IO |
| DS6 | GPIO_LED_1 |
| DS7 | GPIO_LED_0 |
| DS8 | GPIO_LED_2 |
| DS9 | GPIO_LED_5 |
| DS10 | GPIO_LED_4 |
| DS14 | UTIL_3V3_PGOOD |
| DS15 | MGTAVCC_PGOOD |
| DS16 | VCC1V2_PGOOD |
| DS17 | MGTAVTT_PGOOD |
| DS18 | VCCAUX_PGOOD |
| DS19 | VADJ_1V8_PGOOD |
| DS21 | VCCINT_PGOOD |
| DS23 | VCCBRAM_PGOOD |
| DS24 | VCC1V8_PGOOD |
| DS25 | MGTVCCAUX_PGOOD |
| DS26 | 12V ON |
| DS27 | SYS_2V5 ON |
| DS28 | SYS_1V8 ON |
| DS31 | GPIO_LED_7 |
| DS32 | GPIO_LED_6 |
| DS33 | GPIO_LED_5 |
| DS34 | DONE |
| DS36 | DDR4 VTT ON |
| DS37 | CP2105 DUAL UART GPIO1_SCI_IO |
| DS38 | CP2105 DUAL UART GPIO1_ECI_IO |
| DS42 | SYSCTLR INIT |
| DS43 | SYSCTLR STATUS |
| DS44 | SYSCTLR DONE |

Table 1-20: KCU105 Board Status and User LEDs (Cont'd)

| Reference Designator | Description |
|----------------------|-------------------|
| DS45 | SYSCTLR ERROR |
| DS46 | SYS_1VO ON |
| DS49 | 5V ON |
| EPHY P3 GREEN LED | ENET PHY LINK1000 |
| EPHY P3 YELLOW LED | ENET PHY TX |

User I/O

[Figure 1-2, callouts 23-26, 40]

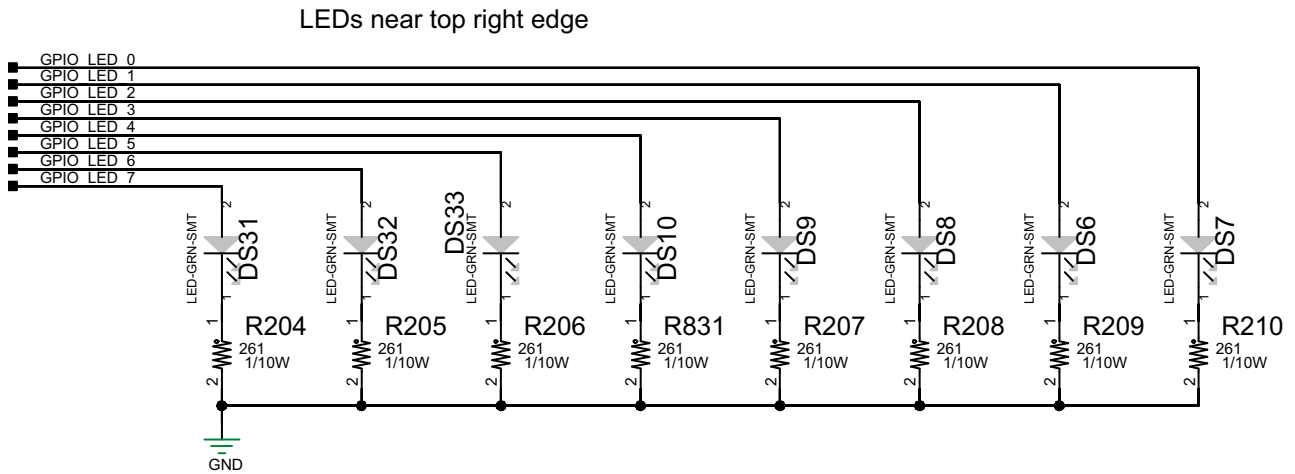
The KCU105 board provides these user and general purpose I/O capabilities:

- Eight user LEDs (callout 23)
 - GPIO_LED[7-0]: DS31, DS32, DS33, DS10, DS19, DS8, DS6, DS7
- Five user pushbuttons and CPU reset switch (callout 24)
 - GPIO_SW_[NESWC]: SW10, SW9, SW8, SW6, SW7
 - CPU_RESET: SW5
- 4-position user DIP Switch (callout 25)
 - GPIO_DIP_SW[3:0]: SW12
- User Rotary Switch (callout 40)
 - ROTARY_PUSH, ROTARY_INCA, ROTARY_INCB: SW13
- User SMA (callout 26)
 - USER_SMA_GPIO_P, USER_SMA_GPIO_N: J36, J37

User GPIO LEDs

[Figure 1-2, callout 23]

Figure 1-24 shows the GPIO LED circuit.



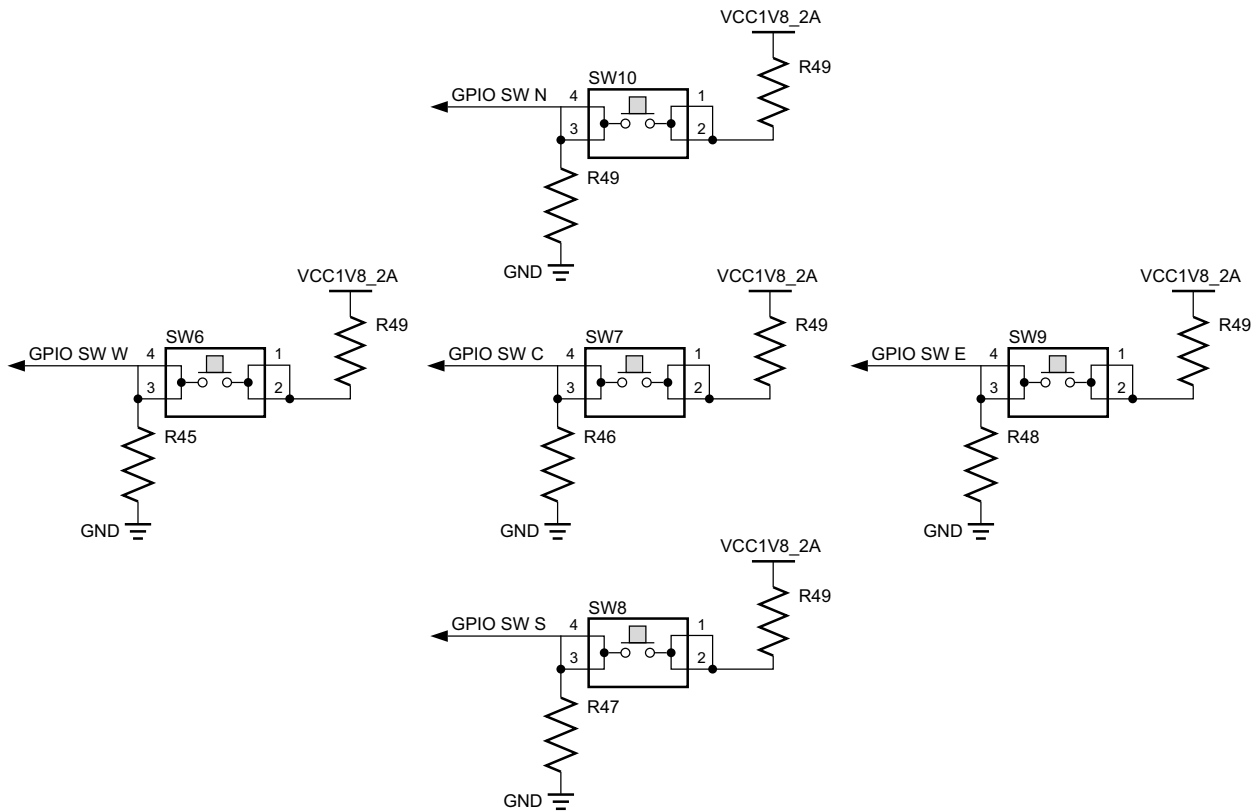
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Figure 1-24: User LEDs

User Pushbuttons

[Figure 1-2, callout 24]

Figure 1-25 shows the user pushbuttons circuit.



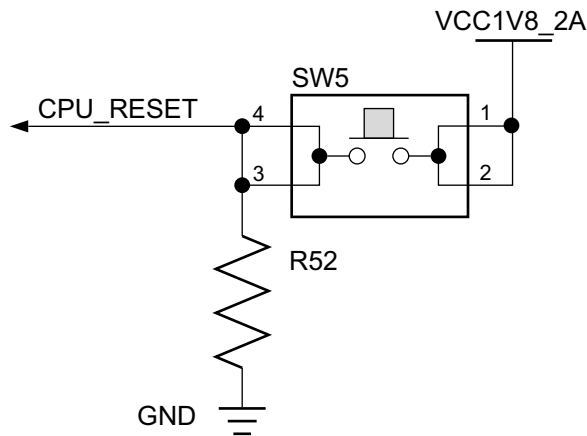
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Figure 1-25: User Pushbuttons

CPU Reset Pushbutton

[Figure 1-2, callout 25]

Figure 1-26 shows the CPU reset pushbutton circuit.



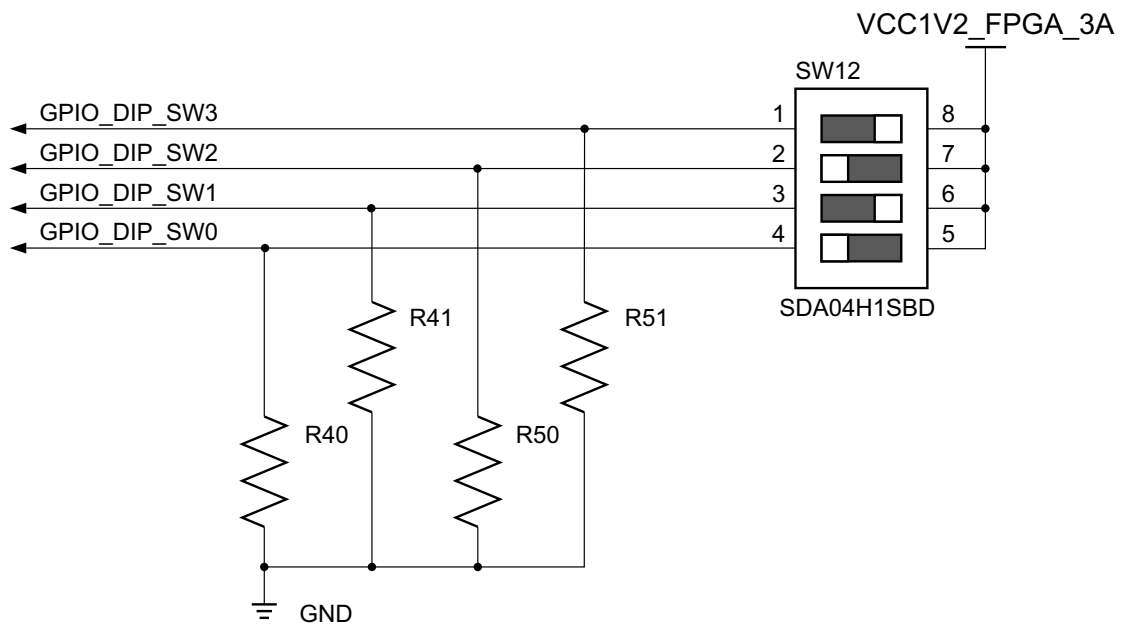
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Figure 1-26: CPU Reset Pushbutton

GPIO DIP Switch

[Figure 1-2, callout 26]

Figure 1-27 shows the GPIO DIP switch circuit.



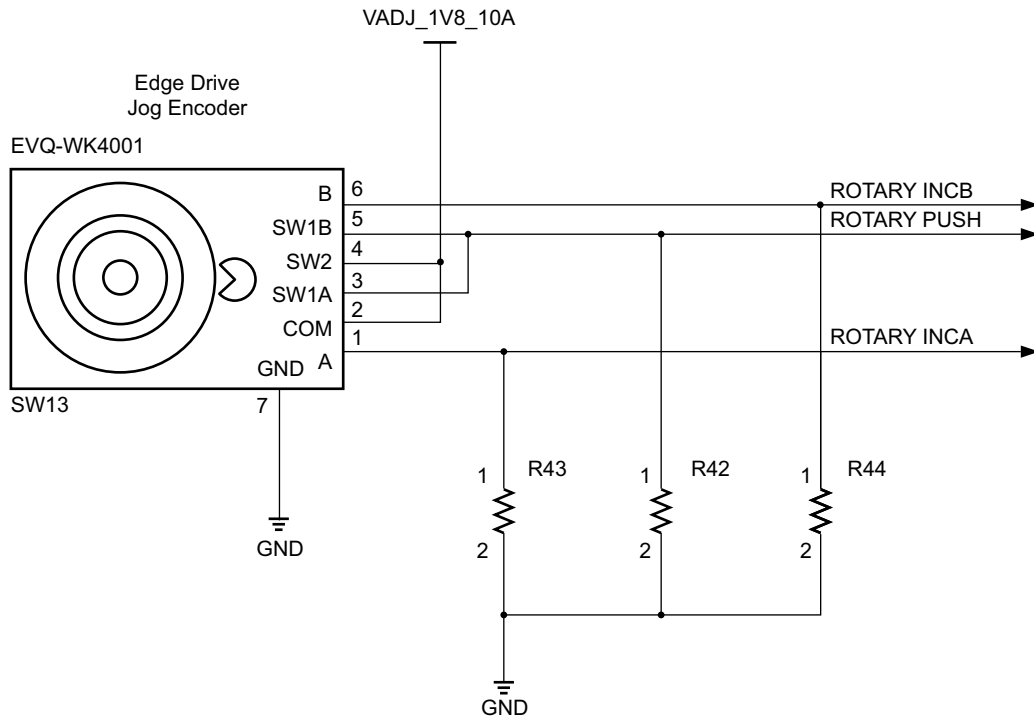
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Figure 1-27: CPU GPIO DIP Switch

Rotary Switch

[Figure 1-2, callout 40]

Figure 1-28 shows the rotary switch SW13.



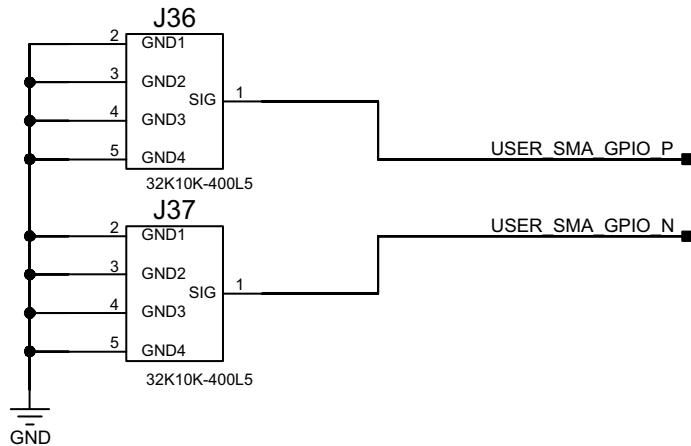
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Figure 1-28: Rotary Switch SW13

User SMA GPIO

[Figure 1-2, callout 11]

Figure 1-29 shows the GPIO SMAs J36 and J37.



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Figure 1-29: GPIO SMAs J36 and J37

Table 1-21 lists the GPIO Connections to FPGA U1.

Table 1-21: KCU105 Board GPIO Connections to FPGA U1

| FPGA (U1) Pin | Schematic Net Name | FPGA (U1) Direction | I/O Standard | Device |
|--|--------------------|---------------------|--------------|------------------|
| GPIO LEDs (Active-High) ⁽¹⁾ | | | | |
| AP8 | GPIO_LED_0 | Output | LVC MOS18 | DS7.1 |
| H23 | GPIO_LED_1 | Output | LVC MOS18 | DS6.1 |
| P20 | GPIO_LED_2 | Output | LVC MOS18 | DS8.1 |
| P21 | GPIO_LED_3 | Output | LVC MOS18 | DS9.1 |
| N22 | GPIO_LED_4 | Output | LVC MOS18 | DS10.1 |
| M22 | GPIO_LED_5 | Output | LVC MOS18 | DS33.1 |
| R23 | GPIO_LED_6 | Output | LVC MOS18 | DS32.1 |
| P23 | GPIO_LED_7 | Output | LVC MOS18 | DS31.1 |
| Directional Pushbuttons (Active-High) | | | | |
| AD10 | GPIO_SW_N | Input | LVC MOS18 | SW10.3, U111.A13 |
| AE8 | GPIO_SW_E | Input | LVC MOS18 | SW9.3, U111.B14 |
| AF9 | GPIO_SW_W | Input | LVC MOS18 | SW6.3, U111.D14 |
| AF8 | GPIO_SW_S | Input | LVC MOS18 | SW8.3, U111.C14 |
| AE10 | GPIO_SW_C | Input | LVC MOS18 | SW7.3, U111.B12 |

Table 1-21: KCU105 Board GPIO Connections to FPGA U1 (Cont'd)

| FPGA (U1) Pin | Schematic Net Name | FPGA (U1) Direction | I/O Standard | Device |
|---|--------------------|------------------------|--------------|--------|
| 4-Pole DIP SW (Active-High) ⁽¹⁾ | | | | |
| AN16 | GPIO_DIP_SW0 | Input | LVC MOS12 | SW12.4 |
| AN19 | GPIO_DIP_SW1 | Input | LVC MOS12 | SW12.3 |
| AP18 | GPIO_DIP_SW2 | Input | LVC MOS12 | SW12.2 |
| AN14 | GPIO_DIP_SW3 | Input | LVC MOS12 | SW12.1 |
| User Rotary Switch (Active-High) ⁽¹⁾ | | | | |
| Y21 | ROTARY_INCA | Input | LVC MOS18 | SW13.1 |
| AD26 | ROTARY_INCB | Input | LVC MOS18 | SW13.6 |
| AF28 | ROTARY_PUSH | Input | LVC MOS18 | SW13.5 |
| User GPIO SMA | | | | |
| G27 | USER_SMA_GPIO_N | I/O | LVC MOS18 | J36.1 |
| H27 | USER_SMA_GPIO_P | I/O | LVC MOS18 | J36.1 |

Notes:

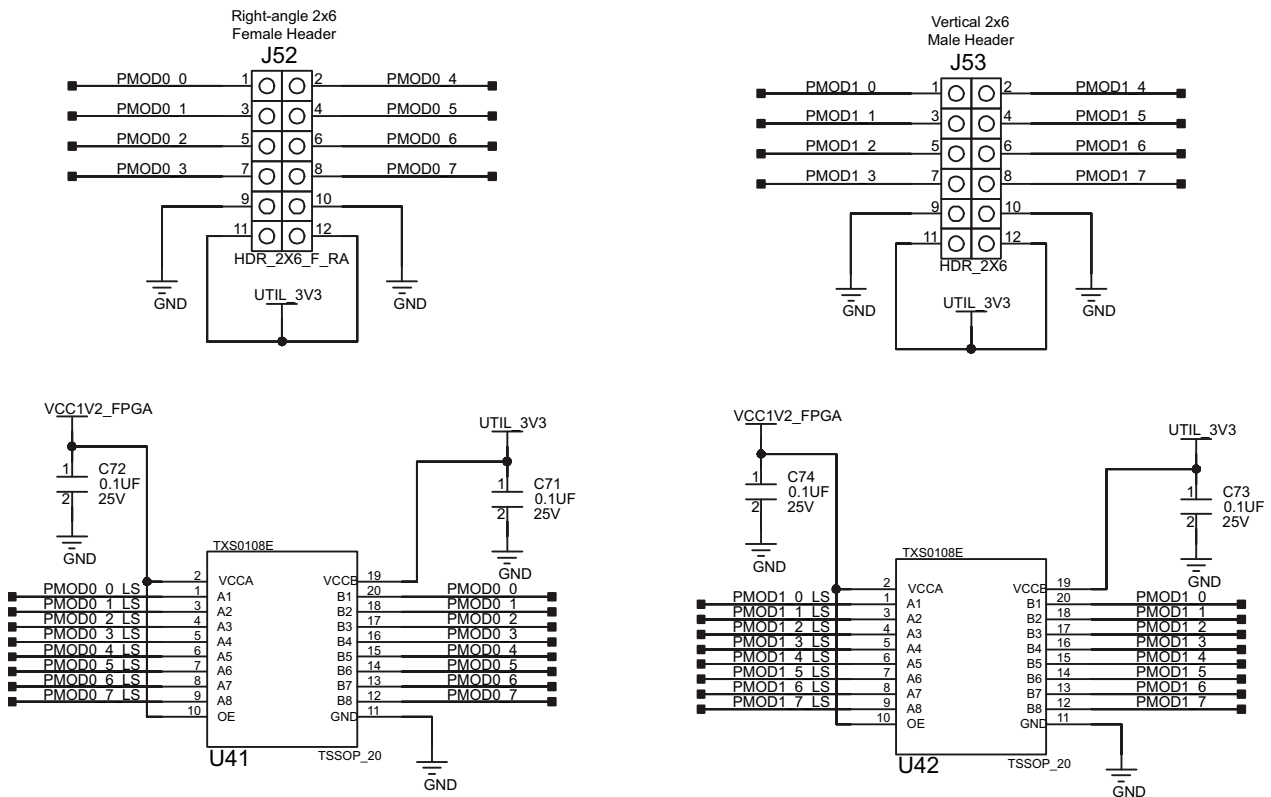
1. Routed through a 3.3V-to-1.8V level-shifter to FPGA.

User PMOD GPIO Headers

[Figure 1-2, callout 34]

The KCU105 evaluation board supports two PMOD GPIO headers J52 (right-angle female) and J53 (vertical male). The PMOD nets connected to these headers are accessed via level-shifters U41 (PMOD0 J52) and U42 (PMOD1 J53). The level-shifters are wired to the XCKU040 device U1 banks 44 and 45.

Figure 1-30 shows the GPIO PMOD headers J52 and J53.



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Figure 1-30: PMOD Connectors J52 and J53 with Level-Shifters U41 and U42

Table 1-22 shows the level-shifter U40 and U41 connections to FPGA U1.

Table 1-22: PMOD Connector J52, J53 Connections via Level-shifter U42, U43 to FPGA U1

| FPGA (U1) Pin | Schematic Net Name | FPGA (U1) Direction | I/O Standard | Level-Shifter | | Schematic Net Name | PMOD Conn. Pin |
|---------------|--------------------|---------------------|--------------|---------------|-------------|--------------------|----------------|
| | | | | Side A 1.2V | Side B 3.3V | | |
| AK25 | PMOD0_0_LS | I/O | LVC MOS12 | U41.1 | U41.20 | PMOD0_0 | J52.1 |
| AN21 | PMOD0_1_LS | I/O | LVC MOS12 | U41.3 | U41.18 | PMOD0_1 | J52.3 |
| AH18 | PMOD0_2_LS | I/O | LVC MOS12 | U41.4 | U41.17 | PMOD0_2 | J52.5 |
| AM19 | PMOD0_3_LS | I/O | LVC MOS12 | U41.5 | U41.16 | PMOD0_3 | J52.7 |
| AE26 | PMOD0_4_LS | I/O | LVC MOS12 | U41.6 | U41.15 | PMOD0_4 | J52.2 |
| AF25 | PMOD0_5_LS | I/O | LVC MOS12 | U41.7 | U41.14 | PMOD0_5 | J52.4 |
| AE21 | PMOD0_6_LS | I/O | LVC MOS12 | U41.8 | U41.13 | PMOD0_6 | J52.6 |
| AM17 | PMOD0_7_LS | I/O | LVC MOS12 | U41.9 | U41.12 | PMOD0_7 | J52.8 |
| AL14 | PMOD1_0_LS | I/O | LVC MOS12 | U42.1 | U42.20 | PMOD1_0 | J53.1 |
| AM14 | PMOD1_1_LS | I/O | LVC MOS12 | U42.3 | U42.18 | PMOD1_1 | J53.3 |
| AP16 | PMOD1_2_LS | I/O | LVC MOS12 | U42.4 | U42.17 | PMOD1_2 | J53.5 |
| AP15 | PMOD1_3_LS | I/O | LVC MOS12 | U42.5 | U42.16 | PMOD1_3 | J53.7 |
| AM16 | PMOD1_4_LS | I/O | LVC MOS12 | U42.6 | U42.15 | PMOD1_4 | J53.2 |
| AM15 | PMOD1_5_LS | I/O | LVC MOS12 | U42.7 | U42.14 | PMOD1_5 | J53.4 |
| AN18 | PMOD1_6_LS | I/O | LVC MOS12 | U42.8 | U42.13 | PMOD1_6 | J53.6 |
| AN17 | PMOD1_7_LS | I/O | LVC MOS12 | U42.9 | U42.12 | PMOD1_7 | J53.8 |

For more information about PMOD connector compatible PMOD modules, see [\[Ref 10\]](#).

Switches

[\[Figure 1-2, callouts 27, 30\]](#)

The KCU105 evaluation board includes a power on-off slide switch and a configuration pushbutton switch:

- Power On/Off Slide Switch SW1 (callout 30)
- FPGA PROG_B SW4, active-Low (callout 27)

Power On/Off Slide Switch SW1

[Figure 1-2, callout 30]

The KCU105 board power switch is SW1. Sliding the switch actuator from the Off to On position applies 12VDC power from the 6-pin mini-fit power input connector J15. Green LED DS26 illuminates when the KCU105 board power is on. See [KCU105 Board Power System](#) for details on the onboard power system.



CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into J15 on the KCU105 evaluation board. The ATX 6-pin connector has a different pinout than J15. Connecting an ATX 6-pin connector to J15 damages the KCU105 evaluation board and voids the board warranty.

The KCU105 evaluation board kit provides the adapter cable shown in [Figure 1-31](#) for powering the KCU105 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to Sourcegate Technologies part number AZCBL-WH-1109-RA4. See [\[Ref 26\]](#) for ordering information.



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Figure 1-31: ATX Power Supply Adapter Cable

FPGA Mezzanine Card Interface

[Figure 1-2, callouts 33, 34]

The KCU105 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification by providing subset implementations of the high pin count (HPC) connector at J22 and low pin count (LPC) version at J2. Both connectors use a 10 x 40 form factor. The HPC connector is populated with 400 pins, while the LPC connector is partially populated with 160 pins. The connectors are keyed so that a mezzanine card, when installed in either of these FMC connectors on the KCU105 evaluation board, faces away from the board.

Connector type:

- Samtec SEAF Series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector

More information about SEAF series connectors is available at the Samtec, Inc. website [Ref 27].

More information about the VITA 57.1 FMC specification is available at the VITA FMC Marketing Alliance website [Ref 28].

FMC HPC Connector J22

[Figure 1-2, callout 33]

The 400-pin HPC connector defined by the FMC specification (Figure B-2) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GTH transceivers
- 2 GTH clocks
- 4 differential clocks
- 159 ground and 15 power connections

The HPC connector at J22 implements a subset of the full FMC HPC connectivity:

- 116 single-ended or 58 differential user-defined pairs (34 LA pairs: LA[00:33]; 24 HA pairs: HA[00:23])
- 8 GTH transceivers
- 2 GTH clocks
- 2 differential clocks
- 159 ground and 15 power connections

The FMC DP[7:0] transmit and receive signal data paths are routed with a differential characteristic impedance of 100Ω (±10%) with an insertion loss of <4 dB up to 8 GHz. The KCU105 board FMC VADJ voltage VADJ_1V8 for the J22 and J2 FMC connectors is sourced by the MAX15301 U30 voltage regulator described in [KCU105 Board Power System](#).

Table 1-23 shows the FMC HPC J22 to the XCKU040 device U1 connections in FMC connector section pairs.

Table 1-23: FMC HPC J22 Connections to XCKU040 Device U1

| J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|-----------------------------------|--------------------|--------------|------------------|---------|---------------------------|--------------|------------------|
| A/B Connections to FPGA U1 | | | | | | | |
| A2 | FMC_HPC_DP1_M2C_P | | D2 | B1 | NC | | |
| A3 | FMC_HPC_DP1_M2C_N | | D1 | B4 | NC | | |
| A6 | FMC_HPC_DP2_M2C_P | | B2 | B5 | NC | | |
| A7 | FMC_HPC_DP2_M2C_N | | B1 | B8 | NC | | |
| A10 | FMC_HPC_DP3_M2C_P | | A4 | B9 | NC | | |
| A11 | FMC_HPC_DP3_M2C_N | | A3 | B12 | FMC_HPC_DP7_M2C_P | | F2 |
| A14 | FMC_HPC_DP4_M2C_P | | M2 | B13 | FMC_HPC_DP7_M2C_N | | F1 |
| A15 | FMC_HPC_DP4_M2C_N | | M1 | B16 | FMC_HPC_DP6_M2C_P | | K2 |
| A18 | FMC_HPC_DP5_M2C_P | | H2 | B17 | FMC_HPC_DP6_M2C_N | | K1 |
| A19 | FMC_HPC_DP5_M2C_N | | H1 | B20 | FMC_HPC_GBTCLK1_M2C_P (1) | LVDS | H6 |
| A22 | FMC_HPC_DP1_C2M_P | | D6 | B21 | FMC_HPC_GBTCLK1_M2C_N (1) | LVDS | H5 |
| A23 | FMC_HPC_DP1_C2M_N | | D5 | B24 | NC | | |
| A26 | FMC_HPC_DP2_C2M_P | | C4 | B25 | NC | | |
| A27 | FMC_HPC_DP2_C2M_N | | C3 | B28 | NC | | |
| A30 | FMC_HPC_DP3_C2M_P | | B6 | B29 | NC | | |
| A31 | FMC_HPC_DP3_C2M_N | | B5 | B32 | FMC_HPC_DP7_C2M_P | | G4 |
| A34 | FMC_HPC_DP4_C2M_P | | N4 | B33 | FMC_HPC_DP7_C2M_N | | G3 |
| A35 | FMC_HPC_DP4_C2M_N | | N3 | B36 | FMC_HPC_DP6_C2M_P | | L4 |
| A38 | FMC_HPC_DP5_C2M_P | | J4 | B37 | FMC_HPC_DP6_C2M_N | | L3 |
| A39 | FMC_HPC_DP5_C2M_N | | J3 | B40 | NC | | |
| C/D Connections to FPGA U1 | | | | | | | |
| C2 | FMC_HPC_DP0_C2M_P | | F6 | D1 | VADJ_1V8_PGOOD (2) | LVC MOS18 | U30.32 |
| C3 | FMC_HPC_DP0_C2M_N | | F5 | D4 | FMC_HPC_GBTCLK0_M2C_P (1) | LVDS | K6 |
| C6 | FMC_HPC_DP0_M2C_P | | E4 | D5 | FMC_HPC_GBTCLK0_M2C_N (1) | LVDS | K5 |
| C7 | FMC_HPC_DP0_M2C_N | | E3 | D8 | FMC_HPC_LA01_CC_P | LVDS | G9 |
| C10 | FMC_HPC_LA06_P | LVDS | D13 | D9 | FMC_HPC_LA01_CC_N | LVDS | F9 |
| C11 | FMC_HPC_LA06_N | LVDS | C13 | D11 | FMC_HPC_LA05_P | LVDS | L13 |

Table 1-23: FMC HPC J22 Connections to XCKU040 Device U1 (Cont'd)

| J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|-----------------------------------|--------------------------------|--------------|------------------|---------|---------------------------------------|--------------|-----------------------------|
| C14 | FMC_HPC_LA10_P | LVDS | L8 | D12 | FMC_HPC_LA05_N | LVDS | K13 |
| C15 | FMC_HPC_LA10_N | LVDS | K8 | D14 | FMC_HPC_LA09_P | LVDS | J9 |
| C18 | FMC_HPC_LA14_P | LVDS | B10 | D15 | FMC_HPC_LA09_N | LVDS | H9 |
| C19 | FMC_HPC_LA14_N | LVDS | A10 | D17 | FMC_HPC_LA_13_P | LVDS | D9 |
| C22 | FMC_HPC_LA18 | LVDS | E22 | D18 | FMC_HPC_LA_13_N | LVDS | C9 |
| C23 | FMC_HPC_LA18 | LVDS | E23 | D20 | FMC_HPC_LA17_CC_P | LVDS | D24 |
| C26 | FMC_HPC_LA27 | LVDS | H21 | D21 | FMC_HPC_LA17_CC_N | LVDS | C24 |
| C27 | FMC_HPC_LA27 | LVDS | G21 | D23 | FMC_HPC_LA23_P | LVDS | G22 |
| C30 | FMC_HPC_IIC_SCL ⁽⁶⁾ | | U80.9 | D24 | FMC_HPC_LA23_N | LVDS | F22 |
| C31 | FMC_HPC_IIC_SDA ⁽⁶⁾ | | U80.8 | D26 | FMC_HPC_LA26_P | LVDS | G20 |
| C34 | GND | | | D27 | FMC_HPC_LA_26_N | LVDS | F20 |
| C35 | VCC12_SW | | | D29 | FMC_HPC_TCK_BUF ⁽³⁾ | | U19.17 |
| C37 | VCC12_SW | | | D30 | FPGA_TDO_FMC_TDI_BUF ⁽⁴⁾ | | U26.1 |
| C39 | UTIL_3V3_10A | | | D31 | FMC_HPC_TDO_LPC_TDI ⁽³⁾⁽⁴⁾ | | U19.21, U26.2, J2.D30 |
| | | | | D32 | UTIL_3V3_10A | | |
| | | | | D33 | FMC_HPC_TMS_BUF ⁽³⁾ | | U19.20 |
| | | | | D34 | NC | | |
| | | | | D35 | GND | | |
| | | | | D36 | UTIL_3V3_10A | | |
| | | | | D38 | UTIL_3V3_10A | | |
| | | | | D40 | UTIL_3V3_10A | | |
| E/F Connections to FPGA U1 | | | | | | | |
| E2 | FMC_HPC_HA01_CC_P | LVDS | E16 | F1 | FMC_HPC_PG_M2C ⁽⁷⁾ | LVC MOS18 | U44.18 |
| E3 | FMC_HPC_HA01_CC_N | LVDS | D16 | F4 | FMC_HPC_HA00_CC_P | LVDS | G17 |
| E6 | FMC_HPC_HA05_P | LVDS | J15 | F5 | FMC_HPC_HA00_CC_N | LVDS | G16 |
| E7 | FMC_HPC_HA05_N | LVDS | J14 | F7 | FMC_HPC_HA04_P | LVDS | G19 |
| E9 | FMC_HPC_HA09_P | LVDS | F18 | F8 | FMC_HPC_HA04_P | LVDS | F19 |
| E10 | FMC_HPC_HA09_N | LVDS | F17 | F10 | FMC_HPC_HA08_P | LVDS | K18 |
| E12 | FMC_HPC_HA13_P | LVDS | B14 | F11 | FMC_HPC_HA08_N | LVDS | K17 |
| E13 | FMC_HPC_HA13_N | LVDS | A14 | F13 | FMC_HPC_HA12_P | LVDS | K16 |
| E15 | FMC_HPC_HA16_P | LVDS | A19 | F14 | FMC_HPC_HA12_N | LVDS | J16 |
| E16 | FMC_HPC_HA16_N | LVDS | A18 | F16 | FMC_HPC_HA15_P | LVDS | D14 |
| E18 | FMC_HPC_HA20_P | LVDS | C19 | F17 | FMC_HPC_HA15_N | LVDS | C14 |

Table 1-23: FMC HPC J22 Connections to XCKU040 Device U1 (Cont'd)

| J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|-----------------------------------|--------------------|--------------|------------------|---------|------------------------------------|--------------|------------------|
| E19 | FMC_HPC_HA20_N | LVDS | B19 | F19 | FMC_HPC_HA19_P | LVDS | D19 |
| E21 | NC | | | F20 | FMC_HPC_HA19_N | LVDS | D18 |
| E22 | NC | | | F22 | NC | | |
| E24 | NC | | | F23 | NC | | |
| E25 | NC | | | F25 | NC | | |
| E27 | NC | | | F26 | NC | | |
| E28 | NC | | | F28 | NC | | |
| E30 | NC | | | F29 | NC | | |
| E31 | NC | | | F31 | NC | | |
| E33 | NC | | | F32 | NC | | |
| E34 | NC | | | F34 | NC | | |
| E36 | NC | | | F35 | NC | | |
| E37 | NC | | | F37 | NC | | |
| E39 | VADJ_1V8 | | | F38 | NC | | |
| | | | | F40 | VADJ_1V8 | | |
| G/H Connections to FPGA U1 | | | | | | | |
| G2 | FMC_HPC_CLK1_M2C_P | LVDS | E25 | H1 | NC | | |
| G3 | FMC_HPC_CLK1_M2C_N | LVDS | D25 | H2 | FMC_HPC_PRSNT_M2C_B ⁽⁵⁾ | LVC MOS18 | U26.4, U44.17 |
| G6 | FMC_HPC_LA00_CC_P | LVDS | H11 | H4 | FMC_HPC_CLK0_M2C_P | LVDS | H12 |
| G7 | FMC_HPC_LA00_CC_N | LVDS | G11 | H5 | FMC_HPC_CLK0_M2C_N | LVDS | G12 |
| G9 | FPC_HPC_LA03_P | LVDS | A13 | H7 | FMC_HPC_LA02_P | LVDS | K10 |
| G10 | FPC_HPC_LA03_N | LVDS | A12 | H8 | FMC_HPC_LA02_N | LVDS | J10 |
| G12 | FMC_HPC_LA08_P | LVDS | J8 | H10 | FMC_HPC_LA04_P | LVDS | L12 |
| G13 | FMC_HPC_LA08_N | LVDS | H8 | H11 | FMC_HPC_LA04_N | LVDS | K12 |
| G15 | FMC_HPC_LA12_P | LVDS | E10 | H13 | FMC_HPC_LA07_P | LVDS | F8 |
| G16 | FMC_HPC_LA12_N | LVDS | D10 | H14 | FMC_HPC_LA07_N | LVDS | E8 |
| G18 | FMC_HPC_LA16_P | LVDS | B9 | H16 | FMC_HPC_LA11_P | LVDS | K11 |
| G19 | FMC_HPC_LA16_N | LVDS | A9 | H17 | FMC_HPC_LA11_N | LVDS | J11 |
| G21 | FMC_HPC_LA20_P | LVDS | B24 | H19 | FMC_HPC_LA15_P | LVDS | D8 |
| G22 | FMC_HPC_LA20_N | LVDS | A24 | H20 | FMC_HPC_LA15_N | LVDS | C8 |
| G24 | FMC_HPC_LA22_P | LVDS | G24 | H22 | FMC_HPC_LA19_P | LVDS | C21 |
| G25 | FMC_HPC_LA22_N | LVDS | F25 | H23 | FMC_HPC_LA19_N | LVDS | C22 |
| G27 | FMC_HPC_LA25_P | LVDS | D20 | H25 | FMC_HPC_LA21_P | LVDS | F23 |
| G28 | FMC_HPC_LA25_N | LVDS | D21 | H26 | FMC_HPC_LA21_N | LVDS | F24 |

Table 1-23: FMC HPC J22 Connections to XCKU040 Device U1 (Cont'd)

| J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|-----------------------------------|--------------------|--------------|------------------|---------|--------------------|--------------|------------------|
| G30 | FMC_HPC_LA29_P | LVDS | B20 | H28 | FMC_HPC_LA24_P | LVDS | E20 |
| G31 | FMC_HPC_LA29_N | LVDS | A20 | H29 | FMC_HPC_LA24_N | LVDS | E21 |
| G33 | FMC_HPC_LA31_P | LVDS | B25 | H31 | FMC_HPC_LA28_P | LVDS | B21 |
| G34 | FMC_HPC_LA31_N | LVDS | A25 | H32 | FMC_HPC_LA28_N | LVDS | B22 |
| G36 | FMC_HPC_LA33_P | LVDS | A27 | H34 | FMC_HPC_LA30_P | LVDS | C26 |
| G37 | FMC_HPC_LA33_N | LVDS | A28 | H35 | FMC_HPC_LA030_N | LVDS | B26 |
| G39 | VADJ_1V8 | | | H37 | FMC_HPC_LA32_P | LVDS | E26 |
| | | | | H38 | FMC_HPC_LA32_N | LVDS | D26 |
| | | | | H40 | VADJ_1V8 | | |
| J/K Connections to FPGA U1 | | | | | | | |
| J2 | NC | | | K1 | NC | | |
| J3 | NC | | | K4 | NC | | |
| J6 | FMC_HPC_HA03_P | LVDS | G15 | K5 | NC | | |
| J7 | FMC_HPC_HA03_N | LVDS | G14 | K7 | FMC_HPC_HA02_P | LVDS | H19 |
| J9 | FMC_HPC_HA07_P | LVDS | L19 | K8 | FMC_HPC_HA02_N | LVDS | H18 |
| J10 | FMC_HPC_HA07_N | LVDS | L18 | K10 | FMC_HPC_HA06_P | LVDS | L15 |
| J12 | FMC_HPC_HA11_P | LVDS | J19 | K11 | FMC_HPC_HA06_N | LVDS | K15 |
| J13 | FMC_HPC_HA11_N | LVDS | J18 | K13 | FMC_HPC_HA10_P | LVDS | H17 |
| J15 | FMC_HPC_HA14_P | LVDS | F15 | K14 | FMC_HPC_HA10_N | LVDS | H16 |
| J16 | FMC_HPC_HA14_N | LVDS | F14 | K16 | FMC_HPC_HA17_CC_P | LVDS | E18 |
| J18 | FMC_HPC_HA18_P | LVDS | B17 | K17 | FMC_HPC_HA17_CC_N | LVDS | E17 |
| J19 | FMC_HPC_HA18_N | LVDS | B16 | K19 | FMC_HPC_HA21_P | LVDS | E15 |
| J21 | FMC_HPC_HA22_P | LVDS | C18 | K20 | FMC_HPC_HA21_N | LVDS | D15 |
| J22 | FMC_HPC_HA22_N | LVDS | C17 | K22 | FMC_HPC_HA23_P | LVDS | B15 |
| J24 | NC | | | K23 | FMC_HPC_HA23_N | LVDS | A15 |
| J25 | NC | | | K25 | NC | | |
| J27 | NC | | | K26 | NC | | |
| J28 | NC | | | K28 | NC | | |
| J30 | NC | | | K29 | NC | | |
| J31 | NC | | | K31 | NC | | |
| J33 | NC | | | K32 | NC | | |
| J34 | NC | | | K34 | NC | | |
| J36 | NC | | | K35 | NC | | |
| J37 | NC | | | K37 | NC | | |
| J39 | NC | | | K38 | NC | | |

Table 1-23: FMC HPC J22 Connections to XCKU040 Device U1 (Cont'd)

| J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J22 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|---------|--------------------|--------------|------------------|---------|--------------------|--------------|------------------|
| | | | | K40 | NC | | |

Notes:

1. Series capacitor coupled to the XCKU040 U1 pin.
2. U30 MAX15301 VADJ_1V8_FPGA voltage regulator power good output signal.
3. XCKU040 U1 JTAG TCK, TMS, TDO pins AC9, W9, U9 buffered by U19 SN74AVC8T245.
4. J22 HPC TDO-TDI connections to U26 HPC FMC JTAG bypass switch (N.C. normally closes/bypassing J22 until an FMC card is plugged into J22).
5. FMC_HPC_PRSNM2C_B is the HPC FMC JTAG bypass switch U26.4 OE control signal and is also connected to the XCKU040 U1 pin H24 via level-shifter U44.
6. Connected to the XCKU040 U1 LS pins J25/J24 IIC_MAIN_SDA/SCL via I2C MUX U80 and level-shifter U77.
7. HPC FMC signal FMC_HPC_PG_M2C is connected to the XCKU040 U1 pin L27 via level-shifter U44.

FMC LPC Connector J2

[Figure 1-2, callout 34]

The 160-pin LPC connector defined by the FMC specification (Figure B-1) provides connectivity for up to:

- 68 single-ended or 34 differential user-defined signals
- 1 GTH transceiver
- 1 GTH clock
- 2 differential clocks
- 61 ground and 9 power connections

The LPC connector at J2 implements the full FMC LPC connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs, LA00-LA33)
- 1 GTH transceiver
- 1 GTH clock
- 2 differential clocks
- 61 ground and 9 power connections

The FMC DP[7:0] transmit and receive signal data paths are routed with a differential characteristic impedance of 100Ω (±10%) with an insertion loss of <4 dB up to 8 GHz.

Table 1-24 shows the FMC LPC J2 to the XCKU040 device U1 connections in FMC connector section pairs.

Table 1-24: FMC LPC J2 Connections to XCKU040 Device U1

| J2 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J2 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|-----------------------------------|--------------------------------|--------------|------------------|--------|------------------------------------|--------------|------------------|
| C/D Connections to FPGA U1 | | | | | | | |
| C2 | FMC_LPC_DP0_C2M_P | | AA4 | D1 | VADJ_1V8_PGOOD ⁽¹⁾ | LVC MOS18 | U30.32 |
| C3 | FMC_LPC_DP0_C2M_N | | AA3 | D4 | FMC_LPC_GBTCLK0_M2C_P | LVDS | T6 |
| C6 | FMC_LPC_DP0_M2C_P | | Y2 | D5 | FMC_LPC_GBTCLK0_M2C_N | LVDS | T5 |
| C7 | FMC_LPC_DP0_M2C_N | | Y1 | D8 | FMC_LPC_LA01_CC_P | LVDS | W25 |
| C10 | FMC_LPC_LA06_P | LVDS | V29 | D9 | FMC_LPC_LA01_CC_N | LVDS | Y25 |
| C11 | FMC_LPC_LA06_N | LVDS | W29 | D11 | FMC_LPC_LA05_P | LVDS | V27 |
| C14 | FMC_LPC_LA10_P | LVDS | T22 | D12 | FMC_LPC_LA05_N | LVDS | V28 |
| C15 | FMC_LPC_LA10_N | LVDS | T23 | D14 | FMC_LPC_LA09_P | LVDS | V26 |
| C18 | FMC_LPC_LA14_P | LVDS | U21 | D15 | FMC_LPC_LA09_N | LVDS | W26 |
| C19 | FMC_LPC_LA14_N | LVDS | U22 | D17 | FMC_LPC_LA13_P | LVDS | AA20 |
| C22 | FMC_LPC_LA18_CC_P | LVDS | AB30 | D18 | FMC_LPC_LA13_N | LVDS | AB20 |
| C23 | FMC_LPC_LA18_CC_N | LVDS | AB31 | D20 | FMC_LPC_LA17_CC_P | LVDS | AA32 |
| C26 | FMC_LPC_LA27_P | LVDS | AG31 | D21 | FMC_LPC_LA17_CC_N | LVDS | AB32 |
| C27 | FMC_LPC_LA27_N | LVDS | AG32 | D23 | FMC_LPC_LA23_P | LVDS | AD30 |
| C30 | FMC_LPC_IIC_SCL ⁽²⁾ | | U80.13 | D24 | FMC_LPC_LA23_N | LVDS | AD31 |
| C31 | FMC_LPC_IIC_SDA ⁽²⁾ | | U80.12 | D26 | FMC_LPC_LA26_P | LVDS | AF33 |
| C34 | GND=0=GND | | | D27 | FMC_LPC_LA_26_N | LVDS | AG34 |
| C35 | VCC12_P | | | D29 | FMC_LPC_TCK_BUF ⁽³⁾ | | U19.16 |
| C37 | VCC12_P | | | D30 | FMC_HPC_TDO_LPC_TDI ⁽⁴⁾ | | U27.2, UG27.1 |
| C39 | VCC3V3 | | | D31 | FMC_LPC_TDO ⁽³⁾⁽⁵⁾ | | U26.2, U55.3 |
| | | | | D32 | VCC3V3 | | |
| | | | | D33 | FMC_LPC_TMS_BUF ⁽³⁾ | | U19.19 |
| | | | | D34 | NC | | |
| | | | | D35 | GND | | |
| | | | | D36 | VCC3V3 | | |
| | | | | D38 | VCC3V3 | | |
| | | | | D40 | VCC3V3 | | |
| G/H Connections to FPGA U1 | | | | | | | |
| G2 | FMC_LPC_CLK1_M2C_P | LVDS | AC31 | H1 | NC | | |
| G3 | FMC_LPC_CLK1_M2C_N | LVDS | AC32 | H2 | FMC_LPC_PRSNM2C_B ⁽⁶⁾ | LVC MOS18 | U27.4, U44.16 |
| G6 | FMC_LPC_LA00_CC_P | LVC MOS18 | W23 | H4 | FMC_LPC_CLK0_M2C_P | LVDS | AA24 |
| G7 | FMC_LPC_LA00_CC_N | LVDS | W24 | H5 | FMC_LPC_CLK0_M2C_N | LVDS | AA25 |

Table 1-24: FMC LPC J2 Connections to XCKU040 Device U1 (Cont'd)

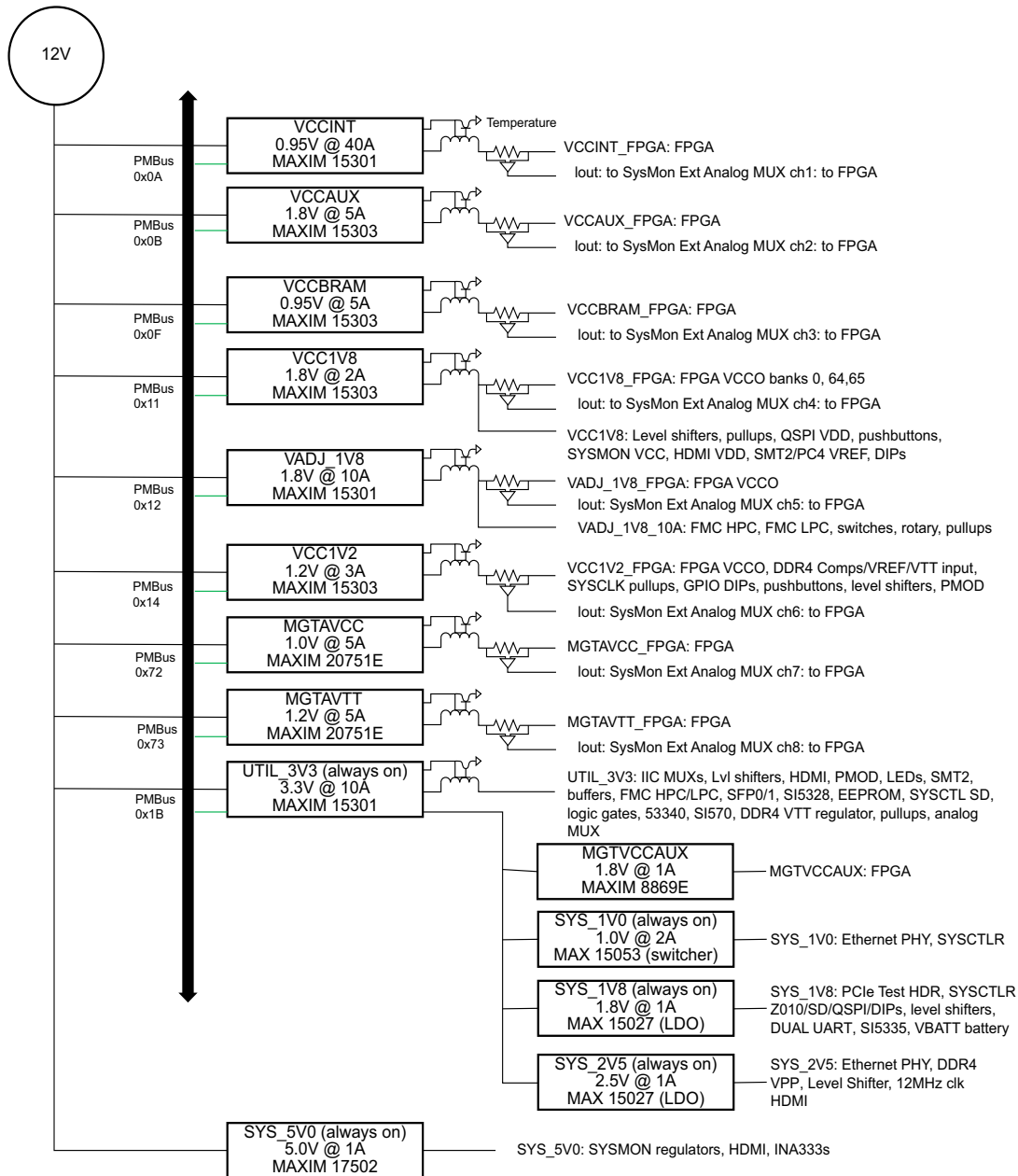
| J2 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin | J2 Pin | Schematic Net Name | I/O Standard | XCKU040 (U1) Pin |
|--------|--------------------|--------------|------------------|--------|--------------------|--------------|------------------|
| G9 | FPC_LPC_LA03_P | LVDS | W28 | H7 | FMC_LPC_LA02_P | LVDS | AA22 |
| G10 | FPC_LPC_LA03_N | LVDS | Y28 | H8 | FMC_LPC_LA02_N | LVDS | AB22 |
| G12 | FMC_LPC_LA08_P | LVDS | U24 | H10 | FMC_LPC_LA04_P | LVDS | U26 |
| G13 | FMC_LPC_LA08_N | LVDS | U25 | H11 | FMC_LPC_LA04_N | LVDS | U27 |
| G15 | FMC_LPC_LA12_P | LVDS | AC22 | H13 | FMC_LPC_LA07_P | LVDS | V22 |
| G16 | FMC_LPC_LA12_N | LVDS | AC23 | H14 | FMC_LPC_LA07_N | LVDS | V23 |
| G18 | FMC_LPC_LA16_P | LVDS | AB21 | H16 | FMC_LPC_LA11_P | LVDS | V21 |
| G19 | FMC_LPC_LA16_N | LVDS | AC21 | H17 | FMC_LPC_LA11_N | LVDS | W21 |
| G21 | FMC_LPC_LA20_P | LVDS | AA34 | H19 | FMC_LPC_LA15_P | LVDS | AB25 |
| G22 | FMC_LPC_LA20_N | LVDS | AB34 | H20 | FMC_LPC_LA15_N | LVDS | AB26 |
| G24 | FMC_LPC_LA22_P | LVDS | AC34 | H22 | FMC_LPC_LA19_P | LVDS | AA29 |
| G25 | FMC_LPC_LA22_N | LVDS | AD34 | H23 | FMC_LPC_LA19_N | LVDS | AB29 |
| G27 | FMC_LPC_LA25_P | LVDS | AE33 | H25 | FMC_LPC_LA21_P | LVDS | AC33 |
| G28 | FMC_LPC_LA25_N | LVDS | AF34 | H26 | FMC_LPC_LA21_N | LVDS | AD33 |
| G30 | FMC_LPC_LA29_P | LVDS | U34 | H28 | FMC_LPC_LA24_P | LVDS | AE32 |
| G31 | FMC_LPC_LA29_N | LVDS | V34 | H29 | FMC_LPC_LA24_N | LVDS | AF32 |
| G33 | FMC_LPC_LA31_P | LVDS | V33 | H31 | FMC_LPC_LA28_P | LVDS | V31 |
| G34 | FMC_LPC_LA31_N | LVDS | W34 | H32 | FMC_LPC_LA28_N | LVDS | W31 |
| G36 | FMC_LPC_LA33_P | LVDS | W33 | H34 | FMC_LPC_LA30_P | LVDS | Y31 |
| G37 | FMC_LPC_LA33_N | LVDS | Y33 | H35 | FMC_LPC_LA030_N | LVDS | Y32 |
| G39 | VADJ_1V8 | | | H37 | FMC_LPC_LA32_P | LVDS | W30 |
| | | | | H38 | FMC_LPC_LA32_N | LVDS | Y30 |
| | | | | H40 | VADJ_1V8 | | |

Notes:

1. U30 MAX15301 VADJ_1V8_FPGA voltage regulator power good output signal.
2. Connected to the XCKU040 U1 LS pins J25/J24 IIC_MAIN_SDA/SCL via I2C MUX U80 and level-shifter U77.
3. XCKU040 U1 JTAG TCK, TMS, TDO pins AC9, W9, U9 buffered by U19 SN74AVC8T245.
4. J2 LPC TDO-TDI connections to U27 LPC FMC JTAG bypass switch (N.C. normally closes/bypassing J2 until an FMC card is plugged into J2).
5. J2 LPC FMC connector TDO is level-shifted by U55, and then connected to system controller U111 pin P9 and Digilent USB JTAG module U115 TDO pin 8 in parallel.
6. FMC_LPC_PRSENT_M2C_B is the LPC FMC JTAG bypass switch U27.4 OE control signal and is also connected to the XCKU040 U1 pin J26 via level-shifter U44.

KCU105 Board Power System

The KCU105 board hosts a Maxim PMBus based power system. Each individual Maxim MAX15301 or MAX15303 voltage regulator has a PMBus interface. Figure 1-34 shows the KCU105 board power system block diagram.



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Figure 1-34: KCU105 Board Power System Block Diagram

The KCU105 evaluation board uses power regulators and PMBus compliant PoL controllers from Maxim Integrated Circuits to supply the core and auxiliary voltages listed in [Table 1-25](#).

Table 1-25: Onboard Power System Devices

| Device Type | Ref. Des. | PMBus Addr. | Description | Power Rail Net Name | Power Rail Voltage | Schematic Page |
|-------------|-----------|-------------|--|---------------------|--------------------|----------------|
| MAX15301 | U29 | 0x0A | Maxim InTune digital POL controller | VCCINT_FPGA | 0.95V | 52 |
| MAX15303 | U10 | 0x0B | Maxim InTune digital POL controller | VCCAUX_FPGA | 1.80V | 53 |
| MAX15303 | U3 | 0x0F | Maxim InTune digital POL controller | VCCBRAM_FPGA | 0.95V | 54 |
| MAX15303 | U9 | 0x11 | Maxim InTune digital POL controller | VCC1V8_FPGA | 1.80V | 55 |
| MAX15301 | U30 | 0x12 | Maxim InTune digital POL controller | VADJ_1V8_FPGA | 1.80V | 56 |
| MAX15303 | U4 | 0x14 | Maxim InTune digital POL controller | VCC1V2_FPGA | 1.20V | 57 |
| MAX20751E | U137 | 0x72 | Multiphase master with smart slave VT1697SBFQX | MGTAVCC_FPGA | 1.00V | 58 |
| MAX20751E | U138 | 0x73 | Multiphase master with smart slave VT1697SBFQX | MGTAVTT_FPGA | 1.20V | 59 |
| MAX8869E | U134 | NA | Maxim adjustable LDO 1A | MGTVCCAUX | 1.80V | 60 |
| MAX15301 | U31 | 0x1B | Maxim InTune digital POL controller | UTIL_3V3 | 3.30V | 61 |
| MAX17502 | U82 | NA | Maxim synch. buck switcher 1A | SYS_5V0 | 5.00V | 62 |
| MAX15053 | U124 | NA | Maxim adj. synch. buck switcher 2A | SYS_1V0 | 1.00V | 63 |
| MAX15027 | U125 | NA | Maxim adjustable LDO 1A | SYS_1V8 | 1.80V | 63 |
| MAX15027 | U126 | NA | Maxim adjustable LDO 1A | SYS_2V5 | 2.50V | 63 |
| TPS51200 | U24 | NA | TI source-sink Vtt regulator 3A | DDR4_VTT | 0.60V | 64 |

The Maxim GUI regulator on/off settings are shown in [Table 1-26](#).

Table 1-26: Maxim Power Tool GUI Regulator Settings

| Maxim Power Tool (1.08.02) PMBus Regulator Settings | | | | | | | Schematic Reference | | | |
|---|---------------|--------------------|--------------------|-------------------|---------------------|--------------------|---------------------|-----------|--------------------|-------------|
| Regulator Type | PMBus Address | Vout Set Point (V) | On Delay Time (ms) | On Rise Time (ms) | Off Delay Time (ms) | Off Fall Time (ms) | Current (A) | Ref. Des. | Schematic Net Name | Page Number |
| MAX15301 | 0x0A | 0.950 | 4.98 | 2.02 | 25.00 | 2.02 | 40 | U29 | VCCINT_FPGA | 52 |
| MAX15303 | 0x0B | 1.800 | 11.81 | 2.34 | 14.78 | 2.34 | 5 | U10 | VCCAUX_FPGA | 53 |
| MAX15303 | 0x0F | 0.950 | 7.84 | 2.02 | 19.94 | 2.02 | 5 | U3 | VCCBRAM_FPGA | 54 |
| MAX15303 | 0x11 | 1.800 | 19.78 | 2.33 | 7.97 | 2.33 | 2 | U9 | VCC1V8_FPGA | 55 |
| MAX15301 | 0x12 | 1.800 | 24.84 | 2.34 | 5.11 | 2.34 | 10 | U30 | VADJ_1V8_FPGA | 56 |
| MAX15303 | 0x14 | 1.200 | 24.88 | 1.89 | 5.12 | 1.89 | 3 | U4 | VCC1V2_FPGA | 57 |
| MAX15301 | 0x1B | 3.300 | 1.00 | 2.12 | 30.13 | 2.12 | 10 | U31 | UTIL_3V3 | 61 |
| MAX20751E | 0x72 | 1.000 | 10.00 | Not Supported | 20.00 | Not Supported | 5 | U137 | MGTAVCC_FPGA | 58 |
| MAX20751E | 0x73 | 1.200 | 14.00 | Not Supported | 14 | Not Supported | 5 | U138 | MGTAVTT_FPGA | 59 |

Documentation describing PMBUS programming for the Maxim InTune™ power controllers is available at the Maxim Integrated website [\[Ref 29\]](#).

The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [\[Ref 3\]](#).

FMC VADJ_1V8 Power Rail

The KCU105 evaluation board implements the ANSI/VITA 57.1 section 5.5.1 IPMI support functionality. The power control of the VADJ_1V8 power rail is significantly different from other Xilinx evaluation boards, and is managed by the U111 system controller. This rail powers both the FMC HPC (J22) and FMC LPC (J2) VADJ pins, as well as the XCKU040 HP banks 47, 48, 66, 67, and 68 (see [Table 1-3](#)). The valid values of the VADJ_1V8 rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is connected to each interface.

- If no cards are attached to the FMC ports, the VADJ voltage is set to 1.8V.
- When one FMC card is attached, its I2C EEPROM is read to find a VADJ voltage supported by both the KCU105 board and the FMC module within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- When two FMC cards are attached with differing VADJ requirements, VADJ_1V8 is set to the lowest value compatible with the KCU105 board and the FMC modules, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- If no valid information is found in the I2C EEPROM, the VADJ_1V8 rail is set to 0.0V.

The system controller user interface (see [FMC Menu Options in Appendix C](#)) allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_1V8_FPGA rail.

Monitoring Voltage and Current

Voltage and current monitoring and control for the Maxim power system is available through either the KCU105 system controller or via the Maxim PowerTool™ software graphical user interface.

The KCU105 system controller is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in [Table 1-25](#). For details on how to use this built-in feature see [PMBus Menu](#) and [SYSMON Menu](#) in [Appendix C, System Controller](#).

The Maxim InTune power controllers listed in [Table 1-25](#) can also be accessed through the PMBus connector J39. Using this connector requires the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL002#). This cable can be ordered from the Maxim Integrated website [\[Ref 29\]](#). The associated Maxim PowerTool GUI is also downloadable from the Maxim website.

SYSMON Power System Measurement

UltraScale FPGAs provide an analog converter (SYSMON) block. The SYSMON block contains a single 10-bit 0.2 MSPS ADC. The KCU105 board SYSMON ADC interface includes current measuring capability for all FPGA voltage rails. The rail current measurements are made available to SYSMON via an Analog Devices ADG707BRU multiplexer U75. Each rail has a TI INA333 op amp strapped across a series current sense resistors' Kelvin terminals. This op amp has its gain adjusted to give 0.75V - 1V at the expected full scale current value for the rail.

The SYSMON block can measure the internal VCCINT, VCCAUX, and VCCBRAM rail voltages and the external MGTAVCC and MGTAVTT rail voltages using SYSMON channels AD0 and AD8, respectively.

Figure 1-35 shows the SYSMON external multiplexer U75 circuit block diagram.

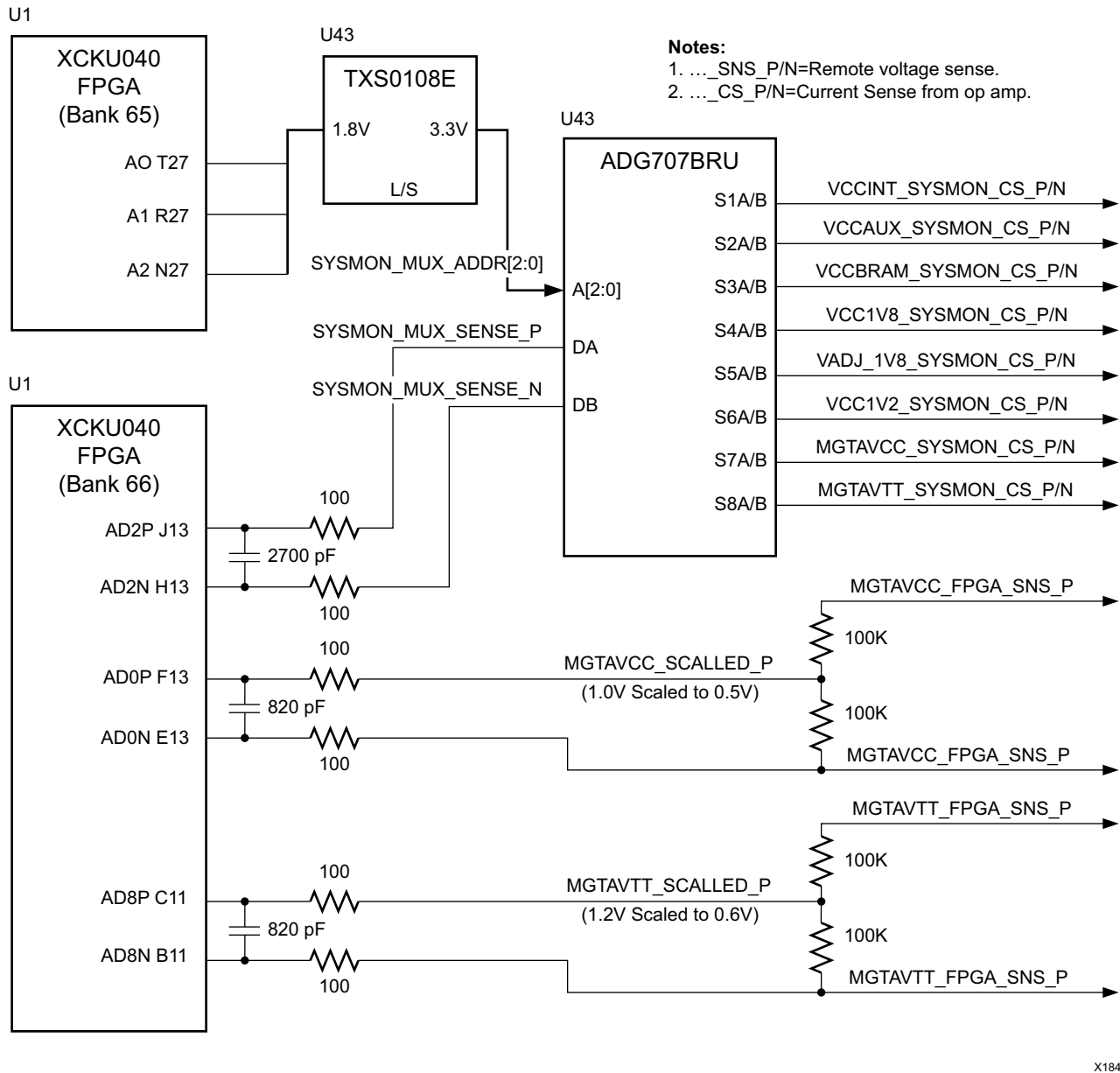


Figure 1-35: SYSMON External Multiplexer Block Diagram

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Table 1-27 lists the KCU105 board SYSMON power system voltage and current measurement details for the external U75 MUX.

Table 1-27: SYSMON Measurements Through MUX U75

| Controlled Rail Name | Ref. Des. | Meas. Type | Nom. Vout | Current Range | Isense Op Amp | | | Schematic Net Name | 8-to-1 Mux. U75 | | |
|----------------------|-----------|------------|-----------|---------------|---------------|------|----------------------|---------------------------|-----------------|----------|--------|
| | | | | | Ref. Des. | Gain | Vo Range | | Pin Num. | Pin Name | A[2:0] |
| VCCINT_FPGA | U29 | V | 0.95V | NA | NA | | | (SYSMON or MAXIM GUI) | NA | | |
| | | I | NA | 0-40A | U74 | 12.5 | 0 - 1V | VCCINT_SYSMON_CS_P | 19 | S1A | 000 |
| | | | | | | | VCCINT_SYSMON_CS_N | 11 | S1B | | |
| VCCAUX_FPGA | U10 | V | 1.80V | NA | NA | | | (SYSMON or MAXIM GUI) | NA | | |
| | | I | NA | 0 - 5A | U73 | 38 | 0 - 1V | VCCAUX_SYSMON_CS_P | 20 | S2A | 001 |
| | | | | | | | VCCAUX_SYSMON_CS_N | 10 | S2B | | |
| VCCBRAM_FPGA | U3 | V | 0.95V | NA | NA | | | (SYSMON or MAXIM GUI) | NA | | |
| | | I | NA | 0 - 5A | U72 | 30 | 0 - 0.75V | VCCBRAM_SYSMON_CS_P | 21 | S3A | 010 |
| | | | | | | | VCCBRAM_SYSMON_CS_N | 9 | S3B | | |
| VCC1V8_FPGA | U9 | V | 1.80V | NA | NA | | | (MAXIM GUI ONLY) | NA | | |
| | | I | NA | 0 - 2A | U116 | 100 | 0 - 1V | VCC1V8_SYSMON_CS_P | 22 | S4A | 011 |
| | | | | | | | VCC1V8_SYSMON_CS_N | 8 | S4B | | |
| VADJ_1V8_FPGA | U30 | V | 1.80V | NA | NA | | | (MAXIM GUI ONLY) | NA | | |
| | | I | NA | 0 - 10A | U119 | 20 | 0 - 1V | VADJ_1V8_SYSMON_CS_P | 23 | S5A | 100 |
| | | | | | | | VADJ_1V8_SYSMON_CS_N | 7 | S5B | | |
| VCC1V2_FPGA | U4 | V | 1.20V | NA | NA | | | (MAXIM GUI ONLY) | NA | | |
| | | I | NA | 0 - 3A | U120 | 60 | 0 - 0.90V | VCC1V2_SYSMON_CS_P | 24 | S6A | 101 |
| | | | | | | | VCC1V2_SYSMON_CS_N | 6 | S6B | | |
| MGTAVCC_FPGA | U137 | V | 1.00V | NA | NA | | | (SYSMON AD0 or MAXIM GUI) | NA | | |
| | | I | NA | 0 - 5A | U118 | 30 | 0 - 0.75V | MGTAVCC_SYSMON_CS_P | 25 | S7A | 110 |
| | | | | | | | MGTAVCC_SYSMON_CS_N | 5 | S7B | | |
| MGTAVTT_FPGA | U138 | V | 1.20V | NA | NA | | | (SYSMON AD8 or MAXIM GUI) | NA | | |
| | | I | NA | 0 - 5A | U117 | 30 | 0 - 0.75V | MGTAVTT_SYSMON_CS_P | 26 | S8A | 111 |
| | | | | | | | MGTAVTT_SYSMON_CS_N | 4 | S8B | | |

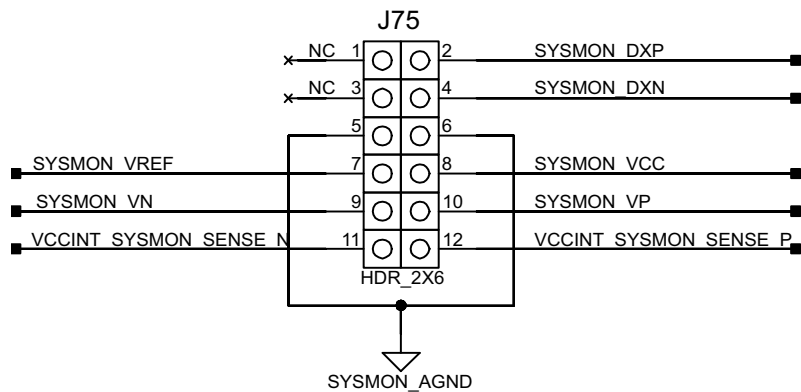
SYSMON Header J75

[Figure 1-2, callout 35]

UltraScale FPGAs provide an analog converter (SYSMON) block. The SYSMON contains a single 10-bit 0.2 MSPS ADC. Consequently, the sequencer for SYSMON does not support simultaneous sampling mode or independent ADC mode. See *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 30] for details on the capabilities of the analog

The KCU105 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the SYSMON. Internal measurements of the die temperature, VCCINT, VCCAUX, and VCCBRAM are available. Header J48 can be used to select either an external differential voltage reference (SYSMON_VREFP) or on-chip voltage reference (jumper J48 2-3) for the analog-to-digital converter.

For external measurements SYSMON header (J75) is provided. This header can be used to provide analog inputs to the FPGA's dedicated VP/VN input channel. The VCCINT_SYSMON_SENSE_P/N signals from the series current sense R86 0.002 Ω VCCINT resistor are also made available at J75. Figure 1-37 shows the header connections.



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Figure 1-37: SYSMON Header J75

Table 1-28 describes the SYSMON header J75 pin functions.

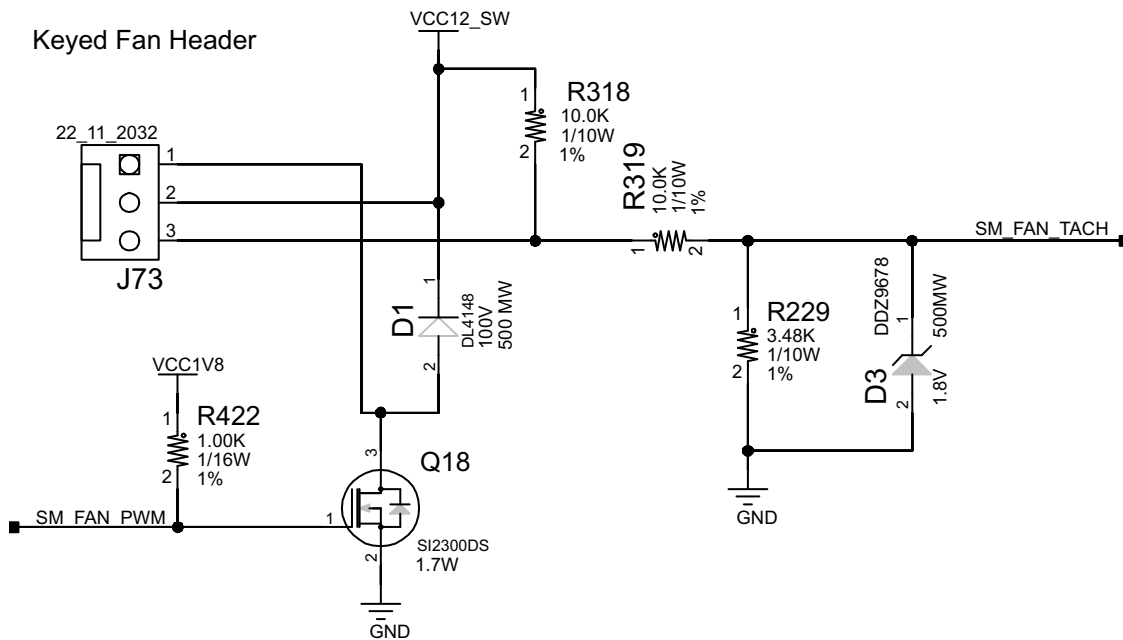
Table 1-28: SYSMON Header J75 Pinout

| Schematic Net Name | J75 Pin Number | Description |
|-------------------------|----------------|--|
| NC | 1,3 | No Connect |
| SYSMON_DXP, SYSMON_DXN | 2,4 | Access to thermal diode. |
| SYSMON_AGND | 5,6 | Analog ground reference. |
| SYSMON_VREF | 7 | REF3012 U40 1.25V. |
| SYSMON_VCC | 8 | Filtered VCC1V8 or ADP123 U14 1.85V. |
| SYSMON_VN, SYSMON_VP | 9,10 | Dedicated analog input channel for SYSMON. |
| VCCINT_SYSMON_SENSE_P/N | 11,12 | MAX15301 U29 VCCINT series 0.002 Ω R86 IR-drop taps. |

For more information on the UltraScale System Monitor (SYSMON), see *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 30].

Cooling Fan

The XCKU040 device U1 cooling fan connector is shown in [Figure 1-38](#). The fan turns on when the KCU105 board is powered up due to pull-up resistor R422. The SM_FAN_PWM and SM_FAN_TACH signals are wired to the XCKU040 device U1 bank 64 pins AJ9 and AJ8, respectively, which enables the user to implement their own fan speed control IP in the FPGA U1 logic.



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Figure 1-38: Cooling Fan Circuit

KCU105 Board Zynq-7000 SoC XC7Z010 System Controller

[[Figure 1-2](#), callout 36]

The KCU105 board Zynq-7000 SoC XC7Z010 system controller sub-system implements interfaces to:

- PMBus power system
- Programmable user clock
- USB UART2
- Five directional user pushbutton switches
- I2C bus MUXes

The system controller is delivered as a black-box design that communicates with onboard programmable devices over an I2C interface. The Zynq-7000 SoC system controller IP is not provided and is not available to end users for modification purposes.

The system controller is an ease-of-use feature that sets up or queries onboard resources available to the XCKU040 UltraScale FPGA U1 on the KCU105 board. Programmable clocks, the internal UltraScale FPGA system monitor block (SYSMON), and the Maxim power controllers are accessible through an I2C interface connected to both the system controller and the FPGA.

A Silicon Labs Si570 programmable low-jitter clock is used to provide a system clock for FPGA designers. Through a UART (115200-8-N-1) text interface, the system clock (Si570) can be set to any frequency between 10 MHz and 810 MHz. The Si570 defaults to a power-on frequency of 156.25 MHz, but then automatically changes to the last saved frequency setting requested by the user. Clock programming does not require FPGA resources and can be set or adjusted prior to configuring the FPGA or after the FPGA has been configured.

Additional functionality provided through the system controller's UART2 is a text display of the internal SYSMON registers for VCCINT, VCCBRAM, VCCAUX, and the UltraScale FPGA U1 device temperature. SYSMON based power measurements are also displayed over the UART2 for the VCCINT, VCCBRAM, VCCAUX, VCC1V8, VADJ_1V8, VCC1V2, MGTAVCC, and MGTAVTT power rails.

Power rail voltages set by the Maxim controllers are also displayed through the UART2 for VCCINT, VCCBRAM, VCCAUX, VCC1V8, VADJ_1V8, VCC1V2, MGTAVCC, MGTAVTT, MGTVCCAUX, and UTIL_3V3.

See [Appendix C, System Controller](#) for information on installing and using the system controller text-based UART menu.

Default Switch and Jumper Settings

The default switch and jumper settings for the KCU105 evaluation board are provided in this appendix.

Switches

The default switch settings are listed in [Table A-1](#). The KCU105 board switch locations are shown in [Figure 1-2](#).

Table A-1: Default Switch Settings

| Switch | Function | Default | Comments | Figure 1-2 Callout | Schematic 0381556 Page |
|--------|------------------------------|---------|----------------------------------|--------------------|------------------------|
| SW1 | SPST SLIDE SWITCH | OFF | BOARD SHIPPED WITH POWER SW. OFF | 30 | 51 |
| SW12 | 4-POLE GPIO DIP (1) | 0000 | POS. 1-4 GPIO ACTIVE HIGH | 26 | 41 |
| SW15 | 6-POLE CONFIGURATION DIP (1) | 00000 | POS. 1-5 ZYNQ SYSTEM CTRL. U111 | 28 | 32 |
| SW15 | 6-POLE CONFIGURATION DIP (1) | 0 | POS. 6 FPGA U1 MODE M2 | 28 | 32 |

Notes:

1. DIP switches are active-High (connected net is pulled High when DIP switch is closed).

Jumpers

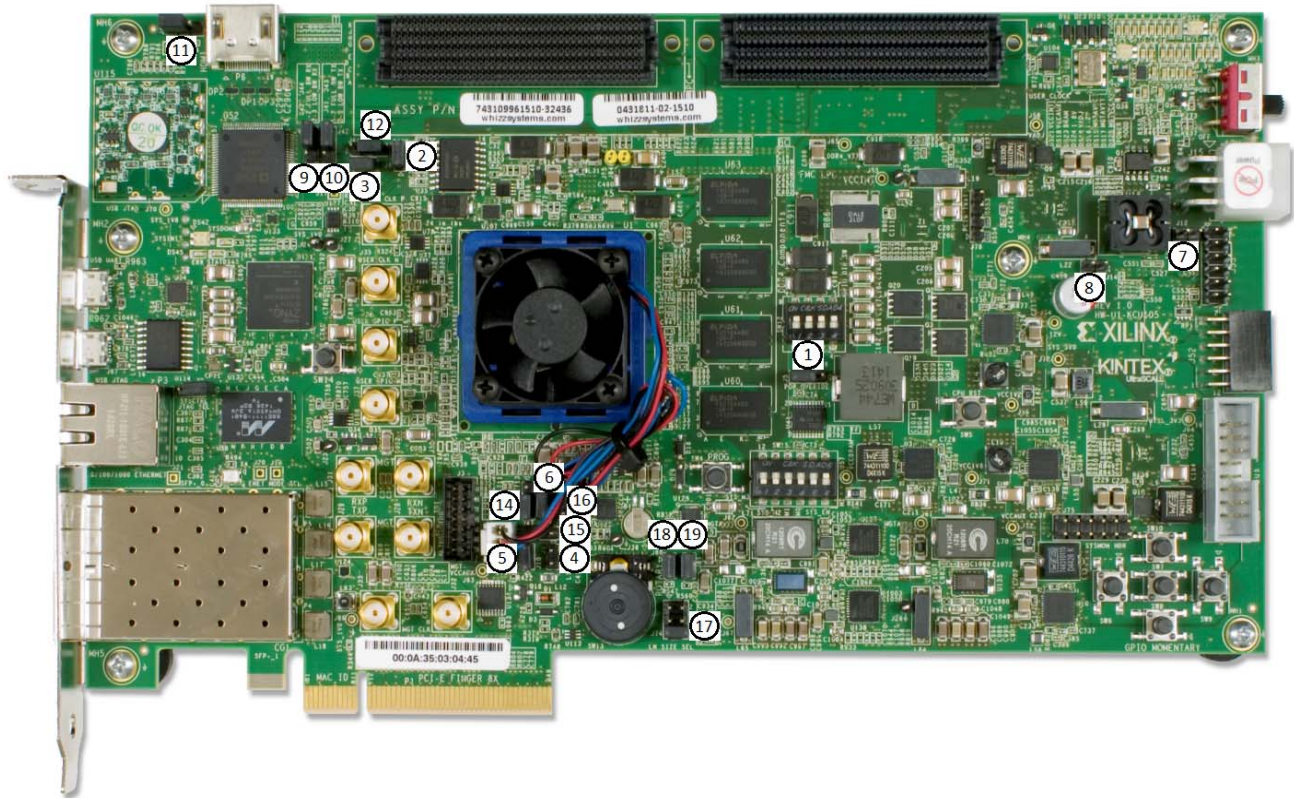
The default jumper settings are listed in [Table A-2](#). The KCU105 board jumper header locations are shown in [Figure A-1](#).

Table A-2: Default Jumper Settings

| Jumper | Function | Default | Comments | Figure A-1 Callout | Schematic 0381556 Page |
|--------|--------------------------------|---------|--|--------------------|------------------------|
| J5 | Power on reset override select | 2-3 | GND = EXTENDED POWER-ON DELAY | 1 | 3 |
| J6 | P5 SFP0 ENABLE | 1-2 | ENABLE SFP0 P5 CONNECTOR | 2 | 27 |
| J7 | P4 SFP1 ENABLE | 1 - 2 | ENABLE SFP1 P4 CONNECTOR | 3 | 28 |
| J9 | U40 1.25V VREF | OFF | AGND-TO-GND FILT. L14 BYPASS | 4 | 43 |
| J10 | U40 1.25V VREF | 1 - 2 | 1 - 2 = SYSMON_GND_FILT TO GND | 5 | 43 |
| J11 | SYSMON_VCC5V0 | OFF | 1 - 2 = SYSMON_VCC5V0 = FILT. SYS_5V0 | 6 | 43 |
| J12 | MAXIM REGULATOR INHIBIT | OFF | USED WHEN PROGRAMMING PWR. SYS. | 7 | 51 |
| J14 | U30 VADJ_1V8 ENABLE | OFF | ADDITIONAL TO J12 VADJ_1V8 ENABLE | 8 | 56 |
| J41 | P5 SFP0_RS1 | 2 - 3 | ENABLE LOW BANDWIDTH TX | 9 | 27 |
| J42 | P5 SFP0_RS0 | 2 - 3 | ENABLE LOW BANDWIDTH RX | 10 | 27 |
| J43 | P5 SFP1_RS1 | 2 - 3 | ENABLE LOW BANDWIDTH TX | 11 | 28 |
| J44 | P5 SFP1_RS0 | 2 - 3 | ENABLE LOW BANDWIDTH RX | 12 | 28 |
| J45 | U58 M88E1111 EPHY | 1 - 2 | SGMII TO CU, WITH CLOCK ⁽¹⁾ | 13 | 38 |
| J47 | SYSMON_VCC SELECT | 1 - 2 | SYSMON_VCC = FILTERED VCCAUX_FPGA | 14 | 43 |
| J48 | SYSMON_VREFP SELECT | 1 - 2 | SYSMON_VREFP = U40 1.25V VREF | 15 | 43 |
| J49 | U40 1.25V VREF Vin SELECT | 2 - 3 | U40 Vin = SYSMON_VCC | 16 | 43 |
| J74 | PCIe LANE SIZE SELECT | 5 - 6 | 8-LANE CONFIGURATION | 17 | 26 |
| J80 | SYSMON_VP | 1 - 2 | U1 VP pin V12 PULL DOWN 20.5K TO GND | 18 | 3 |
| J81 | SYSMON_VN | 1 - 2 | U1 VN pin W11 PULL DOWN 20.5K TO GND | 19 | 3 |

Notes:

1. In KCU105 board Rev. D and later, J45 is deleted, U58 CONFIG4 pin F9 is tied to GND to specify the SGMII to CU with clock functionality.



X18405-011117

Figure A-1: KCU105 Board Header Jumper Locations

VITA 57.1 FMC Connector Pinouts

Overview

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) low pin count (LPC) connector defined by the VITA 57.1 FMC specification. For a description of how the KCU105 evaluation board implements the FMC specification, see [FPGA Mezzanine Card Interface](#) and [FMC LPC Connector J2](#).

| | K | J | H | G | F | E | D | C | B | A |
|----|----|----|-------------|------------|----|----|---------------|-----------|----|----|
| 1 | NC | NC | VREF_A_M2C | GND | NC | NC | PG_C2M | GND | NC | NC |
| 2 | NC | NC | PRSN1_M2C_L | CLK1_M2C_P | NC | NC | GND | DP0_C2M_P | NC | NC |
| 3 | NC | NC | GND | CLK1_M2C_N | NC | NC | GND | DP0_C2M_N | NC | NC |
| 4 | NC | NC | CLK0_M2C_P | GND | NC | NC | GBTCLK0_M2C_P | GND | NC | NC |
| 5 | NC | NC | CLK0_M2C_N | GND | NC | NC | GBTCLK0_M2C_N | GND | NC | NC |
| 6 | NC | NC | GND | LA00_P_CC | NC | NC | GND | DP0_M2C_P | NC | NC |
| 7 | NC | NC | LA02_P | LA00_N_CC | NC | NC | GND | DP0_M2C_N | NC | NC |
| 8 | NC | NC | LA02_N | GND | NC | NC | LA01_P_CC | GND | NC | NC |
| 9 | NC | NC | GND | LA03_P | NC | NC | LA01_N_CC | GND | NC | NC |
| 10 | NC | NC | LA04_P | LA03_N | NC | NC | GND | LA06_P | NC | NC |
| 11 | NC | NC | LA04_N | GND | NC | NC | LA05_P | LA06_N | NC | NC |
| 12 | NC | NC | GND | LA08_P | NC | NC | LA05_N | GND | NC | NC |
| 13 | NC | NC | LA07_P | LA08_N | NC | NC | GND | GND | NC | NC |
| 14 | NC | NC | LA07_N | GND | NC | NC | LA09_P | LA10_P | NC | NC |
| 15 | NC | NC | GND | LA12_P | NC | NC | LA09_N | LA10_N | NC | NC |
| 16 | NC | NC | LA11_P | LA12_N | NC | NC | GND | GND | NC | NC |
| 17 | NC | NC | LA11_N | GND | NC | NC | LA13_P | GND | NC | NC |
| 18 | NC | NC | GND | LA16_P | NC | NC | LA13_N | LA14_P | NC | NC |
| 19 | NC | NC | LA15_P | LA16_N | NC | NC | GND | LA14_N | NC | NC |
| 20 | NC | NC | LA15_N | GND | NC | NC | LA17_P_CC | GND | NC | NC |
| 21 | NC | NC | GND | LA20_P | NC | NC | LA17_N_CC | GND | NC | NC |
| 22 | NC | NC | LA19_P | LA20_N | NC | NC | GND | LA18_P_CC | NC | NC |
| 23 | NC | NC | LA19_N | GND | NC | NC | LA23_P | LA18_N_CC | NC | NC |
| 24 | NC | NC | GND | LA22_P | NC | NC | LA23_N | GND | NC | NC |
| 25 | NC | NC | LA21_P | LA22_N | NC | NC | GND | GND | NC | NC |
| 26 | NC | NC | LA21_N | GND | NC | NC | LA26_P | LA27_P | NC | NC |
| 27 | NC | NC | GND | LA25_P | NC | NC | LA26_N | LA27_N | NC | NC |
| 28 | NC | NC | LA24_P | LA25_N | NC | NC | GND | GND | NC | NC |
| 29 | NC | NC | LA24_N | GND | NC | NC | TCK | GND | NC | NC |
| 30 | NC | NC | GND | LA29_P | NC | NC | TDI | SCL | NC | NC |
| 31 | NC | NC | LA28_P | LA29_N | NC | NC | TDO | SDA | NC | NC |
| 32 | NC | NC | LA28_N | GND | NC | NC | 3P3VAUX | GND | NC | NC |
| 33 | NC | NC | GND | LA31_P | NC | NC | TMS | GND | NC | NC |
| 34 | NC | NC | LA30_P | LA31_N | NC | NC | TRST_L | GA0 | NC | NC |
| 35 | NC | NC | LA30_N | GND | NC | NC | GA1 | 12P0V | NC | NC |
| 36 | NC | NC | GND | LA33_P | NC | NC | 3P3V | GND | NC | NC |
| 37 | NC | NC | LA32_P | LA33_N | NC | NC | GND | 12P0V | NC | NC |
| 38 | NC | NC | LA32_N | GND | NC | NC | 3P3V | GND | NC | NC |
| 39 | NC | NC | GND | VADJ | NC | NC | GND | 3P3V | NC | NC |
| 40 | NC | NC | VADJ | GND | NC | NC | 3P3V | GND | NC | NC |

X18406-113016

Figure B-1: FMC LPC Connector Pinout

Figure B-2 shows the pinout of the FMC high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the KCU105 evaluation board implements the FMC specification, see [FPGA Mezzanine Card Interface](#) and [FMC HPC Connector J22](#).

| | K | J | H | G | F | E | D | C | B | A |
|----|------------|------------|--------------|------------|-----------|-----------|---------------|-----------|---------------|-----------|
| 1 | VREF_B_M2C | GND | VREF_A_M2C | GND | PG_M2C | GND | PG_C2M | GND | RES1 | GND |
| 2 | GND | CLK3_M2C_P | PRSN_T_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_M2C_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_M2C_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C_P | GND | DP9_M2C_P | GND |
| 5 | CLK2_M2C_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C_N | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | GND | DP7_M2C_N | GND |
| 14 | HA10_N | GND | LA07_N | GND | HA12_N | GND | LA09_P | LA10_P | GND | DP4_M2C_P |
| 15 | GND | HA14_P | GND | LA12_P | GND | HA16_P | LA09_N | LA10_N | GND | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GND | DP6_M2C_P | GND |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | DP6_M2C_N | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | GND | DP5_M2C_P |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | DP5_M2C_N |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C_P | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C_N | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | GND | DP9_C2M_N | GND |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | GND | DP8_C2M_P | GND |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |

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Figure B-2: FMC HPC Connector Pinout

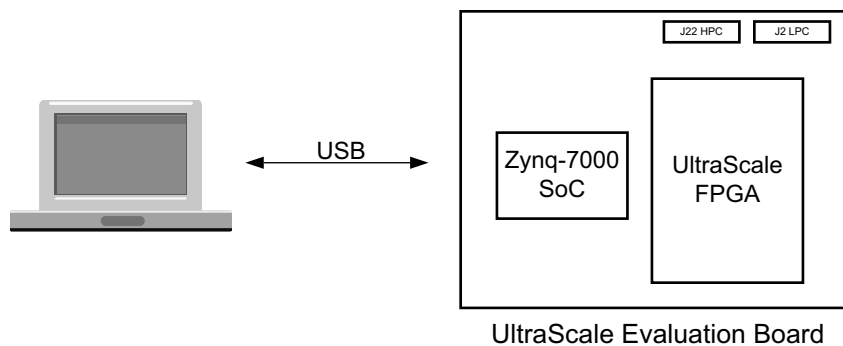
System Controller

Overview

The Xilinx system controller is an ease-of-use application that runs on a Zynq®-7000 SoC at power-up on all UltraScale™ device evaluation boards. These select board features can be controlled and monitored:

- Programmable clocks
- Power system monitoring (PMBus)
- UltraScale FPGA system monitor (SYSMON)
- Adjustable FMC expansion interface voltage
- GPIO pushbuttons and configuration DIP switch
- UltraScale FPGA Configuration

On power-up, the system controller presents a menu-driven selection of actions invoked by running a terminal program over a UART (115200-8-N-1) connection through the USB-to-UART bridge interface (J4).



X18408-050818

Figure C-1: PC Host (Terminal Window) and UltraScale Evaluation Board

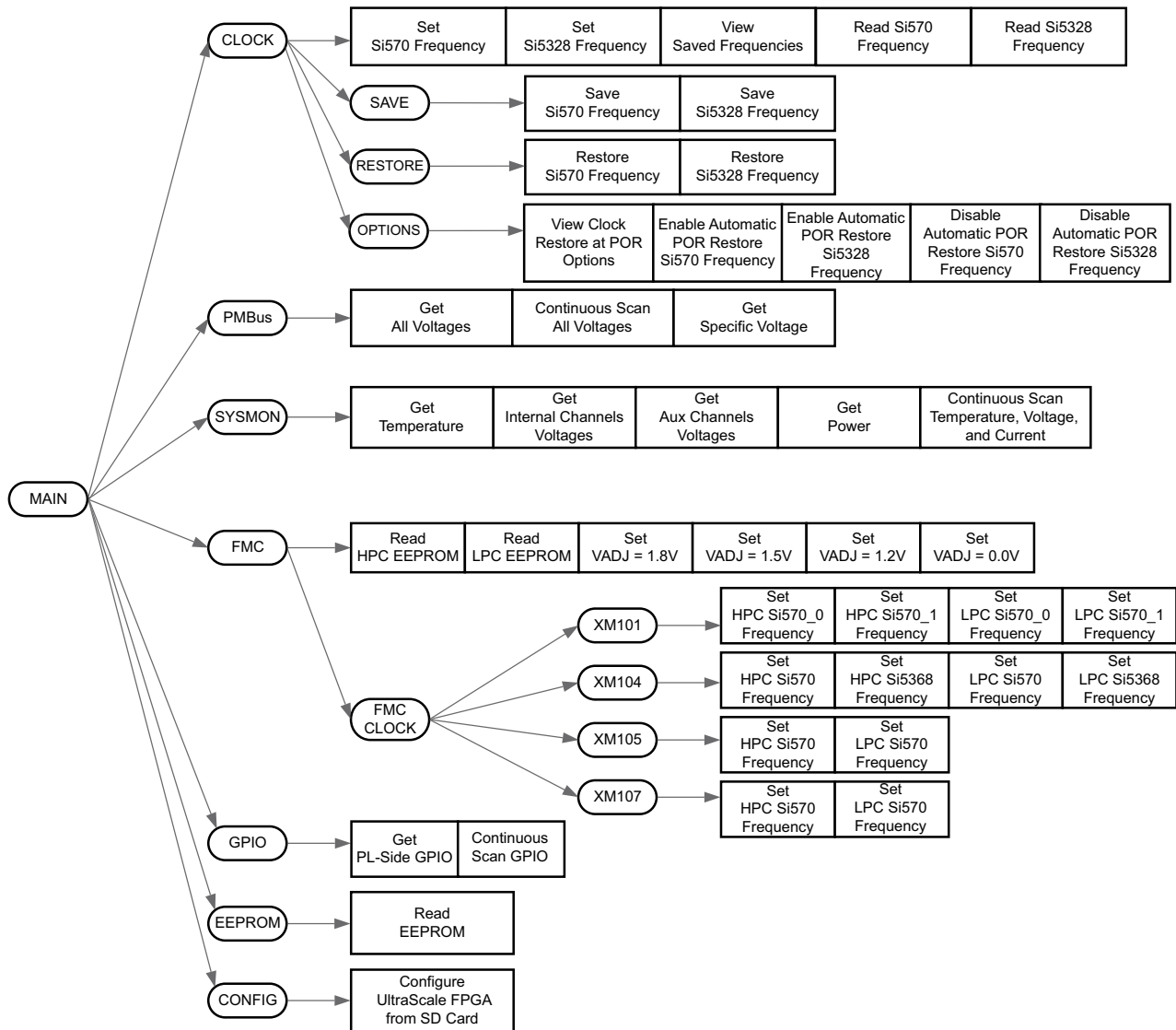
Access the system controller menu as follows:

1. Install the Silicon Labs CP2105GM dual USB-to-UART bridge driver by following the instructions in the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033) [Ref 31].
2. The Tera Term terminal application installation is referenced in the driver installation instructions in step 1, which point to the *Tera Term Terminal Emulator Installation Guide* (UG1036) [Ref 32].
3. With the KCU105 evaluation board power turned off, install the USB cable supplied in the KCU105 evaluation board kit (standard type-A end to host computer, type Micro-B end to KCU105 evaluation board connector J4).
4. Turn on the KCU105 evaluation board. The PC recognizes that new hardware is connected, and runs the driver installation wizard to complete the installation of the CP2015GM bridge chip drivers. The system controller UART appears in the PC device manager ports (COM & LPT) list as the Silicon Labs Dual CP210x Enhanced COM Port (COMnn).
5. Open a Tera Term terminal window on the PC desktop. In the New connection dialog box, click the serial radio button, and then click the drop-down arrow to open the list of ports. Select the COM port with the Enhanced description. Click OK.
6. At the top of the Tera Term VT window, select **Setup > Serial port**. In the dialog box that appears, set baud rate to 115200, data to 8 bit, parity to none, stop to 1 bit, and flow control to none. Click OK.
7. Power cycle the KCU105 evaluation board. The Tera Term window displays the KCU105 evaluation board system controller main menu.

The main menu lists seven sub-menus that carry out selected actions.

```
KCU105 System Controller
- Main Menu-
1. Set Programmable Clocks (see Clock Menu)
2. Get Power System (PMBus) Voltages (see PMBus Menu)
3. Get UltraScale FPGA System Monitor (SYSMON) Data (see SYSMON Menu)
4. Adjust FPGA Mezzanine Card (FMC) Settings (see FMC Menu)
5. Get GPIO Data (see GPIO Menu)
6. Get EEPROM Data (see EEPROM Menu)
7. Configure UltraScale FPGA (see CONFIG Menu)
Select an option
```

The menu system is shown in Figure C-2.



X18409-113016

Figure C-2: System Controller Menu System

Power-On and Reset

Prior to displaying the main menu, the system controller initializes the adjustable voltage (VADJ) on the FPGA FMC expansion port interface within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.

- If no cards are attached to the FMC ports, the VADJ voltage is set to 1.8V.
- When one FMC card is attached, its I2C EEPROM is read to find a VADJ voltage supported by both the KCU105 board and the FMC module within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- When two FMC cards are attached with differing VADJ requirements, VADJ is set to the lowest value compatible with the KCU105 board and the FMC modules, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.

The VADJ voltage is set and then the main menu is displayed. The VADJ settings can be viewed by scrolling back through the terminal window output.



IMPORTANT: *If an attached FMC card does not have its I2C EEPROM programmed, the firmware sets VADJ to 0.0V.*

The VADJ voltage can be set manually with the FMC menu.

KCU105 On-board Clocks

The KCU105 board hosts two programmable clocks. One is the user programmable system clock (Silicon Labs Si570) that operates in the frequency range between 10 MHz and 810 MHz. The second KCU105 programmable clock source is the Silicon Labs Si5328B, which is typically used as a jitter attenuator for a recovered clock from a serial transceiver. However, the Si5328B can also be used as an independent clock source with a frequency range of 8 kHz to 808 MHz. In addition to the programmable clock sources, the UltraScale FPGA evaluation boards provide a 300 MHz fixed frequency system clock.

Clock Menu

The clock menu is used to set the frequency of the onboard programmable clock sources. At KCU105 board power-up, the onboard programmable clock sources generate their factory default frequencies until the system controller has booted and checked the onboard EEPROM to determine if a frequency value has previously been saved for either onboard clock source. Previously saved values are restored to the onboard clock sources, which then output these frequencies until they are reprogrammed to a different value, or the KCU105 board is turned off.

A KCU105 board power cycle (power off/power on) returns the clock sources to the factory default settings. On the UltraScale FPGA evaluation boards, the factory default for the Si570 is 156.250 MHz, and the factory default for the Si5328 is 0 Hz.

The programmable clock frequencies of the KCU105 board can be set and saved for later restoration. The saved frequencies are maintained in the KCU105 board onboard non-volatile I2C EEPROM. The clock menu is used to manually restore previously saved clock frequencies.

This section includes a description of the clock menu options, presenting arbitrary sample value entries and the system controller responses. The entry value commentary is shown in parentheses.

```
KCU105 System Controller
- Clock Menu-
1. Set KCU105 Si570 User Clock Frequency
2. Set KCU105 Si5328 MGT Clock Frequency
3. Save KCU105 Clock Frequency to EEPROM
4. Restore KCU105 Clock Frequency from EEPROM
5. View KCU105 Saved Clocks in EEPROM
6. Set KCU105 Clock Restore Options
7. Read KCU105 Si570 User Clock Frequency
8. Read KCU105 Si5328 MGT Clock Frequency
0. Return to Main Menu
Select an option
```

Clock Menu Options

Option 1: Set KCU105 Si570 User Clock Frequency

```
Enter the Si570 frequency <10-810MHz>:
```

```
(enter a value between 10 and 810)
```

```
100
```

```
RFreq_Cal [0]=0x02,RFreq_Cal [1]=0xBC,RFreq_Cal [2]=0x00,RFreq_Cal [3]=0xE4,
RFreq_Cal [4]=0xED
```

```
Freq: 100.0000000000 HS_DIV=5 N1=10 DCO=5000.0 RFREQ= 0x02BC00E4ED
```

(The returned values include configuration setting details.)

Option 2: Set KCU105 Si5328 MGT Clock Frequency

Enter the Si5328 frequency (0.008-808MHz):

200



IMPORTANT: *Several seconds might elapse before the result is returned.*

```
Freq:200.0000000000 fosc=5600.000MHz f3=5.000KHz LBW=0.200KHz N1=28 N1_HS=7
NC1_LS=4 N2=1120000 N2_HS=4 N2_LS=280000 N31=40000 N32=22857
```

(The returned values include configuration setting details.)

Option 3: Save KCU105 Clock Frequency to EEPROM

KCU105 System Controller

- Save Menu -

1. Save KCU105 Si570 Frequency to EEPROM
2. Save KCU105 Si5328 Frequency to EEPROM
0. Return to Clock Menu

Select an option

- Save KCU105 Si570 Frequency to EEPROM
Saving Si570 Frequency = 200.000 to EEPROM
- Save KCU105 Si5328 Frequency to EEPROM
Saving Si5328 Frequency = 150.000 to EEPROM
- Return to Clock Menu

This option returns to the menu level above.

Option 4: Restore KCU105 Clock Frequency from EEPROM

If either clock device is reprogrammed and the frequency value is not saved, the previously saved frequency can be restored to the clock source.

KCU105 System Controller

- Restore Menu -

1. Restore KCU105 Si570 Frequency from EEPROM
2. Restore KCU105 Si5328 Frequency from EEPROM
0. Return to Clock Menu

Select an option

- Restore KCU105 Si570 Frequency from EEPROM

```
Freq:200.0000000000 HS_DIV=7 N1=4 DCO=5600.0 RFREQ=0x030FFF204B
Restored Si570 Frequency = 200.000 from EEPROM
```

(The returned values include configuration setting details.)

- Restore KCU105 Si5328 Frequency from EEPROM

```
Restoring Si5328 Frequency = 150.000 from EEPROM
Freq:150.0000000000 fosc=5400.000MHz f3=15.000KHz LBW=0.600KHz N1=36 N1_HS=6
NC1_LS=6 N2=360000 N2_HS=4 N2_LS=90000 N31=10000 N32=7619
```

(The returned values include configuration setting details.)

- Return to Clock Menu

This option returns to the menu level above.

Option 5: View KCU105 Saved Clocks in EEPROM

This option is for verifying that the recently programmed values are in EEPROM.

```
Saved Clocks in EEPROM
-----
Si570 User Clock: 200.00000000 MHz
Si5328 MGT Clock: 150.00000000 MHz
```

Option 6: View KCU105 Clocks Restore Options

```
KCU105 System Controller
- Options Menu-
-----
1. View KCU105 Clock Restore Options
2. Enable KCU105 Si570 Automatic Restore at Power-Up Reset
3. Enable KCU105 Si5328 Automatic Restore at Power-Up Reset
4. Disable KCU105 Si570 Automatic Restore at Power-Up Reset
5. Disable KCU105 Si5328 Automatic Restore at Power-Up Reset
0. Return to Clock Menu
Select an option
```

- View KCU105 Clock Restore Options

```
Clock Restore Options:
-----
Si570 Automatic Restore at Power-Up Reset = DISABLED
Si5328 Automatic Restore at Power-Up Reset = DISABLED
```

- Enable KCU105 Si570 Automatic Restore at Power-Up Reset

There is no menu response to selecting this option. To verify that the enabling function occurred, select option 1 again.

- Enable KCU105 Si5328 Automatic Restore at Power-Up Reset

There is no menu response to selecting this option. To verify that the enabling function occurred, select option 1 again.

- View KCU105 Clock Restore Options

Clock Restore Options:

```
-----
Si570 Automatic Restore at Power-Up Reset = ENABLED
Si5328 Automatic Restore at Power-Up Reset = ENABLED
```

- Return to Clock Menu

This option returns to the menu level above.

Option 7: Read KCU105 Si570 User Clock Frequency

This option displays the current frequency setting of the Si570.

```
Si570 Current Frequency = 1.562500E+02 MHz
```

Option 8: Read KCU105 Si5328 MGT Clock Frequency

This option displays the current frequency setting of the Si5328.

```
Si5328 CKOUT1 Current Frequency = 2.000000E+02 MHz
Si5328 CKOUT1 Current Frequency = 2.000000E+02 MHz
```

- Return to Main Menu

This option returns to the menu level above.

PMBus Menu

The PMBus is an I2C bus that is used to read the voltage settings of the nine KCU105 power rails controlled by the Maxim power system. Through the PMBus menu these power rails can be read once or scanned continuously until stopped by a key press. [Table C-1](#) lists the voltage rails accessible through the system controller's interface to the Maxim PMBus.

Table C-1: Maxim Power Supply Rail

| Maxim Power Supply Rail | I2C Address | Nominal Voltage |
|-------------------------|-------------|-----------------|
| VCCINT | 0x0A | 0.95V |
| VCCBRAM | 0x0F | 0.95V |
| VCCAUX and VCCAUX_IO | 0x0B | 1.80V |
| VCC1V8 | 0x11 | 1.80V |
| VADJ_1V8 | 0x12 | 1.80V |
| VCC1V2 | 0x14 | 1.20V |
| MGTAVCC | 0x72 | 1.00V |
| MGTAVTT | 0x73 | 1.20V |
| UTIL_3V3 | 0x1B | 3.30V |

PMBus Menu Options

```

KCU105 System Controller
- PMBus Menu-
1. Get PMBus Voltages
2. Continuous Scan PMBUS Voltages
3. Get VCCINT Voltage
4. Get VCCAUX Voltage
5. Get VCCBRAM Voltage
6. Get VCC1V8 Voltage
7. Get VADJ1V8 Voltage
8. Get VCC1V2 Voltage
9. Get MGTAVCC Voltage
A. Get MGTAVTT Voltage
B. Get UTIL3V3 Voltage
0. Return to Main Menu
Select an option
    
```

Option 1: Get PMBus Voltages

```

VCCINT    = 0.950 V
VCCAUX    = 1.800 V
    
```

```

VCCBRAM    = 0.950 V
VCC1V8     = 1.800 V
VADJ1V8    = 1.800 V
VCC1V2     = 1.200 V
MGTAVCC    = 1.000 V
MGTAVTT    = 1.200 V
UTIL3V3    = 3.297 V
  
```

Option 2: Continuous Scan PMBUS Voltages

The list of voltages shown in option 1 is displayed and updated about once per second. Pressing any key re-displays the PMBus menu.

Option 3: Get VCCINT Voltage

```

VCCINT = 0.950 V (one-time snapshot of the VCCINT voltage)
Unscaled Hex: MSB = 0x0F, LSB = 0x34
  
```

(The returned values include configuration setting details.)

Option 4: Get VCCAUX Voltage

```

VCCAUX = 1.800 V
Unscaled Hex: MSB = 0x1C, LSB = 0xCC
  
```

(The returned values include configuration setting details.)

Option 5: Get VCCBRAM Voltage

```

VCCBRAM = 0.950 V
Unscaled Hex: MSB = 0x0F, LSB = 0x33
  
```

(The returned values include configuration setting details.)

Option 6: Get VCC1V8 Voltage

```

VCC1V8 = 1.800 V
Unscaled Hex: MSB = 0x1C, LSB = 0xCC
  
```

(The returned values include configuration setting details.)

Option 7: Get VADJ1V8 Voltage

```

VADJ1V8 = 1.800 V
Unscaled Hex: MSB = 0x1C, LSB = 0xCB
  
```

(The returned values include configuration setting details.)

Option 8: Get VCC1V2 Voltage

VCC1V2 = 1.200 V

Unscaled Hex: MSB = 0x13, LSB = 0x33

(The returned values include configuration setting details.)

Option 9: Get MGTAVCC Voltage

MGTAVCC = 1.000 V

Unscaled Hex: MSB = 0x10, LSB = 0x00

(The returned values include configuration setting details.)

Option A: Get MGTAVTT Voltage

MGTAVTT = 1.200 V

Unscaled Hex: MSB = 0x13, LSB = 0x32

(The returned values include configuration setting details.)

Option B: Get UTIL3V3 Voltage

UTIL3V3 = 3.299 V

Unscaled Hex: MSB = 0x34, LSB = 0xC7

(The returned values include configuration setting details.)

Option 0: Return to Main Menu

This option returns to the menu level above.

SYSMON Menu

The Kintex UltraScale FPGA on the KCU105 contains a 200 KSPS analog-to-digital converter known as the system monitor (SYSMON), which is described in *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 30]. Measurements made internal to the UltraScale FPGA are accomplished by the SYSMON block for VCCINT, VCCBRAM, and VCCAUX. In conjunction with an onboard analog multiplexer (Analog Devices ADG707) and inline Kelvin sense resistors, the UltraScale SYSMON ADC measures the current on the eight rails listed in [Table C-2](#).

Table C-2: SYSMON Monitored Power Rail

| SYSMON Monitored Power Rail | Nominal Voltage | Maximum Rail Current |
|-----------------------------|-----------------|----------------------|
| VCCINT | 0.95V | 40A |
| VCCAUX and VCCAUX_IO | 1.80V | 5A |
| VCCBRAM | 0.95V | 5A |
| VCC1V8 | 1.80V | 2A |
| VADJ_1V8 | 1.80V | 10A |
| VCC1V2 | 1.20V | 3A |
| MGTAVCC | 1.00V | 5A |
| MGTAVTT | 1.20V | 5A |

The system controller reads and displays SYSMON based measurements prior to configuring the UltraScale FPGA. Bank 66 of the Kintex UltraScale device is the default SYSMON bank and is ready to monitor the SYSMON auxiliary channels at power-up. Auxiliary channels VAUX0, VAUX2, and VAUX8 are used to monitor MGTVCC, the ADG707 analog MUX, and MGTAVTT, respectively. At power-up, jumpers J80 and J81 connect SYSMON's VP and VN pins to ground, setting the default SYSMON I2C address to 0x32. This power-up default I2C address is used by the system controller to access SYSMON data.

If the KCU105 system controller SYSMON menu is used after the UltraScale FPGA has been configured with a design, the UltraScale resident design must contain logic to enable I2C access to the UltraScale system monitor and the internal (VCCINT, VCCBRAM, VCCAUX) and auxiliary channels (VAUX0, VAUX2, VAUX8). Designs that access I2C devices through the TCA9548 I2C switch must also deassert the TCA9548 reset pin from logic within the UltraScale FPGA. There is an external pull-up on this reset signal. See *UltraScale Architecture System Monitor User Guide (UG580)* [Ref 30] for more details.

Through the SYSMON menu, single readings or a continuous scan of the voltages, currents, power, and temperature are available. The minimum and maximum current usage for the monitored rails are also displayed and are reset each time the SYSMON menu is entered.

SYSMON Menu Options

```

KCU105 System Controller
- SYSMON Menu-
1. Get Temperature
2. Get Internal Channel Voltages
3. Get Auxiliary Channel Voltages
4. Get Power
5. Continuous Scan SYSMON Measurements
0. Return to Main Menu
Select an option
    
```

Option 1: Get Temperature

Temperature = 33.31 C Min = 30.65 C Max = 33.54 C

Option 2: Get Internal Channel Voltages

```
VCCINT  =  0.955 V Max = 0.956 V Min = 0.946 V
VCCBRAM =  0.954 V Max  = 0.954 V Min = 0.945 V
VCCAUX  =  1.804 V Max = 1.805 V Min = 1.796 V
-----
VPVN    =  0.003 V
VREFP   =  1.257 V
VREFN   =  0.012 V
```

Option 3: Get Auxiliary Channel Voltages

```
VAUX_0 = 0.503 V
VAUX_2 = 0.005 V
VAUX_8 = 0.603 V
```

Option 4: Get Power

```
-----
VCCINT  POWER = 0.147 W
VCCBRAM POWER = 0.039 W
VCCAUX  POWER = 0.419 W
VCC1V8  POWER = 0.015 W
VADJ1V8 POWER = 0.089 W
VCC1V2  POWER = 0.068 W
MGTAVCC POWER = 0.078 W
MGTAVTT POWER = 0.035 W
-----
```

Option 5: Continuous Scan SYSMON Measurements

Press Any Key to Return to SYSMON Menu

Temperature = 33.03 C Min = 30.51 C Max = 33.81 C

```
-----
                                     MIN      MAX
                                     Current  Current
Power      Voltage  Current  Current  Current
VCCINT:    0.30 W   0.95 V   0.31 A   0.15 A   0.37 A
VCCAUX:    0.41 W   1.80 V   0.23 A   0.22 A   0.24 A
VCCBRAM:   0.03 W   0.95 V   0.03 A   0.03 A   0.05 A
VCC1V8:    0.02 W   1.80 V   0.01 A   0.01 A   0.01 A
VADJ_1V8:  0.06 W   1.80 V   0.03 A   0.02 A   0.06 A
```

| | | | | | |
|----------|--------|--------|--------|--------|--------|
| VCC1V2: | 0.07 W | 1.20 V | 0.06 A | 0.05 A | 0.06 A |
| MGTAVCC: | 0.08 W | 1.00 V | 0.08 A | 0.07 A | 0.09 A |
| MGTAVTT: | 0.03 W | 1.20 V | 0.03 A | 0.02 A | 0.03 A |

Option 0: Return to Main Menu

This option returns to the menu level above.

FMC Menu

The KCU105 board provides two FMC ANSI/VITA 57.1 expansion interfaces that use a common VADJ voltage supply. At power-up, prior to displaying the main menu, the system controller initializes the VADJ on the FMC expansion port interface. If no cards are attached to the FMC ports, the VADJ voltage is set to 1.8V. Otherwise, the FMC module's I2C EEPROM is read to find a VADJ voltage supported by both the KCU105 board and the FMC module within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V. The VADJ voltage is set and then the main menu is displayed. Users can scroll back through their terminal window output and view the settings determined for VADJ. If an attached FMC card does not have its I2C EEPROM programmed, the VADJ voltage can be set manually with the FMC menu.

All FMC mezzanine cards must host an I2C EEPROM, powered from the always on 3P3VAUX rail, which can be read out through the FMC menu. A raw hexadecimal display and a formatted version of the FMC EEPROM data are provided through the FMC menu. The VITA 57.1 standard identifies the data fields of the intelligent platform management interface (IPMI) specification used for the FMC EEPROM. The KCU105 board system controller utilizes the board information area and the multi-record DC load record to query the FMC module for its VADJ requirements. See the VITA FMC Marketing Alliance website [\[Ref 28\]](#) for details on these standards. The KCU105 board system controller is aware of the programmable clock resources on these FMCs:

- FMC XM101 LVDS QSE card
- FMC XM104 MGT serial connectivity card
- FMC XM105 debug card
- FMC XM107 loopback card

These mezzanine cards can be attached to the J22 HPC or J2 LPC expansion ports on the KCU105 board. [Table C-3](#) shows the accessible clock resources on each FMC module.

Table C-3: FMC Module/Board

| Xilinx FMC Module/Board | Clock Source #1 | Clock Source #2 |
|-------------------------|-----------------|-----------------|
| XM101 | Si570 | Si570 |
| XM104 | Si570 | Si5638 |
| XM105 | Si570 | n/a |
| XM107 | Si570 | n/a |
| KCU105 Base Board | Si570 | Si5328 |

FMC Menu Options

```

KCU105 System Controller
- FMC Menu-
1. Set FMC XMxxx CLOCKS
2. Read FMC HPC IIC EEPROM
3. Read FMC LPC IIC EEPROM
4. Set FMC VADJ to 1.8V
5. Set FMC VADJ to 1.5V
6. Set FMC VADJ to 1.2V
7. Set FMC VADJ to 0.0V
0. Return to Main Menu
Select an option
    
```

Identify the FMC module types plugged on to the KCU105 board, and which FMC connector is associated - the left J22 HPC or right J2 LPC. The examples shown in this section reflect the particular FMC installed at the KCU105 board J22 HPC FMC connector.

Option 1: Set FMC XMxxx CLOCKS

```

KCU105 System Controller
  - FMC Clock Menu -
-----
1. Set FMC XM101 Clocks
2. Set FMC XM104 Clocks
3. Set FMC XM105 Clocks
4. Set FMC XM107 Clocks
0. Return to FMC Menu
Select an option
    
```

Set FMC XM101 Clocks

```

KCU105 System Controller
  - XM101 Menu -
-----
1. Set HPC Si570_0 Frequency
2. Set HPC Si570_1 Frequency
3. Set LPC Si570_0 Frequency
4. Set LPC Si570_1 Frequency
0. Return to FMC Clock Menu
Select an option
    
```

- Set HPC Si570_0 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```

board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer [i] = 58
ReadBuffer [i+1] = 4D
ReadBuffer [i+2] = 31
ReadBuffer [i+3] = 30
ReadBuffer [i+4] = 31
Enter the Si570 frequency (10-810MHz):
50
Freq:50.000000000 HS_DIV=7 N1=14 DCO=4900.0 RFREQ=0x02AE100C27
    
```

(The returned values include configuration setting details.)

- Set HPC Si570_1 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 31
Enter the Si570 frequency (10-810MHz):
100
Freq:100.0000000000 HS_DIV=5 N1=10 DCO=5000.0 RFREQ=0x02BC48225C
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

This option returns to the menu level above.

Set FMC XM104 Clocks

```
KCU105 System Controller
  - XM104 Menu -
-----
1. Set HPC Si570   Frequency
2. Set HPC Si5368 Frequency
3. Set LPC Si570   Frequency
4. Set LPC Si5368 Frequency
0. Return to FMC Clock Menu
Select an option
```

- Set HPC Si570 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
```

```

board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer [i] = 58
ReadBuffer [i+1] = 4D
ReadBuffer [i+2] = 31
ReadBuffer [i+3] = 30
ReadBuffer [i+4] = 34
Enter the Si570 frequency (10-810MHz):
125
Freq:125.0000000000 HS_DIV=4 N1=10 DCO=5000.0 RFREQ=0x02BBEE4A63
    
```

(The returned values include configuration setting details.)

- Set HPC Si5368 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```

board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer [i] = 58
ReadBuffer [i+1] = 4D
ReadBuffer [i+2] = 31
ReadBuffer [i+3] = 30
ReadBuffer [i+4] = 34
Enter the Si5368 output frequency (0.002-808MHz):
205
    
```



IMPORTANT: *Several seconds may elapse before the result is returned.*

```

Freq:205.0000000000 fosc=4920.000MHz f3= 5.000KHz LBW=0.200KHz N1=24 N1_HS=6
NC1_LS=4 N2=984000 N2_HS=4 N2_LS=246000 N31=41000 N32=22857
    
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

This option returns to the menu level above.

Set FMC XM105 Clocks

```

KCU105 System Controller
  - XM105 Menu -
-----
1. Set HPC Si570   Frequency
2. Set LPC Si570   Frequency
0. Return to FMC Clock Menu
Select an option
    
```

- Set HPC Si570 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```

board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 35
Enter the Si570 frequency (10-810MHz):
50
Freq:50.0000000000 HS_DIV=7 N1=14 DCO=4900.0 RFREQ=0x02AE1505E5
    
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

This option returns to the menu level above.

Set FMC XM107 Clocks

```

KCU105 System Controller
  - XM107 Menu -
-----
1. Set HPC Si570   Frequency
2. Set LPC Si570   Frequency
0. Return to FMC Clock Menu
Select an option
    
```

- Set HPC Si570 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```

board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 37
Enter the Si570 frequency (10-810MHz):
230
Freq:230.0000000000 HS_DIV=11 N1=2 DCO=5060.0 RFREQ=0x02C44FF69F
    
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

This option returns to the menu level above.

Return to FMC Menu

This option returns to the menu level above.

Option 2: Read FMC HPC IIC EEPROM

```
FMC HPC card present
```

The I2C EEPROM data displayed is too long to include in this appendix. If the FMC I2C EEPROM has been programmed, several data groupings are displayed:

ReadBuffer[000] - ReadBuffer[255] displays various value contents

```

Common Header
Board Area Info
MultiRecord Area
- OEM FMC Record
- DC Load Records (three groups)
- DC Output Records (three groups)
If the FMC IIC EEPROM has not been programmed,
ReadBuffer[000] - ReadBuffer[255] displays buffer contents = 0xFF and
the Common Header reports "Invalid Format Version FF"
At the end of the displayed data, the system controller again displays the FMC Menu.
    
```

Option 3: Read FMC LPC IIC EEPROM

This option displays the FMC I2C EEPROM data, if programmed, in a similar fashion as option 1.

Options 4-7: Set FMC VADJ Voltage

Each of the following options sets the VADJ_1V8 rail to the voltage indicated. The result of choosing an option here may be viewed by returning to the Main Menu, choosing the SYSMON Menu, and selecting option 5: Continuous Scan SYSMON Measurements.

- Option 4: Set FMC VADJ to 1.8V
- Option 5: Set FMC VADJ to 1.5V
- Option 6: Set FMC VADJ to 1.2V
- Option 7: Set FMC VADJ to 0.0V

The result of choosing an option here can be viewed by returning to the Main Menu, choosing the SYSMON Menu, and selecting option 5: Continuous Scan SYSMON Measurements (the results after choosing option 5.Set FMC VADJ to 1.5V are shown here:

```

Press Any Key to Return to SYSMON Menu
Temperature = 33.29 C  Min = 28.15 C  Max = 33.96 C
-----

```

| | Power | Voltage | Current | MIN Current | MAX Current |
|-----------|--------|---------|---------|----------------|----------------|
| VCCINT: | 0.35 W | 0.95 V | 0.37 A | 0.17 A | 0.42 A |
| VCCAUX: | 0.42 W | 1.80 V | 0.23 A | 0.22 A | 0.24 A |
| VCCBRAM: | 0.05 W | 0.95 V | 0.05 A | 0.03 A | 0.05 A |
| VCC1V8: | 0.02 W | 1.80 V | 0.01 A | 0.01 A | 0.01 A |
| VADJ_1V8: | 0.06 W | 1.50 V | 0.04 A | 0.01 A | 0.06 A |
| VCC1V2: | 0.06 W | 1.20 V | 0.05 A | 0.05 A | 0.06 A |
| MGTAVCC: | 0.07 W | 1.00 V | 0.07 A | 0.07 A | 0.09 A |
| MGTAVTT: | 0.03 W | 1.20 V | 0.02 A | 0.02 A | 0.03 A |

Option 0: Return to Main Menu

This option returns to the menu level above.

GPIO Menu

The system controller continuously scans specific user activated inputs and several onboard status signals. Positions 1 – 4 (M3, M2, M1, M0) of MODE DIP switch SW15 are monitored, as well as the five directional user pushbuttons (N, S, E, W, C). The 4-position GPIO DIP switch SW12 is not monitored. The monitored onboard status signals include: FMC1_PRSENT, FMC2_PRSENT, PMBUS_CABLE_B, FPGA_IIC_BUSY, and PMBUS_ALERT.

GPIO Menu Options

```
KCU105 System Controller
- GPIO Menu-
1. Get GPIO PL Data
2. Continuous Scan GPIO Readings
0. Return to Main Menu
Select an option
```

Option 1: Get GPIO PL Data

```
-----
FMC1_PRSENT = NO
FMC2_PRSENT = YES
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = NO
PMBUS_ALERT = NO
```

Option 2: Continuous Scan GPIO Readings

Press any Key to Return to GPIO Menu

When any of the mode DIP SW15 poles 1-4 are changed, or a pushbutton pressed, the value beneath the switch position changes accordingly (showing a 0 or a 1).

```
SYS Mode DIP Switch (M3, M2, M1, M0)
                        0  0  0  0
Pushbuttons (N, S, E, W, C)
                        0  0  0  0  0
-----
FMC1_PRSENT = NO
FMC2_PRSENT = YES
```

```

PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = NO
PMBUS_ALERT   = NO
    
```

Option 0: Return to Main Menu

This option returns to the menu level above.

EEPROM Menu

The system controller EEPROM menu is used to read the contents of the KCU105 on-board EEPROM.

EEPROM Menu Options

```

KCU105 System Controller
- EEPROM Menu -
-----
1. Read Board EEPROM Data
0. Return to Main Menu
Select an option
    
```

Option 1: Read Board EEPROM Data

```

EEPROM  DATA
-----
Board Name:KCU105
Board Revision:1.0
Serial Number:RTK13497603
MAC ID:11:22:33:AA:BB:CC
    
```

Option 0: Return to Main Menu

This option returns to the menu level above.

CONFIG Menu

The system controller CONFIG menu is used to configure the KCU105 UltraScale FPGA from a micro-SD card. One of sixteen bitstreams can be selected for use by the configuration engine by setting a binary encoded value on the system controller mode DIP switch SW15 positions 1 - 4 (M3, M2, M1, M0) prior to board power up. See [FPGA Configuration](#). Once the board is powered up or when the system controller POR pushbutton (SW14) is pressed, the system controller CONFIG Menu can also be used to select the micro-SD card bitstream.

CONFIG Menu Options

```
KCU105 System Controller
- CONFIG Menu-
1. Configure UltraScale FPGA from microSD Card
0. Return to Main Menu
Select an option
```

Option 1: Configure UltraScale FPGA from microSD Card

```
Enter a Bitstream number (0-15):
0
Info: Xilinx.sys opened
Info Configuration definition file "kcu105d/set0/config.def" opened
Info: Clock divider is set to 2
Info: Total 1 device(s) in the chain
Info: Total 1 configuration target(s) in the chain
Info: Target device ID code: 0x3822093
Info: Target device DNA code: 0xD4B3A5820E041
Info: Configuring target(s)...
Info: Bitfile "kcu105d/set0/ipi_app.bit" opened
...10%...20%...30%...40%...50%...60%...70%...80%...90%...100%
Info: Target Done is high
Info: Target Init_b is high
```

```
Configuration completed successfully!
```

Option 0: Return to Main Menu

This option returns to the menu level above.

UltraScale FPGA User Design Considerations

The KCU105 system controller provides simplified access to the programmable features on the KCU105 over an I2C interface. This I2C interface is shared with the UltraScale FPGA and can be driven by an I2C master within a design.

Access to the I2C devices from either the UltraScale FPGA or the system controller takes place over the same shared I2C topology. All I2C accesses go through either the TCA9548 8-port I2C switch or the PCA9544 4-port I2C switch. Designs must deassert the TCA9548 reset (signal IIC_MUX_RESET_B) to access any I2C device attached to one of its eight ports. The PCA9544 4-port I2C switch does not have a reset function.



IMPORTANT: *The TCA9548 U28 RESET_B pin 3 is connected to FPGA U1 bank 64 pin AP10 via level-shifter U44. The PCA9544 U80 does not have a reset pin. FPGA pin AP10 LVCMOS18 net IIC_MUX_RESET_B_LS must be driven High to enable I2C bus transactions with the devices connected to U28.*

Designs that access the SYSMON block over I2C must enable the SYSMON I2C interface and the desired SYSMON channels. See *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 30] for designing with the SYSMON block.

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the KCU105 board provides for designs targeting the KCU105 evaluation board. Net names correlate with net names on the latest KCU105 evaluation board schematic. Users must identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 33] for more information.

The FMC connectors J2 (LPC) and J22 (HPC) are connected to 1.8V VADJ banks. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.



IMPORTANT: *The XDC file can be accessed on the [KCU105 Evaluation Kit website](#).*

Board Setup

Installing the KCU105 Board in a PC Chassis

Installation of the KCU105 board inside a computer chassis is required when developing or testing PCI Express® functionality.

When the KCU105 board is used inside a computer chassis (that is, plugged in to the PCIe® slot), power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable (Figure E-1) to J22 on the KCU105 board. The Xilinx part number for this cable is 2600304. See [Ref 26] for ordering information.



Figure E-1: ATX Power Supply Adapter Cable

To install the KCU105 board in a PC chassis:

1. On the KCU105 board, remove the six screws retaining the six rubber feet with their standoffs, and the PCIe bracket. Reinstall the PCIe bracket using two of the previously removed screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.
5. Plug the KCU105 board into the PCIe connector at this slot.

6. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the KCU105 board in its slot.



IMPORTANT: *The KCU105 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.*

7. Connect the ATX power supply to the KCU105 board using the ATX power supply adapter cable as shown in [Figure E-1](#).
 - a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J15 on the KCU105 board.
 - b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.



CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J15 on the KCU105 evaluation board. The ATX 6-pin connector has a different pin out than J15. Connecting an ATX 6-pin connector into J15 damages the KCU105 evaluation board and voids the board warranty.*

8. Slide the KCU105 board power switch SW1 to the ON position. The PC can now be powered on.

Board Specifications

Dimensions

Height: 5.5 inch (14.0 cm)

Thickness ($\pm 5\%$): 0.062 inch (0.1575 cm)

Length: 10.5 inch (26.7 cm)



IMPORTANT: *The KCU105 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express[®] card.*

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the KCU105 board Master Answer Record concerning the CE requirements for the PC Test Environment:

[KCU105 Evaluation Kit - Master Answer Record \(AR 63175\)](#)

The [Kintex UltraScale KCU105 Declaration of Conformity](#) is online.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*



IMPORTANT: This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

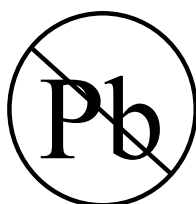
Markings



In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.



This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on Documentation Navigator, see the [Documentation Navigator](#) page on the Xilinx website.

References

The most up to date information related to the KCU105 board and its documentation is available on the following websites.

[KCU105 Evaluation Kit](#)

[KCU105 Evaluation Kit – Master Answer Record 63175](#)

For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the [Xilinx documentation website](#).

These documents and sites provide supplemental material useful with this guide:

1. *Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics* ([DS892](#))
2. *UltraScale Architecture Configuration User Guide* ([UG570](#))
3. *UltraScale Architecture PCB Design User Guide* ([UG583](#))
4. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (Vivado Design Suite)* ([PG150](#))
5. Micron Technology: www.micron.com
(MT40A256M16GE-083E, N25Q256A11ESF40F)
6. Fairchild Semiconductor: www.fairchildsemi.com
(FSSD07)
7. STMicroelectronics: www.st.com
(STG3220)
8. SanDisk Corporation: www.sandisk.com
9. SD Association: www.sdcard.org
10. Digilent: www.digilentinc.com
(USB JTAG Module, Pmod Peripheral Modules)
11. Silicon Labs: www.silabs.com
(Si5335A, Si570, Si53340, Si5328B)
12. *UltraScale Architecture Clocking Resources User Guide* ([UG572](#))
13. *UltraScale Architecture GTH Transceivers User Guide* ([UG576](#))
14. *UltraScale FPGAs Transceivers Wizard Product Guide for Vivado Design Suite* ([PG182](#))

15. *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide (PG156)*
16. PCI Express® standard: www.pcisig.com/specifications
17. SFF-8431 specification: [ftp.seagate.com/sff](ftp://ftp.seagate.com/sff)
18. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide (PG051)*
19. Marvell Semiconductor: www.marvell.com
www.marvell.com/transceivers/alaska-gbe
(M88E1111)
20. *LogiCORE IP AXI UART Lite v2.0 Product Guide (PG142)*
21. Analog Devices: www.analog.com/en/index.html
(ADV7511KSTZ-P, ADP123, ADG707)
22. *DisplayPort LogiCORE Product Guide (PG064)*
23. Texas Instruments: www.ti.com
(TCA9548, PCA9544)
24. *Zynq-7000 SoC Overview Data Sheet (DS190)*
25. *Zynq-7000 SoC Technical Reference Manual (UG585)*
26. The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009. Sourcegate only manufactures the latest revision, which is currently A4. To order, contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and cannot be ordered from the Sourcegate website.
27. Samtec, Inc.: www.samtec.com
(SEAF series connectors)
28. VITA FMC Marketing Alliance: www.vita.com
(FPGA Mezzanine Card (FMC) VITA 57.1 specification)
29. Maxim Integrated: <http://www.maximintegrated.com/products/power/intune/> and <http://www.maxim-ic.com/xilinx>
(Maxim power system devices, InTune™ Digital Power Solutions)

InTune™ Digital PowerTool Software Version 1.08.02 is available. You need to create a Maxim account and login before you can see the link to download the GUI.
30. *UltraScale Architecture System Monitor User Guide (UG580)*

31. *Silicon Labs CP210x USB-to-UART Installation Guide* ([UG1033](#))
32. *Tera Term Terminal Emulator Installation Guide* ([UG1036](#))
33. *Vivado Design Suite User Guide: Using Constraints* ([UG903](#))

The following sources might also be useful with this guide:

34. *Zynq-7000 SoC Packaging and Pinout Product Specification* ([UG865](#))
35. *Zynq-7000 SoC PCB Design* ([UG933](#))
36. Xilinx, Inc: www.xilinx.com

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