FMC XM105 Debug Card User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/06/09	1.0	Initial Xilinx release.
11/11/09	1.0.1	Minor typographical edit.
07/13/10	1.1	• Changed user guide title and product name throughout to XM105. • Minor typographical edits.
09/24/10	1.2	Updated note about FMC cards in Table 1-1.
06/16/11	1.3	Corrected typographical errors in Table 1-3 (to pin H11, FMC_LA04_N) and Table 1-18 (to pin J17-C35).

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About This Guide

This document describes the FMC XM105 debug card (HW-FMC-XM105-G), referred to as the *XM105* in this guide. Xilinx FMC-supported evaluation (carrier) boards are referred to simply as *boards* in this guide.

Guide Contents

This manual contains the following chapters:

- Chapter 1, XM105.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support/mysupport.htm.

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Chapter 1

XM105

Overview

This document describes the FPGA Mezzanine Card (FMC) debug mezzanine card (HW-FMC-XM105-G), referred to as the XM105 in this guide. A Quick Start section and Board Technical Description are combined within this document.

Related Xilinx Documents

Prior to using the XM105 users should be familiar with Xilinx resources. See the following locations for additional documentation on Xilinx tools and solutions:

- ISE: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Intellectual Property: www.xilinx.com/ipcenter

The XM105 must be used in conjunction with a Xilinx board. Documentation for Xilinx boards is available at the following locations:

- SP601: www.xilinx.com/sp601
- SP605: www.xilinx.com/sp605
- ML605: www.xilinx.com/ml605

Quick Start

System Requirements

Hardware

Table 1-1 lists the boards validated to support the XM105. Both low pin count (LPC) and high pin count (HPC) FMC interfaces are supported. The SP601 and SP605 boards provide a single FMC LPC interface. The ML605 board provides one FMC LPC and one FMC HPC interface. The XM105 contains an HPC connector that mates with either LPC or HPC connectors.

Table 1-1: **FMC Supported Boards**

Xilinx Platform	Part Number	FMC LPC Support	FMC HPC Support
Spartan-6 FPGA SP601 Evaluation Kit	EK-S6-SP601-G	1	0
Spartan-6 FPGA SP605 Evaluation Kit	EK-S6-SP605-G	1	0
Virtex-6 FPGA ML605 Evaluation Kit	EK-V6-ML605-G	1	1

Notes:

While every effort has been made to comply with the *FPGA Mezzanine Card Specification*, Xilinx cannot claim nor assume full compliance with the FMC/VITA-57-1 specification. Consequently, Xilinx cannot claim nor support the usage of the XM105 on any other FMC (VITA-57.1) board.

Xilinx FMC cards are generally designed to implement expanded functionality for supported Xilinx evaluation boards (SP601, SP605, or ML605) and thus might exceed the FMC card outline dimensions discussed in the Single Width FMC Module Mechanical section of the FMC/VITA-57-1 specification. Therefore, Xilinx FMC cards might not physically fit in a non-Xilinx evaluation board environment.

Software

Example designs that use this hardware are not provided.

Package Contents

The following items are included in the HW-FMC-XM105-G shipment:

- XM105
- Four (4) mounting screws
- Two (2) standoffs
- Welcome letter

Board documentation, schematics, and PCB design files are available at www.xilinx.com/fmc.

Necessary Equipment

- Small Phillips screwdriver to secure the XM105 to the board
- PC with Internet access to download documentation, board files, and schematics

System Setup

Complete the following steps to install the XM105 to a Xilinx board. For additional information on Xilinx boards, refer to the board's user guide. See Related Xilinx Documents, page 7.

1. Turn off the DC power switch and disconnect the input power source from the board.
2. Remove the XM105 from the electrostatic device (ESD) bag.
3. Using a small Phillips screwdriver, remove the two screws from the bottom side of the two standoffs on the XM105. These screws will be used to attach the board to the standoffs attached to the XM105.
4. Install the XM105 to the board's FMC HPC or FMC LPC connector. The XM105 hangs off the edge of the board as shown in Figure 1-1.
5. Turn the attached board and XM105 unit such that the FPGA is facing the table. Install two screws from the bottom side of board's FMC mounting holes into the two standoffs attached to the XM105. Hand tighten the two mounting screws to the bottom of the board.
6. Turn the attached board and XM105 unit over so that the Xilinx FPGA is visible.
7. Connect the input power source to the board. Turn the board power input switch to ON.

The system is now ready for use. The three power good LEDS on the XM105 should be on, indicating power supplied from the board is good at the XM105.

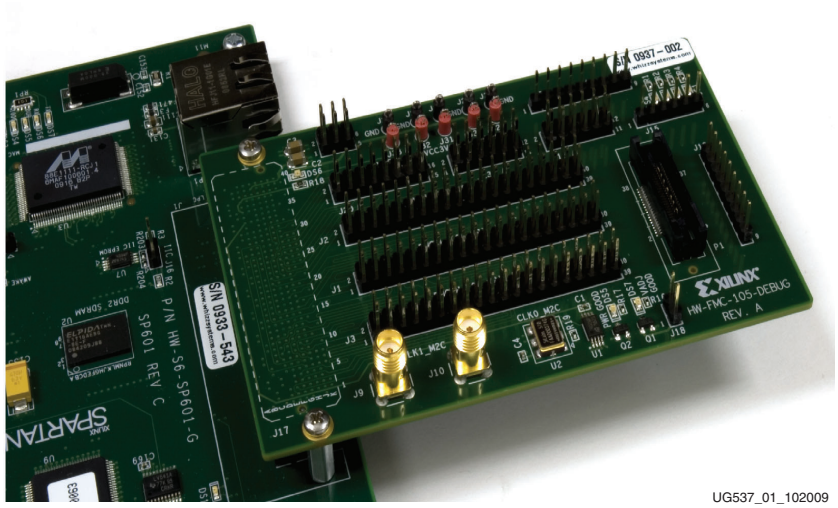

Figure 1-1: **Installation of Mezzanine Card to Board FMC Connector**

Technical Support

Xilinx offers technical support for this product *only* when used in conjunction with boards listed in Table 1-1. For assistance with the XM105 and Xilinx boards, contact Xilinx for technical support at www.xilinx.com/support.

Board Technical Description

The XM105 provides a number of multi-position headers and connectors which break out the FPGA interface signals to and from the board interface. A serial IIC bus reprogrammable LVDS clock source and a pair of SMA connectors provide differential clock sources to the board FPGA. A 2-Kb serial IIC EEPROM is connected to the IIC interface of the board providing non-volatile storage.

Figure 1-2 shows a block diagram of the XM105. The gray shaded blocks are only available when the board interface is a high pin count board interface. All other interfaces are available for low pin count board applications.

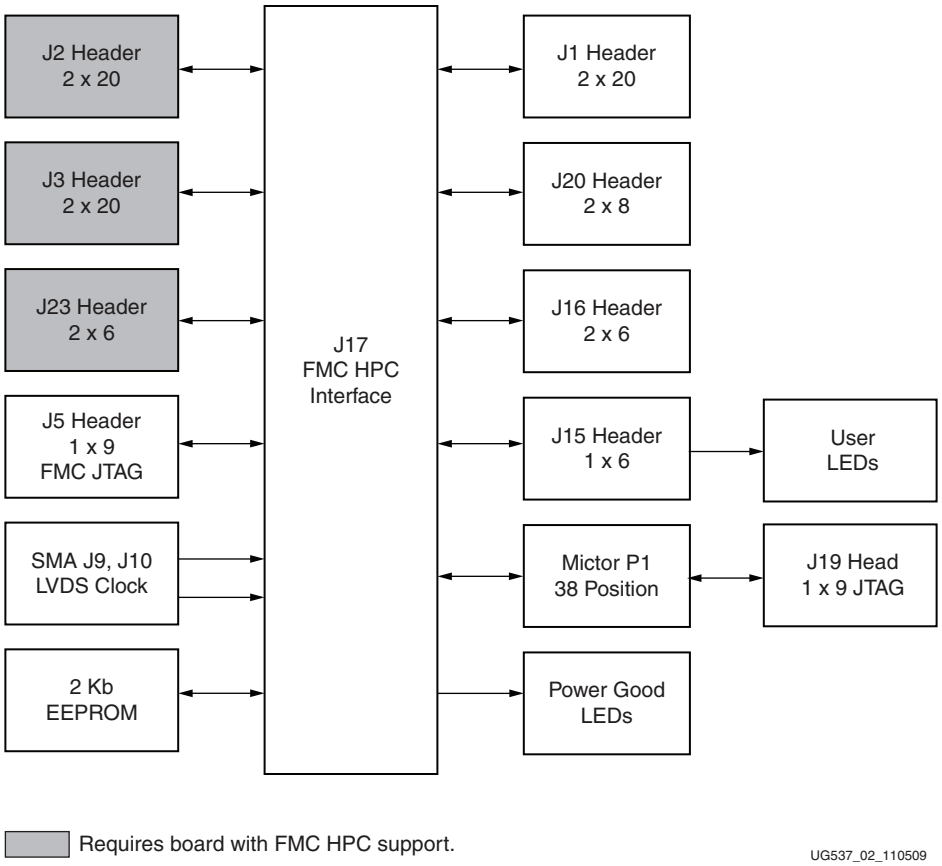

Figure 1-2: **XM105 Block Diagram**

Detailed Description

The numbered features in Figure 1-3 correlate to the features and notes listed in Table 1-2. The XM105 can be installed on a board FMC connector supporting either low pin count or high pin count interfaces. For LPC board applications, the HPC features are not available. All features are available for HPC board applications.

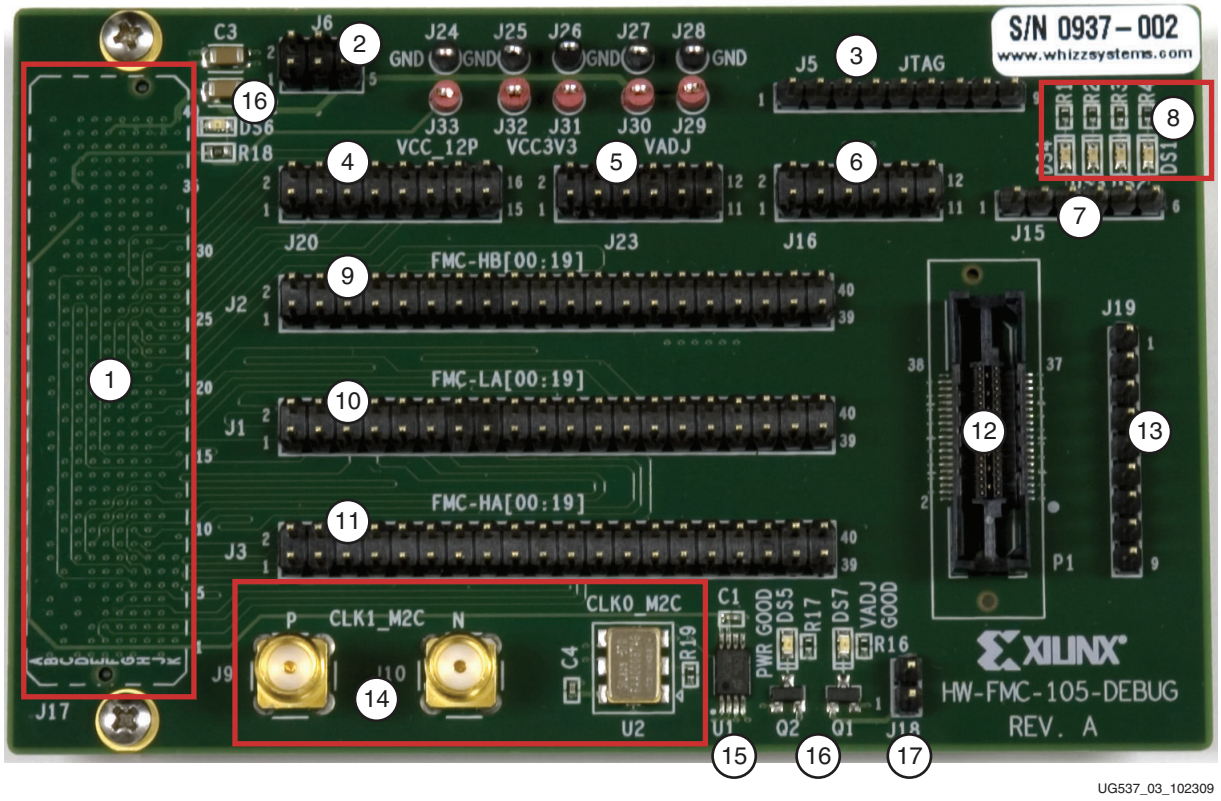

Figure 1-3: **XM105**

Table 1-2: **XM105 Features**

Number	Feature	Notes	Schematic Page
1	VITA 57.1 FMC HPC connector	**J17**: Single-ended signals from the board, clocks, JTAG, power. This connector is mounted on the bottom side of the board.	2-5
2	6-pin header	**J6**: 3 pin x 2 row male header	7
3	9-pin header	**J5**: 9 pin x 1 row male header with FMC JTAG connections	7
4	16-pin header	**J20**: 8 pin x 2 row male header	7
5	12-pin header (1)	**J23**: 6 pin x 2 row male header	8
6	12-pin header	**J16**: 6 pin x 2 row male header	7
7	6-pin header	**J15**: 6 pin x 1 row male header	7
8	User LEDS	Four user LEDS	7

Table 1-2: **XM105 Features *(Cont'd)***

Number	Feature	Notes	Schematic Page
9	40-pin header (1)	**J2**: 20 pin x 2 row male header	8
10	40-pin header	**J1**: 20 pin x 2 row male header	7
11	40-pin header (1)	**J3**: 20 pin x 2 row male header	8
12	Mictor connector	**P1**: 38 pin female Mictor connector	6
13	9-pin header	**J19**: 9 pin x 1 row male header with Mictor JTAG pins connected between J19 and P1	6
14	Clocking	SMA connectors (**J9**, **J10**) and Silicon Labs Si570 IIC serial bus reprogrammable LVDS clock source	9
15	2 Kb EEPROM	IIC compatible electrically erasable programmable memory (EEPROM) with 2 Kb (256 bytes) of non-volatile storage.	2
16	Power Good LEDS	Power good LEDS for +12V, board to mezzanine card (PG_C2M) and V_{adjust}/3.3V	7
17	2-pin header	**J18**: 2 pins x 1 male header for GND connection to PG_M2C LPC connector.	3

Notes:

1. Available only with FMC HPC board interfaces. Xilinx Virtex-6 FPGA ML605 evaluation board provides one FMC LPC and one FMC HPC interface. Xilinx Spartan-6 FPGA SP601 and SP605 evaluation boards provide a single FMC LPC interface.

1. VITA 57.1 FMC HPC Connector J17

This connector provides the interface to the board containing the Xilinx FPGA. The XM105 uses Samtec FMC HPC connector part number ASP-134488-01. The XM105 connector mates with a FMC LPC connector or an FMC HPC connector on Xilinx boards.

Table 1-3 shows the VITA 57.1 FMC HPC pin assignments, associated schematic signal names, and XM105 header or connector to which the signal is wired. Pins labeled as *no connect* are not used on the XM105. Board FPGA signals are wired to various headers and connectors on the XM105. Subsequent sections define each connector, including a connection table showing FMC HPC to breakout connector wiring. Xilinx boards listed in Table 1-3 provide fixed 2.5V power to VADJ pins of the FMC HPC connector.

Table 1-3: **VITA 57.1 FMC HPC Connections**

FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector		FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector
A2	No connect	Not Used		B1	No connect	Not Used
A3				B4		
A6				B5		
A7				B8		
A10				B9		
A11				B12		
A14				B13		
A15				B16		
A18				B17		
A19				B20		
A22				B21		
A23				B24		
A26				B25		
A27				B28		
A30				B29		
A31				B32		
A34				B33		
A35				B36		
A38				B37		
A39				B40		

Table 1-3: **VITA 57.1 FMC HPC Connections *(Cont'd)***

FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector		FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector
C2	No Connect	Not Used		D1	PG_C2M	
C3				D4	No Connect	Not Used
C6				D5		
C7				D8	FMC_LA01_CC_P	J1, P1
C10	FMC_LA06_P	J1, P1		D9	FMC_LA01_CC_N	J1, P1
C11	FMC_LA06_N			D11	FMC_LA05_P	
C14	FMC_LA10_P			D12	FMC_LA05_N	
C15	FMC_LA10_N			D14	FMC_LA09_P	
C18	FMC_LA14_P	J1		D15	FMC_LA09_N	
C19	FMC_LA14_N			D17	FMC_LA13_P	J1
C22	FMC_LA18_CC_P			D18	FMC_LA13_N	
C23	FMC_LA18_CC_N			D20	FMC_LA17_CC_P	
C26	FMC_LA27_P	J20		D21	FMC_LA17_CC_N	
C27	FMC_LA27_N			D23	FMC_LA23_P	J20
C30	IIC_SCL_MAIN	EEPROM, Si570		D24	FMC_LA23_N	
C31	IIC_SDA_MAIN			D26	FMC_LA26_P	
C34	GA0	EEPROM		D27	FMC_LA26_N	
C35	VCC12			D29	FMC_TCK	J5
C37	VCC12			D30	FMC_TDI	
C39	VCC3V3			D31	FMC_TDO	
				D32	VCC3V3_AUX	
				D33	FMC_TMS	J5
				D34	No connect	
				D35	GA1	EEPROM
				D36	VCC3V3	
				D38	VCC3V3	
				D40	VCC3V3	

Table 1-3: **VITA 57.1 FMC HPC Connections *(Cont'd)***

FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector		FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector
E2	FMC_HA01_CC_P	J3		F1	FMC_PG_M2C	
E3	FMC_HA01_CC_N			F4	FMC_HA00_CC_P	J3
E6	FMC_HA05_P			F5	FMC_HA00_CC_N	
E7	FMC_HA05_N			F7	FMC_HA04_P	
E9	FMC_HA09_P			F8	FMC_HA04_N	
E10	FMC_HA09_N			F10	FMC_HA08_P	
E12	FMC_HA13_P			F11	FMC_HA08_N	
E13	FMC_HA13_N			F13	FMC_HA12_P	
E15	FMC_HA16_P			F14	FMC_HA12_N	
E16	FMC_HA16_N			F16	FMC_HA15_P	
E18	FMC_HA20_P	J23		F17	FMC_HA15_N	
E19	FMC_HA20_N			F19	FMC_HA19_P	
E21	FMC_HB03_P	J2		F20	FMC_HA19_N	
E22	FMC_HB03_N			F22	FMC_HB02_P	J2
E24	FMC_HB05_P			F23	FMC_HB02_N	
E25	FMC_HB05_N			F25	FMC_HB04_P	
E27	FMC_HB09_P			F26	FMC_HB04_N	
E28	FMC_HB09_N			F28	FMC_HB08_P	
E30	FMC_HB13_P			F29	FMC_HB08_N	
E31	FMC_HB13_N			F31	FMC_HB12_P	
E33	FMC_HB19_P			F32	FMC_HB12_N	
E34	FMC_HB19_N			F34	FMC_HB16_P	
E36	FMC_HB21_P	J23		F35	FMC_HB16_N	
E37	FMC_HB21_N			F37	FMC_HB20_P	J23
E39	VADJ			F38	FMC_HB20_N	
				F40	VADJ	
G2	CLK1_M2C_P	J9		H1	No connect	
G3	CLK1_M2C_N	J10		H2	Tied to GND (PRSNT_M2C_L)	
G6	FMC_LA00_CC_P	J1, P1		H4	CLK0_M2C_P	Si570
G7	FMC_LA00_CC_N	J1		H5	CLK0_M2C_N	

Table 1-3: **VITA 57.1 FMC HPC Connections *(Cont'd)***

FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector		FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector
G9	FMC_LA03_P	J1, P1		H7	FMC_LA02_P	J1, P1
G10	FMC_LA03_N			H8	FMC_LA02_N	
G12	FMC_LA08_P			H10	FMC_LA04_P	
G13	FMC_LA08_N			H11	FMC_LA04_N	
G15	FMC_LA12_P	J1		H13	FMC_LA07_P	
G16	FMC_LA12_N			H14	FMC_LA07_N	
G18	FMC_LA16_P			H16	FMC_LA11_P	J1
G19	FMC_LA16_N			H17	FMC_LA11_N	
G21	FMC_LA20_P	J20		H19	FMC_LA15_P	
G22	FMC_LA20_N			H20	FMC_LA15_N	
G24	FMC_LA22_P			H22	FMC_LA19_P	
G25	FMC_LA22_N			H23	FMC_LA19_N	
G27	FMC_LA25_P			H25	FMC_LA21_P	J20
G28	FMC_LA25_N			H26	FMC_LA21_N	
G30	FMC_LA29_P	J16		H28	FMC_LA24_P	
G31	FMC_LA29_N			H29	FMC_LA24_N	
G33	FMC_LA31_P			H31	FMC_LA28_P	J16
G34	FMC_LA31_N			H32	FMC_LA28_N	
G36	FMC_LA33_P	J15		H34	FMC_LA30_P	
G37	FMC_LA33_N			H35	FMC_LA30_N	
G39	VADJ			H37	FMC_LA32_P	J15
				H38	FMC_LA32_N	
				H40	VADJ	

Table 1-3: **VITA 57.1 FMC HPC Connections *(Cont'd)***

FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector		FMC HPC Pin	Schematic Net Name	Breakout Signal to Connector
J2	No connect	Not Used		K1	No connect	Not Used
J3				K4		
J6	FMC_HA03_P	J3		K5		
J7	FMC_HA03_N			K7	FMC_HA02_P	J3
J9	FMC_HA07_P			K8	FMC_HA02_N	
J10	FMC_HA07_N			K10	FMC_HA06_P	
J12	FMC_HA11_P			K11	FMC_HA06_N	
J13	FMC_HA11_N			K13	FMC_HA10_P	
J15	FMC_HA14_P			K14	FMC_HA10_N	
J16	FMC_HA14_N			K16	FMC_HA17_CC_P	
J18	FMC_HA18_P			K17	FMC_HA17_CC_N	
J19	FMC_HA18_N			K19	FMC_HA21_P	J23
J21	FMC_HA22_P	J23		K20	FMC_HA21_N	
J22	FMC_HA22_N			K22	FMC_HA23_P	
J24	FMC_HB01_P	J2		K23	FMC_HA23_N	
J25	FMC_HB01_N			K25	FMC_HB00_CC_P	J2
J27	FMC_HB07_P			K26	FMC_HB00_CC_N	
J28	FMC_HB07_N			K28	FMC_HB06_CC_P	
J30	FMC_HB11_P			K29	FMC_HB06_CC_N	
J31	FMC_HB11_N			K31	FMC_HB10_P	
J33	FMC_HB15_P			K32	FMC_HB10_N	
J34	FMC_HB15_N			K34	FMC_HB14_P	
J36	FMC_HB18_P			K35	FMC_HB14_N	
J37	FMC_HB18_N			K37	FMC_HB17_CC_P	
J39	VADJ			K38	FMC_HB17_CC_N	
				K40	VADJ	

See the Xilinx board user guides and schematics for a description of features provided by LPC and/or HPC interfaces contained on the board, including power supply specifications, FPGA banking connectivity, and FPGA pin assignments.

- For SP601 LPC interface, see UG518 *SP601 Hardware User Guide*
- For SP605 LPC interface, see UG526 *SP605 Hardware User Guide*
- For ML605 LPC and HPC interfaces, see UG534 *ML605 Hardware User Guide*

See the *VITA57.1 Specification* at www.vita.com/fmc.html for additional information on FMC.

2. Connector J6 6-pin Header

This 3 x 2 position header provides a means to manually configure XM105 voltage connections provided to the J16 connector by configuring the shunts on the XM105. Shunts are not provided with the kit.

For 3.3V power:

Install a shunt on connector J6-1 to J6-3 and another shunt on connector J6-2 to J6-4 to connect the board 3.3V power to the HDR_POWER net on connector J16 pins 1 and 2.

For VADJ power:

Install a shunt on connector J6-3 to J6-5 and another shunt on connector J6-4 to J6-6 connect the board VADJ power to the HDR_POWER net on connector J16 pins 1 and 2.

Xilinx boards provide fixed 2.5V power to the VADJ pins of the FMC connector.

3. Connector J5 FMC JTAG

This 9-position connector provides an interface from the XM105 to the board's FMC LPC or FMC HPC JTAG signals. This interface is not intended to provide a means to program the FPGA on the board. See the Xilinx board user guide for details of board JTAG interface support of FMC mezzanine cards. Connections between the mezzanine FMC HPC and connector J5 are defined in Table 1-4.

Table 1-4: **Mezzanine FMC HPC J17 to Connector J5 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J5 Connector Pin
3.3V	3.3V	1
GROUND	GROUND	2
–	NC(1)	3
D29	FMC_TCK	4
–	NC	5
D31	FMC_TDO	6
D30	FMC_TDI	7
–	NC	8
D33	FMC_TMS	9

Notes:

1. No connection (NC).

4. Connector J20

This 16-position connector provides an interface from the XM105 to 16 single-ended signals on the board's FMC LPC or FMC HPC interface. Connections between the mezzanine FMC HPC and connector J20 are defined in Table 1-5.

Table 1-5: **Mezzanine FMC HPC J17 to Connector J20 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J20 Connector Odd Pins		FMC HPC Connector J17 Pin	Signal Name	J20 Connector Even Pins
G21	FMC_LA20_P	1		H28	FMC_LA24_P	2
G22	FMC_LA20_N	3		H29	FMC_LA24_N	4
H25	FMC_LA21_P	5		G27	FMC_LA25_P	6
H26	FMC_LA21_N	7		G28	FMC_LA25_N	8
G24	FMC_LA22_P	9		D26	FMC_LA26_P	10
G25	FMC_LA22_N	11		D27	FMC_LA26_N	12
D23	FMC_LA23_P	13		C26	FMC_LA27_P	14
D24	FMC_LA23_N	15		C27	FMC_LA27_N	16

5. Connector J23

This 12-position connector provides an interface from the XM105 to 12 single-ended signals on the board's FMC HPC interface. Connections between the mezzanine FMC HPC and connector J23 are defined in Table 1-6. This interface can only be used when the XM105 is installed on a board supporting the FMC HPC interface.

Table 1-6: **Mezzanine FMC HPC J17 to Connector J23 Pin Assignments**

FMC HPC Connector(1) J17 Pin	Signal Name	J23 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	J23 Connector (Even Pins)
F37	FMC_HB20_P(2)	1		E36	FMC_HB21_P(2)	2
F38	FMC_HB20_N(2)	3		E37	FMC_HB21_N(2)	4
E18	FMC_HA20_P	5		J21	FMC_HA22_P	6
E19	FMC_HA20_N	7		J22	FMC_HA22_N	8
K19	FMC_HA21_P	9		K22	FMC_HA23_P	10
K20	FMC_HA21_N	11		K23	FMC_HA23_N	12

Notes:

1. Available only when connected to board with FMC HPC interface support.
2. These pins are not connected on the Xilinx ML605 FMC HPC board interface.

6. Connector J16

This 12-position connector provides an interface from the XM105 to 12 single-ended signals on the board's FMC LPC or FMC HPC interface. Connections between the mezzanine FMC HPC and connector J16 are defined in Table 1-7.

Table 1-7: **Mezzanine FMC HPC J17 to Connector J16 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J16 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	J16 Connector (Even Pins)
–	HDR_POWER(1)	1		–	HDR_POWER	2
–	GROUND	3		–	GROUND	4
H31	FMC_LA28_P	5		H34	FMC_LA30_P	6
H32	FMC_LA28_N	7		H35	FMC_LA30_N	8
G30	FMC_LA29_P	9		G33	FMC_LA31_P	10
G31	FMC_LA29_N	11		G34	FMC_LA31_N	12

Notes:

1. HDR_POWER can be either 3.3V or 2.5. See connector J6 (2. Connector J6 6-pin Header, page 18) for configuration options.

7. Connector J15

This 6-position connector provides an interface from the XM105 to four single-ended signals on the board's FMC LPC or FMC HPC interface. Connections between the mezzanine FMC HPC and connector J15 are defined in Table 1-8. These four FMC LPC signals are connected to green LEDS on the XM105.

Table 1-8: **Mezzanine FMC J17 to Connector J15 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J15 Connector (Odd Pins)	User LED Reference Designator Silk Screen
–	VADJ	1	–
–	GROUND	2	–
H37	FMC_LA32_P(1)	3	DS4
H38	FMC_LA32_N(1)	4	DS3
G36	FMC_LA33_P(1)	5	DS2
G37	FMC_LA33_N(1)	6	DS1

Notes:

1. These signals are also connected to the anode of green LEDS. The LED cathodes are connected to 27.4 ohm resistors to ground.

8. User LEDS

Four green user LEDS are provided on the XM105, with reference designators as shown in Table 1-8. LEDS are illuminated with an active-High signal from the FPGA on the board.

9. Connector J2

This 40-position connector provides an interface from the XM105 to 40 single-ended signals on the board's FMC HPC interface. Connections between the mezzanine FMC HPC and connector J2 are defined in Table 1-9, This interface can only be utilized when installed in a board supporting the FMC HPC interface.

Table 1-9: **Mezzanine FMC HPC J17 to Connector J2 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J2 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	J2 Connector (Even Pins)
K25	FMC_HB00_CC _P(1)	1		K31	FMC_HB10_P	2
K26	FMC_HB00_CC _N(1)	3		K32	FMC_HB10_N	4
J24	FMC_HB01_P	5		J30	FMC_HB11_P	6
J25	FMC_HB01_N	7		J31	FMC_HB11_N	8
F22	FMC_HB02_P	9		F31	FMC_HB12_P	10
F23	FMC_HB02_N	11		F32	FMC_HB12_N	12
E21	FMC_HB03_P	13		E30	FMC_HB13_P	14
E22	FMC_HB03_N	15		E31	FMC_HB13_N	16

Table 1-9: **Mezzanine FMC HPC J17 to Connector J2 Pin Assignments *(Cont'd)***

FMC HPC Connector J17 Pin	Signal Name	J2 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	J2 Connector (Even Pins)
F25	FMC_HB04_P	17		K34	FMC_HB14_P	18
F26	FMC_HB04_N	19		K35	FMC_HB14_N	20
E24	FMC_HB05_P	21		J33	FMC_HB15_P	22
E25	FMC_HB05_N	23		J34	FMC_HB15_N	24
K28	FMC_HB06_CC _P(1)	25		F34	FMC_HB16_P	26
K29	FMC_HB06_CC _N(1)	27		F35	FMC_HB16_N	28
J27	FMC_HB07_P	29		K37	FMC_HB17_CC _P(1)	30
J28	FMC_HB07_N	31		K38	FMC_HB17_CC _N(1)	32
F28	FMC_HB08_P	33		J36	FMC_HB18_P	34
F29	FMC_HB08_N	35		J37	FMC_HB18_N	36
E27	FMC_HB09_P	37		E33	FMC_HB19_P	38
E28	FMC_HB09_N	39		E34	FMC_HB19_N	40

Notes:

1. Signal names with "_CC_" can be connected to FPGA clock capable pins on the board. See Xilinx board user guides for additional information.

10. Connector J1

This 40-position connector provides an interface from the XM105 to 40 single-ended signals on the board's FMC LPC or FMC HPC interface. Connections between the mezzanine FMC HPC and J1 are defined in Table 1-10.

Table 1-10: **Mezzanine FMC HPC J17 to Connector J1 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J1 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	J1 Connector (Even Pins)
G6	FMC_LA00_CC_P (1)	1		C14	FMC_LA10_P	2
G7	FMC_LA00_CC_N(1)	3		C15	FMC_LA10_N	4
D8	FMC_LA01_CC_P(1)	5		H16	FMC_LA11_P	6
D9	FMC_LA01_CC_N(1)	7		H17	FMC_LA11_N	8
H7	FMC_LA02_P	9		G15	FMC_LA12_P	10
H8	FMC_LA02_N	11		G16	FMC_LA12_N	12
G9	FMC_LA03_P	13		D17	FMC_LA13_P	14
G10	FMC_LA03_N	15		D18	FMC_LA13_N	16
H10	FMC_LA04_P	17		C18	FMC_LA14_P	18
H11	FMC_LA04_N	19		C19	FMC_LA14_N	20
D11	FMC_LA05_P	21		H19	FMC_LA15_P	22
D12	FMC_LA05_N	23		H20	FMC_LA15_N	24
C10	FMC_LA06_P	25		G18	FMC_LA16_P	26
C11	FMC_LA06_N	27		G19	FMC_LA16_N	28
H13	FMC_LA07_P	29		D20	FMC_LA17_CC _P (1)	30
H14	FMC_LA07_N	31		D21	FMC_LA17_CC _N(1)	32
G12	FMC_LA08_P	33		C22	FMC_LA18_CC _P(1)	34
G13	FMC_LA08_N	35		C23	FMC_LA18_CC _N(1)	36
D14	FMC_LA09_P	37		H22	FMC_LA19_P	38
D15	FMC_LA09_N	39		H23	FMC_LA19_N	40

Notes:

1. Signal names with "_CC_" can be connected to FPGA clock capable pins on the board. See Xilinx board user guides for additional information.

11. Connector J3

This 40-position connector provides an interface from the XM105 to 40 single-ended signals on the board's FMC HPC interface. Connections between the mezzanine FMC HPC and connector J3 are defined in Table 1-11. This interface can only be used when installed on a board supporting the FMC HPC interface.

Table 1-11: **Mezzanine FMC HPC J17 to Connector J3 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	J3 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	J3 Connector (Even Pins)
F4	FMC_HA00_CC _P (1)	1		K13	FMC_HA10_P	2
F5	FMC_HA00_CC _N(1)	3		K14	FMC_HA10_N	4
E2	FMC_HA01_CC _P(1)	5		J12	FMC_HA11_P	6
E3	FMC_HA01_CC _N(1)	7		J13	FMC_HA11_N	8
K7	FMC_HA02_P	9		F13	FMC_HA12_P	10
K8	FMC_HA02_N	11		F14	FMC_HA12_N	12
J6	FMC_HA03_P	13		E12	FMC_HA13_P	14
J7	FMC_HA03_N	15		E13	FMC_HA13_N	16
F7	FMC_HA04_P	17		J15	FMC_HA14_P	18
F8	FMC_HA04_N	19		J16	FMC_HA14_N	20
E6	FMC_HA05_P	21		F16	FMC_HA15_P	22
E7	FMC_HA05_N	23		F17	FMC_HA15_N	24
K10	FMC_HA06_P	25		E15	FMC_HA16_P	26
K11	FMC_HA06_N	27		E16	FMC_HA16_N	28
J9	FMC_HA07_P	29		K16	FMC_HA17_CC _P(1)	30
J10	FMC_HA07_N	31		K17	FMC_HA17_CC _N(1)	32
F10	FMC_HA08_P	33		J18	FMC_HA18_P	34
F11	FMC_HA08_N	35		J19	FMC_HA18_N	36
E9	FMC_HA09_P	37		F19	FMC_HA19_P	38
E10	FMC_HA09_N	39		F20	FMC_HA19_N	40

Notes:

1. Signal names with "_CC_" can be connected to FPGA clock capable pins on the board. See Xilinx board user guides for additional information.

12. Mictor Connector P1

This 38-position connector contains an interface from the XM105 to 21 signals on the board's FMC LPC or FMC HPC interface. Four Mictor JTAG signals are wired to connector J19. Connections between the mezzanine FMC HPC and connector P1 are defined in Table 1-12. The Mictor connector is AMP part number 2-767004-2.

Table 1-12: **Mezzanine FMC J17 to Mictor Connector P1 Pin Assignments**

FMC HPC Connector J17 Pin	Signal Name	P1 Connector (Odd Pins)		FMC HPC Connector J17 Pin	Signal Name	P1 Connector (Even Pins)
–	NC	1		NA	NC	2
–	NC	3		NA	NC	4
–	NC	5		G6	FMC_LA00_CC _P(2)	6
–	NC	7		NA	NC	8
–	NC	9		NA	NC	10
NC	MICTOR_TDO(1)	11			VADJ	12
–	NC	13		NA	NC	14
NC	MICTOR_TCK(1)	15		D9	FMC_LA01_CC _N(2)	16
NC	MICTOR_TMS(1)	17		D8	FMC_LA01_CC _P(2)	18
NC	MICTOR_TDI(1)	19		D15	FMC_LA09_N	20
–	NC	21		D14	FMC_LA09_P	22
G13	FMC_LA08_N	23		H11	FMC_LA04_N	24
G12	FMC_LA08_P	25		H10	FMC_LA04_P	26
H14	FMC_LA07_N	27		G10	FMC_LA03_N	28
H13	FMC_LA07_P	29		G9	FMC_LA03_P	30
C11	FMC_LA06_N	31		H8	FMC_LA02_N	32
C10	FMC_LA06_P	33		H7	FMC_LA02_P	34
D12	FMC_LA05_N	35		C15	FMC_LA10_N	36
D11	FMC_LA05_P	37		C14	FMC_LA10_P	38

Notes:

1. Mictor JTAG signals are available on 9-position connector J19.
2. Signal names with "_CC_" may be connected to FPGA clock capable pins on the board. See Xilinx board user guides for additional information.

13. Connector J19

This 9-position connector (Table 1-13) does not have an interface to the FMC LPC or FMC HPC interface of the board. It provides a connection to Mictor connector P1 and includes 3.3V and GROUND connections.

Table 1-13: **Connector J19 Pin Assignments**

Signal Name	J19 Connector Pin	Mictor P1 Connector Pin
3.3V	1	–
GROUND	2	–
NC	3	–
MICTOR_TCK	4	15
NC	5	–
MICTOR_TDO	6	11
MICTOR_TDI	7	19
NC	8	–
MICTOR_TMS	9	17

14. Clocks

Two clock sources (Table 1-14) are provided for FMC LPC and FMC HPC board applications:

- Differential SMA connectors
- Si570 IIC LVDS clock

A pair of differential SMA connectors can be utilized to provide a high-precision differential clock or a single-ended clock to the board. Virtex-6 FPGA and Spartan-6 FPGA devices require single-ended clocks on the "P" input of an IOB pair. See Xilinx FPGA documentation for additional information.

Consult Xilinx FMC- supported board user guide for interface voltages, I/O standard support on FPGA clock pins; and to determine LVDS input clock termination requirements, either on the printed-circuit board or using an IBUFGDS primitive for FPGA on-chip termination.

Table 1-14: **Clock Sources Routed to Mezzanine FMC HPC J17 Connector**

FMC HPC Connector J17 Pin	Signal Name	Source(1)
H4	CLK0_M2C_P(2)	Si570 U2 pin 4
H5	CLK0_M2C_N(2)	Si570 U2 pin 5
G2	CLK1_M2C_P	SMA J9
G3	CLK1_M2C_N	SMA J10

Notes:

1. Clock sources are available for FMC LPC and FMC HPC board applications.
2. The Si570 provides a LVDS output clock.

A Silicon Labs Si570 IIC programmable clock source provides a low-jitter clock with a user-programmable output frequency from 10 to 810 MHz. As shipped, the CLK0_M2C clock frequency is 156.25 MHz. The component installed on the XM105 is factory programmed with parameters in Table 1-15.

Table 1-15: **Characteristics of Si570 Component**

Si570 Characteristic	XM105
Output Format	LVDS
Output Enable Polarity	High
Temperature Stability	50 ppm
Frequency Range	10–810 MHz
Six-Digit Startup	156.250 MHz
Power Supply	3.3V
IIC Address	x5D

For additional information on this component, including reprogramming the clock frequency through the IIC serial bus interface, consult the Silicon Labs *Si570 Data Sheet* at https://www.silabs.com.

15. 2-Kb EEPROM

A ST Microelectronics M24C02 2-Kb serial IIC bus EEPROM component provides a small amount of non-volatile memory storage on the XM105.

The IIC address of this component is controlled by a combination of the specific board interface and chip enable connections to the component inputs on the XM105. Signals GA0 and GA1 from the board are connected to the chip enable inputs of the M24C02 component enables E0 and E1. As shown in Table 1-16, Xilinx boards provide GA0 and GA1 signal strapping to 3.3V and GND signals, which creates a different E0 and E1 chip enable decode on the E1 and E0 inputs of the EEPROM.

The IIC memory addressing protocol requires a bus master to initiate communication to a peripheral device using a start condition followed by a device select code. The device select code consists of a 4-bit Device Type Identifier and a 3-bit Chip Enable Address (E2, E1, E0). Bit 0 is used to indicate read/write. The Device Type Identifier for the EEPROM is `1010` binary. Table 1-17 shows the generic EEPROM Device Select Code as well as specific Device Code Select addresses for the EEPROM when the XM105 is connected to boards defined in Table 1-1, page 8.

Table 1-16: **M24C02 Enable Input Connections**

M24C02 Chip Enable Input	FMC HPC Control Signal Connection	SP601 LPC Connector	SP605 LPC Connector	ML605 LPC Connector	ML605 HPC Connector
E0	GA1	GND	GND	3.3V	GND
E1	GA0	3.3V	3.3V	GND	GND
E2	GND	GND	GND	GND	GND

Table 1-17: **EEPROM IIC Device Select Code**

Bit 7:4 Device Type Identifier	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Description
`1010`	E2	E1	E0	Read/$\overline{\text{Write}}$	M24C02 Device Select Code
`1010`	0	GA0	GA1	Read/$\overline{\text{Write}}$	Connected to XM105
`1010`	0	1	0	Read/$\overline{\text{Write}}$	Connected to SP601 LPC interface
`1010`	0	1	0	Read/$\overline{\text{Write}}$	Connected to SP605 LPC interface
`1010`	0	0	1	Read/$\overline{\text{Write}}$	Connected to ML605 LPC interface
`1010`	0	0	0	Read/$\overline{\text{Write}}$	Connected to ML605 HPC interface

16. Power Good LEDS

Three power good LEDS are on the board with functions defined in Table 1-18.

Table 1-18: **Power Good LED Indicators**

Power Good Indicator	Description	Controlled by...
DS5	Board power good	This LED is driven by the signal PG_C2M output from the board to the mezzanine connector on connector J17 pin D1. Board power good is indicated when this LED is on. Reference the Xilinx board schematics and user guides for additional information on the power system.
DS6	XM105 +12V input power good	+12V input voltage from FMC LPC pins J17-C35 and J17-C37. The +12V power input is good when this LED is on.
DS7	XM105 VADJ input power good	VADJ input voltage on the FMC HPC VADJ pins from the board power is good. Xilinx FMC-supported platforms listed in Table 1-1, page 8 connect 2.5V to the FMC HPC and FMC LPC connectors.

17. Connector J18

This 2 x 1 position connector facilitates connection of the board signal PG_M2C on pin J17-F1 to ground on the XM105. Boards listed in Table 1-1, page 8 have pull-up resistors on this FPGA input. Connection to ground is only used to signal *power not good* from the XM105 to the board. There are no power supplies on this XM105. By default, the connector is left open. See Xilinx board user guides and schematics for additional information.

- Shunt OFF = PG_M2C signal asserted on the board through pull-up resistor to V_{CCO} (default). No connection to the XM105.
- Shunt ON = J17-F1 PG_M2C signal connected to GND. *Power not good* signaled to the board.

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