

FH8707G3

N- Channel Enhancement Mode Power MOSFET

Description

The FH8707G3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

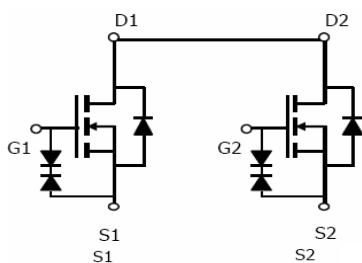
General Features

- $V_{DS} = 20V, I_D = 12A$
- $R_{DS(ON)} < 7.9 \text{ m}\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} < 8.3 \text{ m}\Omega @ V_{GS}=3.8V$
- $R_{DS(ON)} < 9.8 \text{ m}\Omega @ V_{GS}=2.5V$
- ESD Rating: 2000V HBM

Application

- PWM application
- Load switch

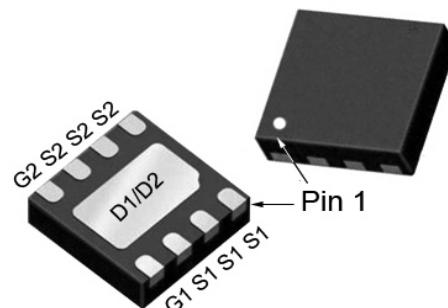
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package



Schematic diagram



Marking and pin assignment



DFN3x3-8L Pin assignment and Top / Bottom View

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	12	A
Drain Current-Pulsed (Note 1)	I_{DM}	48	A
Maximum Power Dissipation (T _A =25 °C)	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	42.6	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=18V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.8	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=6.0A$		5.5	7.9	$m\Omega$
		$V_{GS}=3.8V, I_D=5.0A$		5.8	8.3	$m\Omega$
		$V_{GS}=2.5V, I_D=4.0A$		7.4	9.8	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=5A$	-	19	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, F=1.0MHz$	-	1280	-	PF
Output Capacitance	C_{oss}		-	254	-	PF
Reverse Transfer Capacitance	C_{rss}		-	185	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1.35\Omega, V_{GS}=5V, R_{GEN}=3\Omega$	-	6		nS
Turn-on Rise Time	t_r		-	13		nS
Turn-Off Delay Time	$t_{d(off)}$		-	52		nS
Turn-Off Fall Time	t_f		-	16		nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=7A, V_{GS}=4.5V$	-	15		nC
Gate-Source Charge	Q_{gs}		-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=1A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	7	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

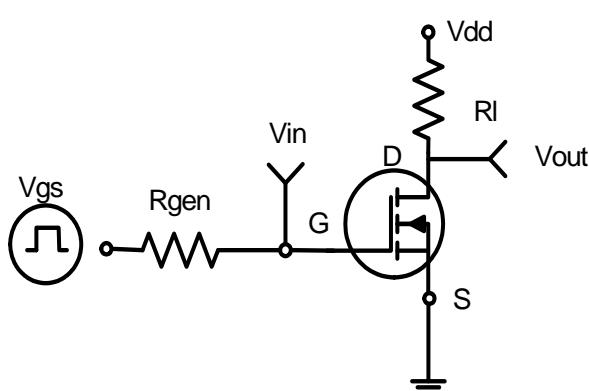


Figure 1:Switching Test Circuit

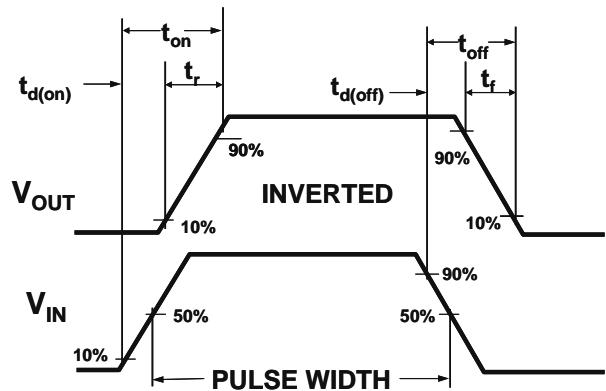


Figure 2:Switching Waveforms

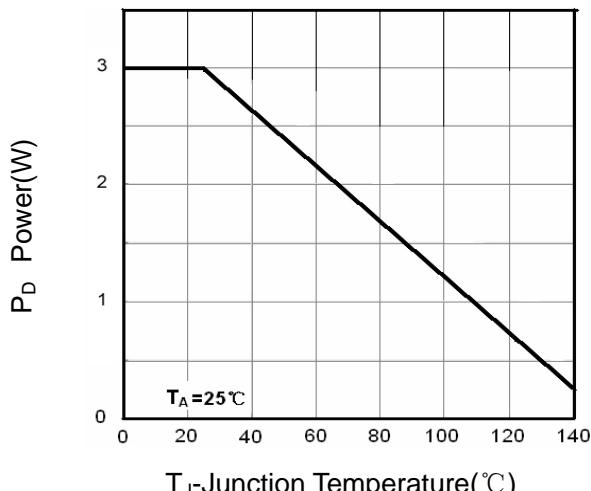


Figure 3 Power Dissipation

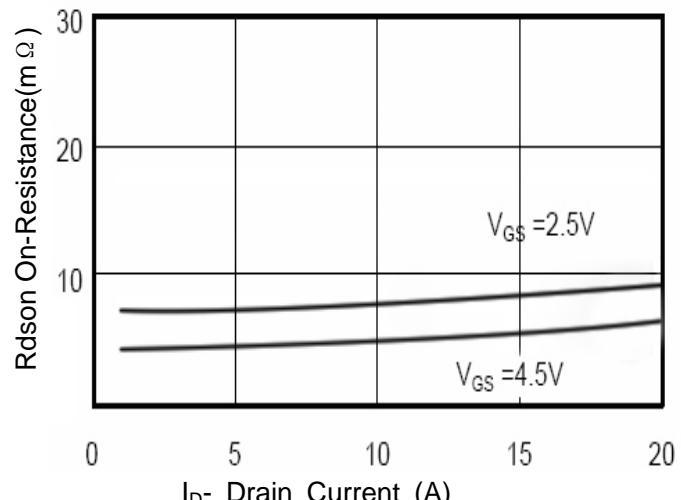


Figure 4 Drain-Source On-Resistance

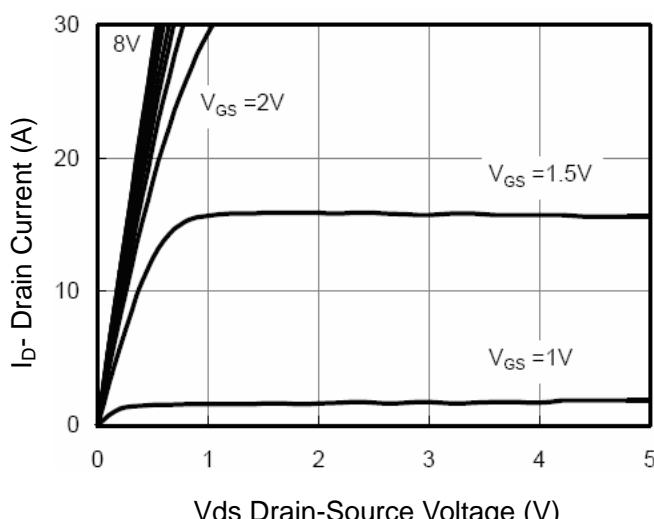


Figure 5 Output CHARACTERISTICS

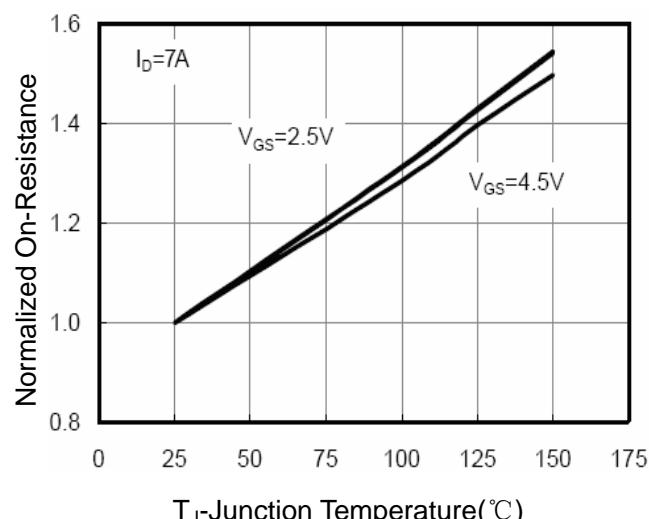


Figure 6 Drain-Source On-Resistance

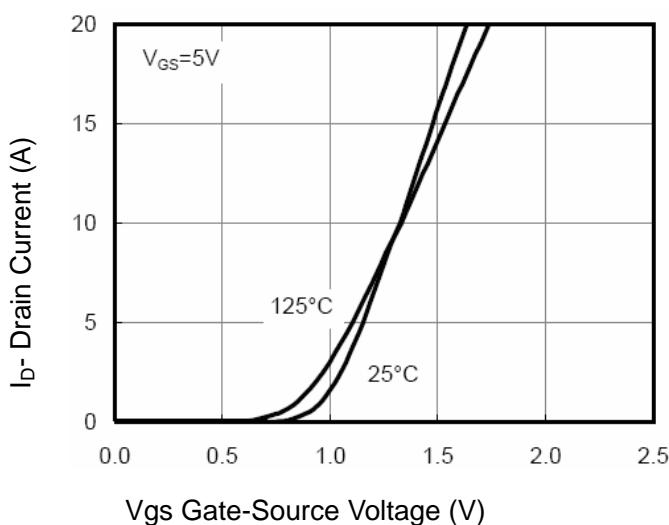


Figure 7 Transfer Characteristics

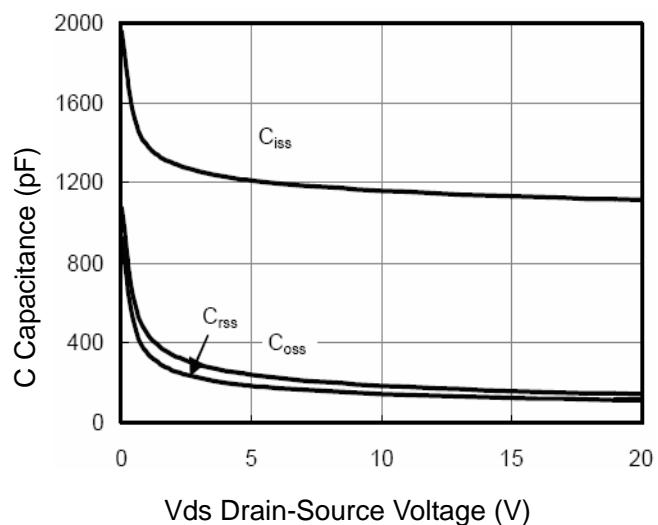


Figure 8 Capacitance vs Vds

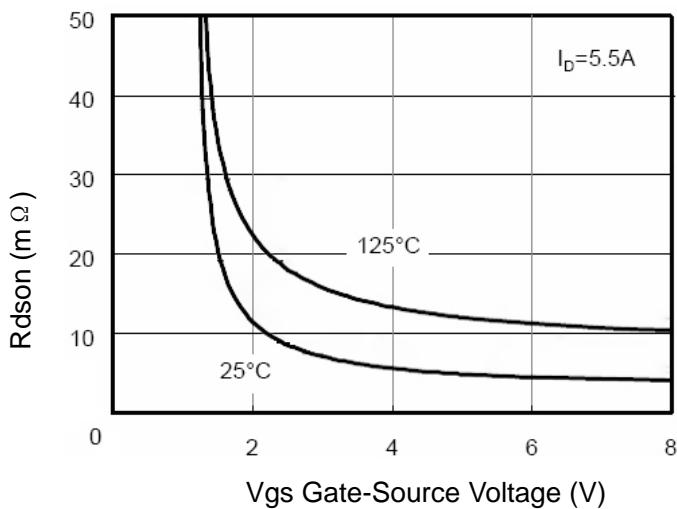


Figure 9 $R_{DS(on)}$ vs V_{GS}

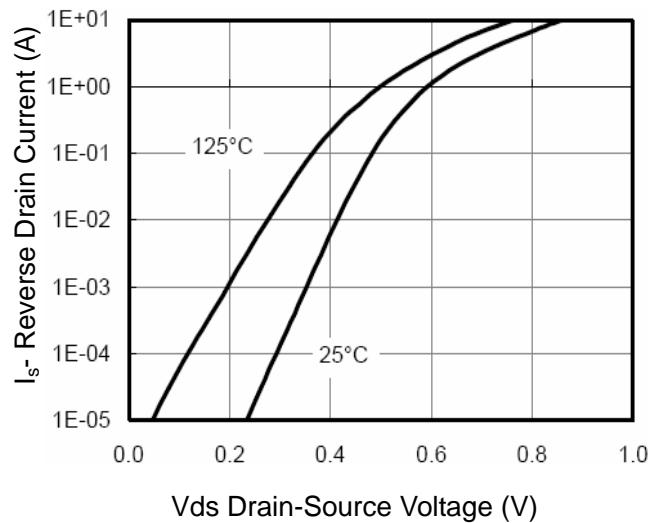


Figure 10 Capacitance vs V_{DS}

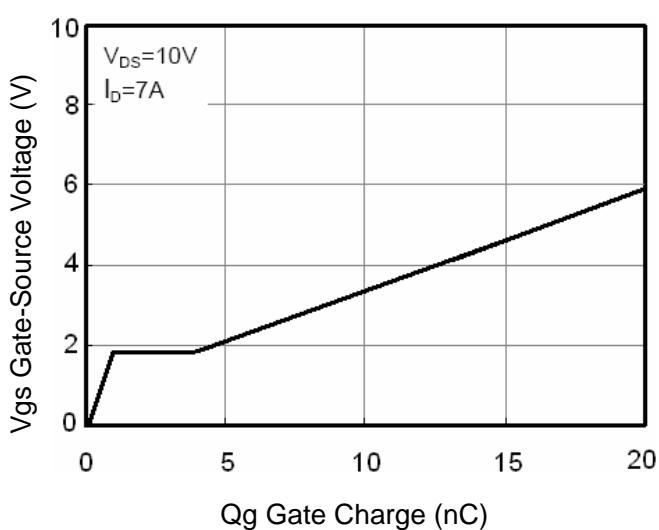


Figure 11 Gate Charge

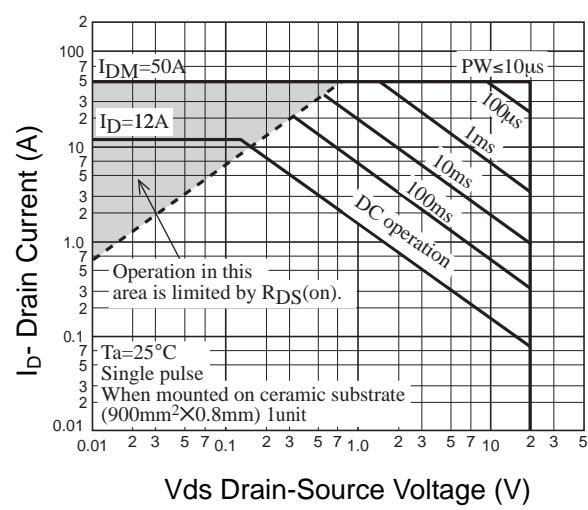
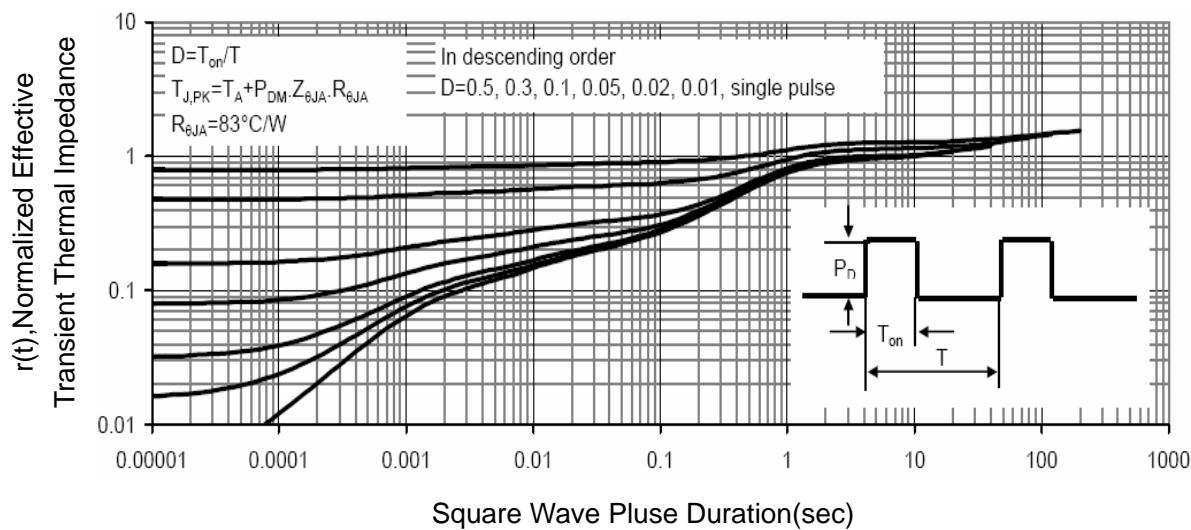
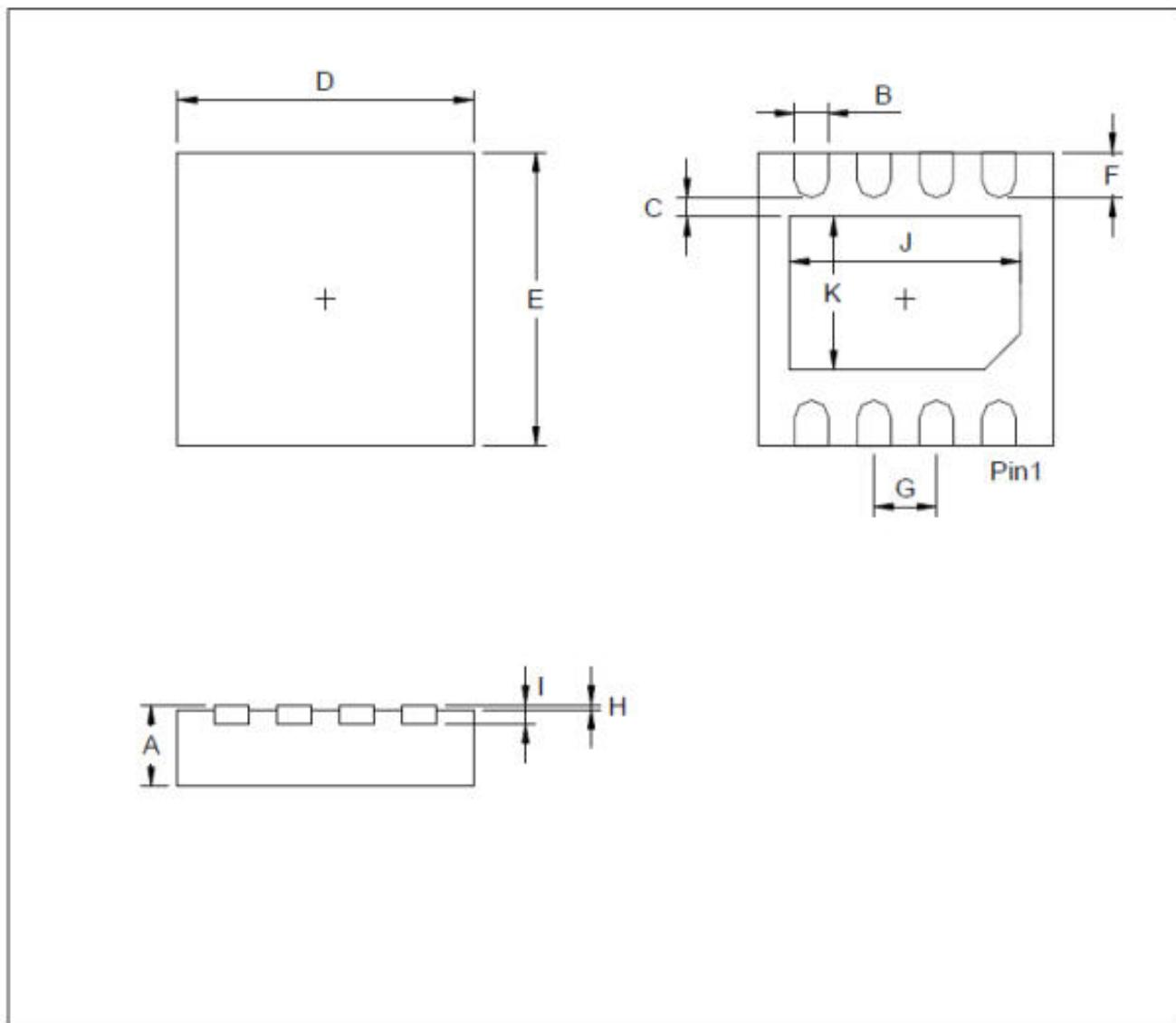


Figure 12 Safe Operation Area

**Figure 13 Normalized Maximum Transient Thermal Impedance**

Package Outline Dimensions : DFN3*3-8L



Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.7		0.8	I		0.203	
B	0.25		0.35	J	2.2		2.4
C	0.2			K	1.4		1.6
D	2.924		3.076				
E	2.924		3.076				
F	0.324		0.476				
G		0.65					
H	0		0.05				

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