FH8802G

N- Channel Enhancement Mode Power MOSFET

Description

The FH8802G uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

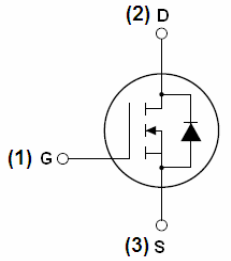
Application

- Power switching application
- DC/DC Converters In Computing
- Isolated DC/DC Converters In Telecom and Industrlal

General Features

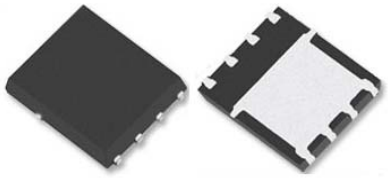
VDSS	ID	RDS(ON) (Typ)
30V	75A	2.2mΩ@VGS=10V

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Schematic diagram

Marking and pin Assignment



PDFN5X6-8L top and bottom view

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25℃	I_D	75	A
	T_C=100℃		57	
Pulsed Drain Current [C]		I_{DM}	165	
Continuous Drain Current	T_A=25℃	I_{DSM}	22	A
	T_A=70℃		18	
Avalanche Current [C]		I_{AS}	37	A
Avalanche energy L=0.1mH [C]		E_{AS}	225	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	V
Power Dissipation [B]	T_C=25℃	P_D	42	W
	T_C=100℃		23	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.5	W
	T_A=70℃		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16	25	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		41	60	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.1	3.2	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

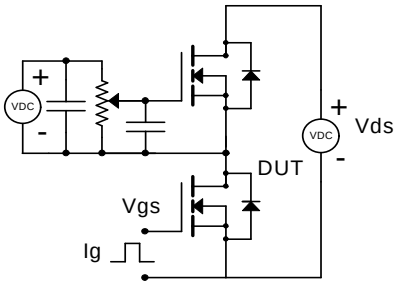
Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30	33		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.6	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=30A		2.2	2.9	mΩ
		T_J=125℃		3.2	4.2	
		V_{GS}=4.5V, I_D=20A		3.4	5.8	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		75		S
V_{SD}	Diode Forward Voltage	Is=1A,V_{GS}=0V		0.7	1.2	V
I_S	Maximum Body-Diode Continuous Current [G]				75	A
DYNAMIC PARAMETERS						
C_{ss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2930		pF
C_{oss}	Output Capacitance			500		pF
C_{rss}	Reverse Transfer Capacitance			431		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.9	2.1	2.9	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		38		nC
Q_g(4.5V)	Total Gate Charge			18		nC
Q_{gs}	Gate Source Charge			9		nC
Q_{gd}	Gate Drain Charge			13		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		26		ns
t_r	Turn-On Rise Time			24		ns
$t_{D(off)}$	Turn-Off DelayTime			91		ns
t_f	Turn-Off Fall Time			39		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs		42		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs		39		nC

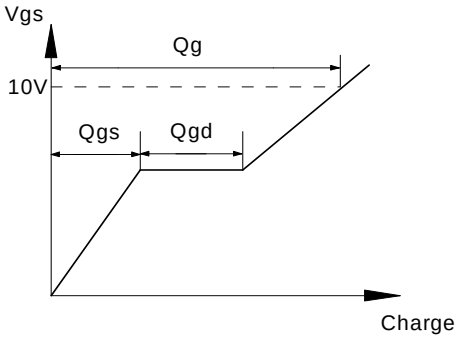
A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

Notes:

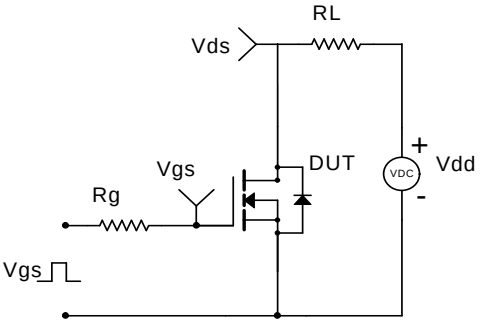
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω，I_{AS}=25A

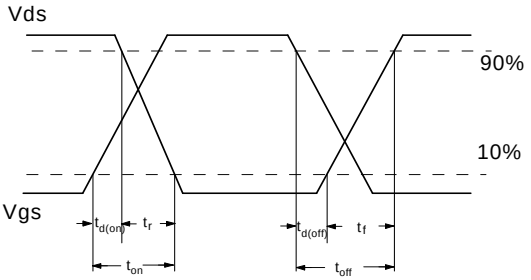
Gate Charge Test Circuit & Waveform



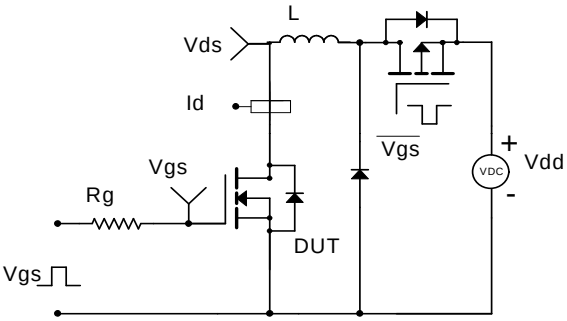


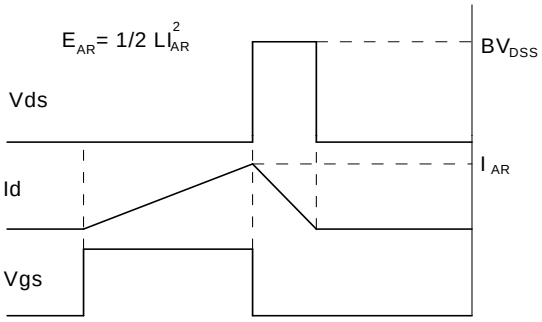
Resistive Switching Test Circuit & Waveforms



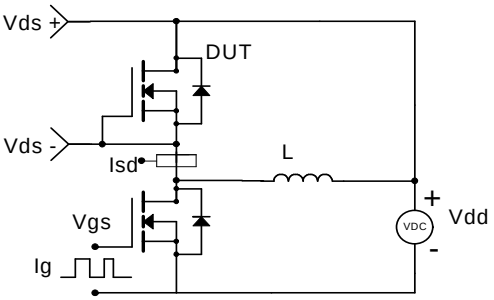


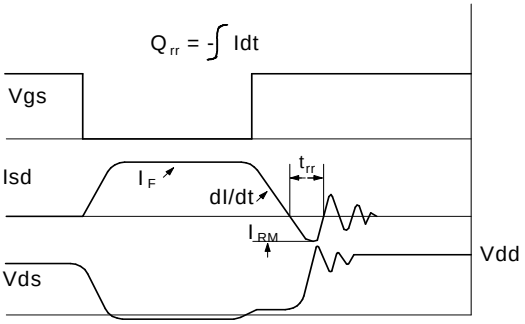
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





Typical Electrical and Thermal Characteristics (Curves)

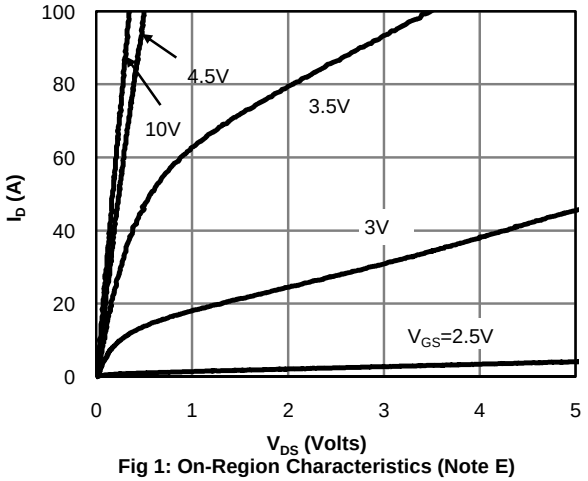


Fig 1: On-Region Characteristics (Note E)

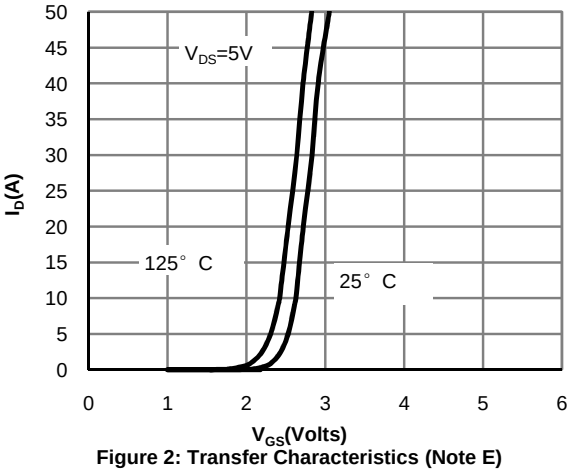


Figure 2: Transfer Characteristics (Note E)

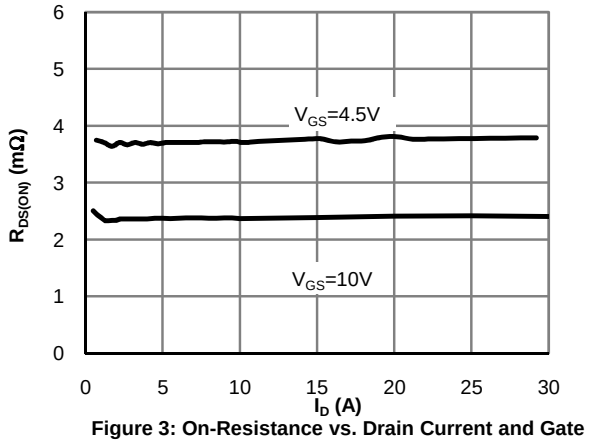


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

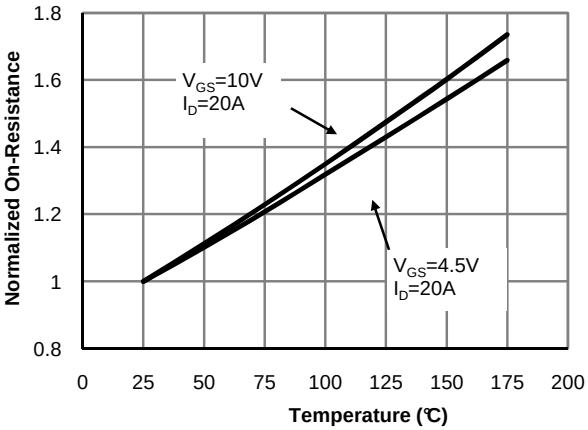


Figure 4: On-Resistance vs. Junction Temperature (Note E)

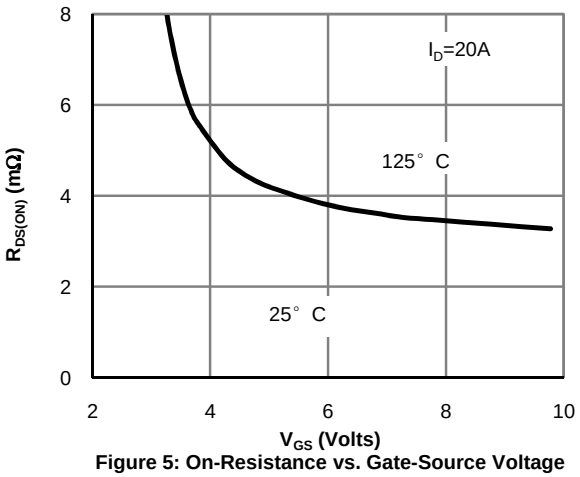


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

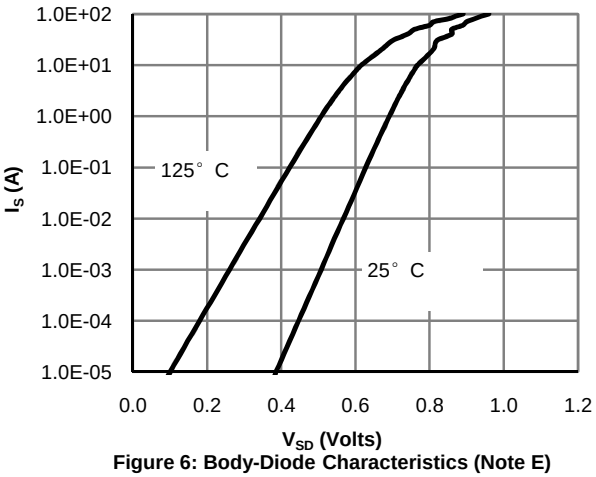


Figure 6: Body-Diode Characteristics (Note E)

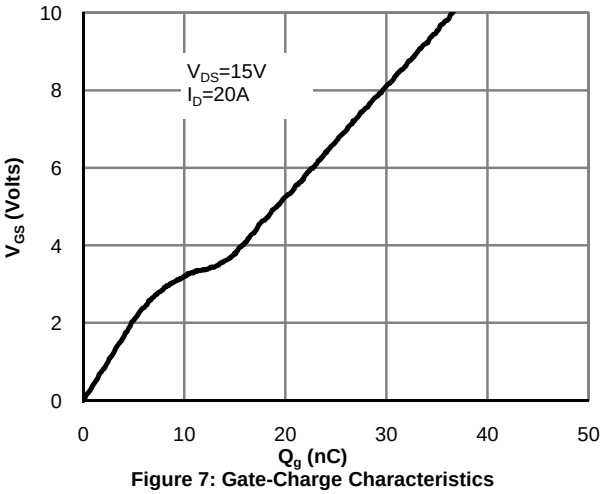


Figure 7: Gate-Charge Characteristics

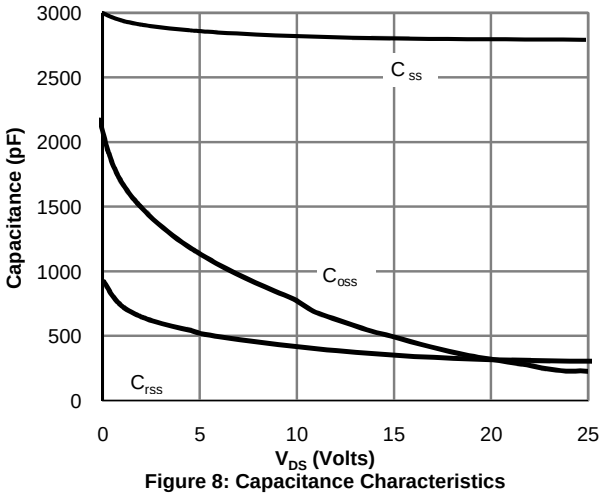


Figure 8: Capacitance Characteristics

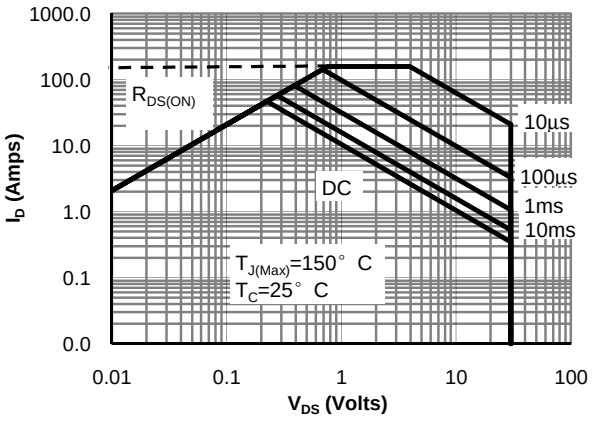


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

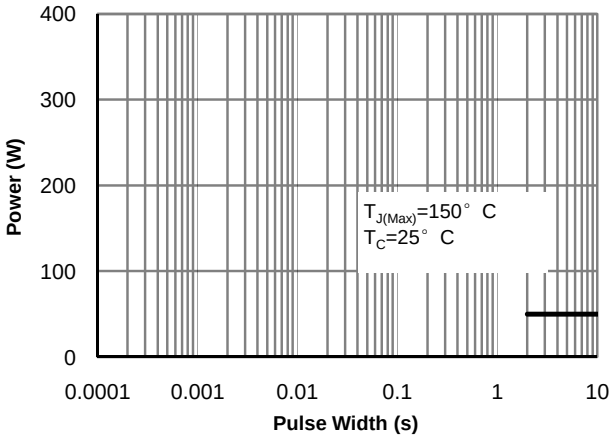


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

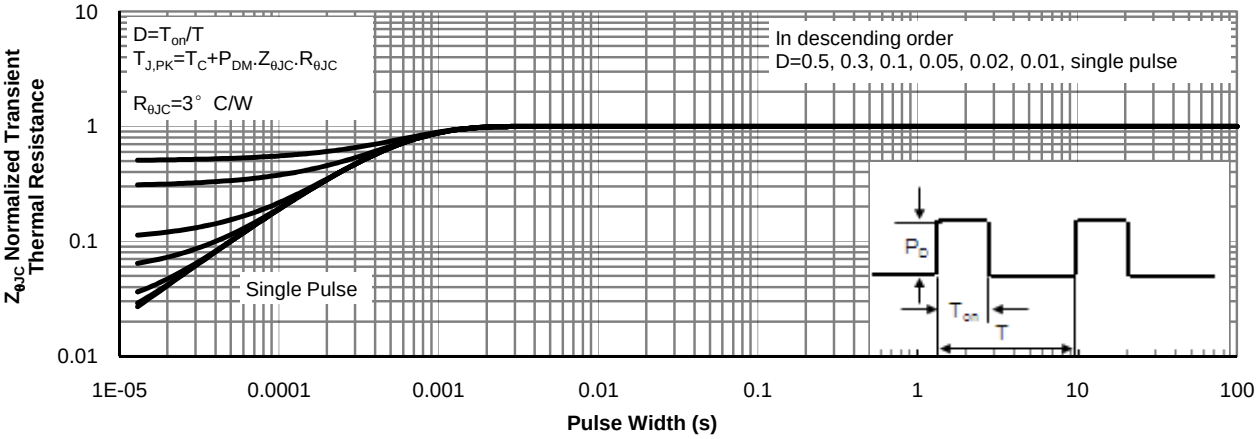


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

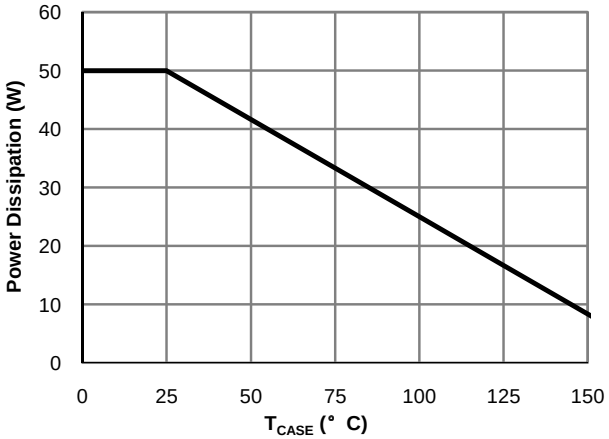


Figure 12: Power De-rating (Note F)

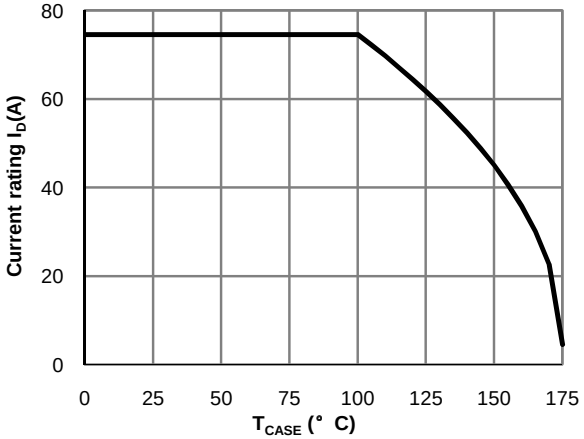


Figure 13: Current De-rating (Note F)

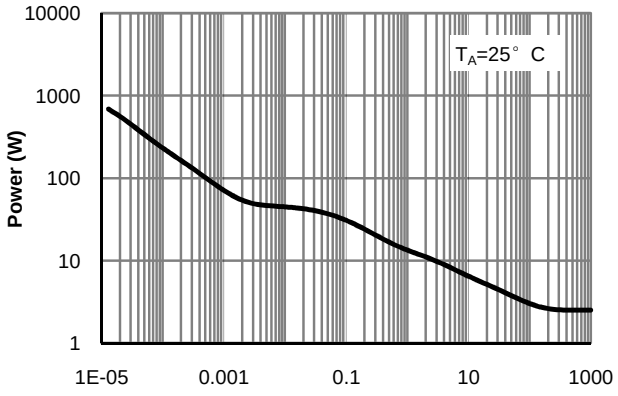


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

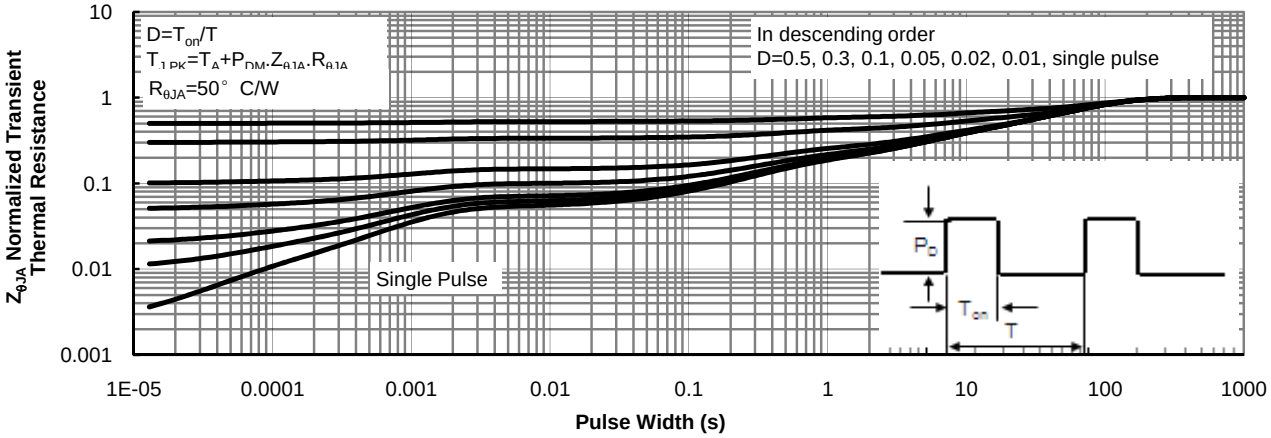
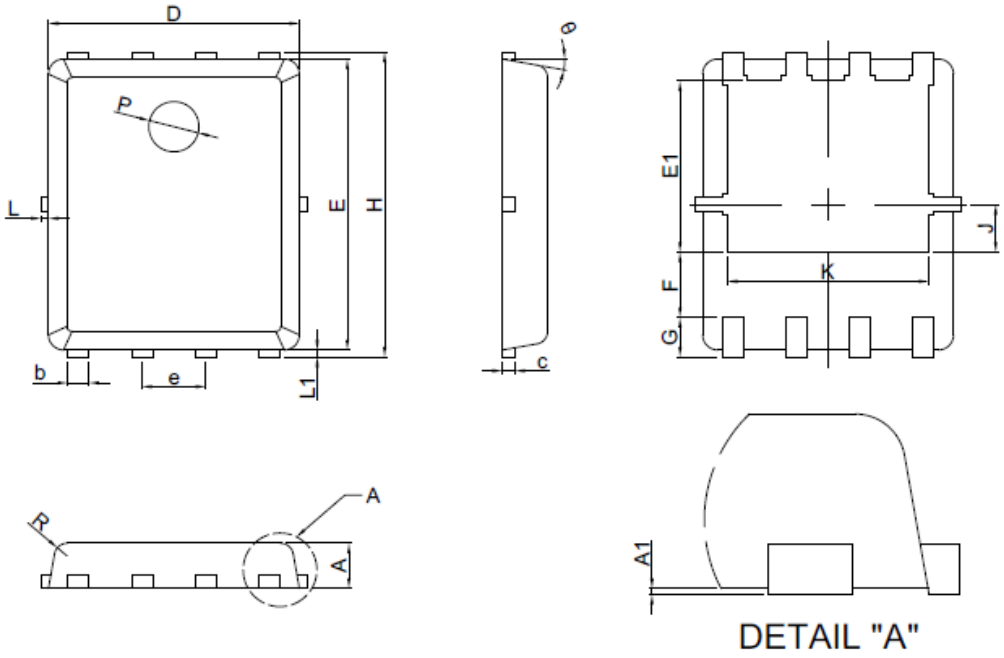


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Package Information：PDFN5x6-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.05
b	0.35	0.49
c	0.254REF	
D	4.80	5.20
F	1.40REF	
E	5.60	5.90
e	1.27BSC	
H	5.80	6.20
L1	0.10	0.18
G	0.60REF	
K	4.00REF	
L	-	0.15
J	0.95BSC	
P	1.00REF	
E1	3.40REF	
θ	6°	14°
R	0.25REF	

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