

FH8805

N-Channel Enhancement Mode Power MOSFET

◆ General Description

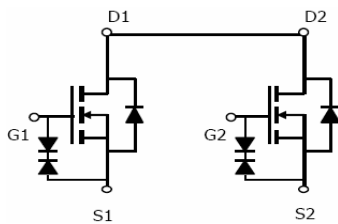
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

◆ Applications

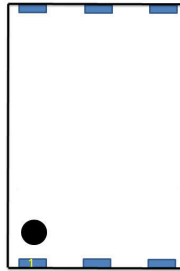
- Portable Equipment
- Battery Powered System
- Load Switch

◆ Features

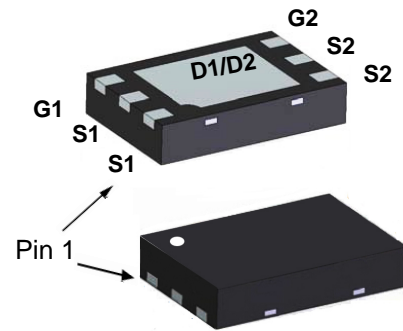
- $V_{DS}=20V$, $I_D=11A$
- $R_{DS(ON)} < 7.2m\Omega$ (MAX) @ $V_{GS}=4.5V$
 $R_{DS(ON)} < 8.2m\Omega$ (MAX) @ $V_{GS}=3.7V$
 $R_{DS(ON)} < 10.2m\Omega$ (MAX) @ $V_{GS}=2.5V$
- Fast switching
- G-S ESD protection diode embedded
- Green Device Available
- DFN2x3 package design



Schematic diagram



Marking and pin Assignment



DFN2x3-6L Pin assignment and Top / Bottom View

◆ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

| Parameter | Symbol | Maximum | Unit |
|--|----------------|----------------------------------|-------------|
| Drain-Source Voltage | V_{DS} | 20 | V |
| Gate-Source Voltage | V_{GS} | ± 12 | V |
| Continuous Drain Current | I_D | $T_A = 25^{\circ}C$ ¹ | 11 |
| | | $T_A = 70^{\circ}C$ ¹ | 8.8 |
| Pulse Drain Current ² | I_{DM} | 70 | A |
| Maximum Power Dissipation ¹ | P_D | $T_A = 25^{\circ}C$ | 1.56 |
| | | $T_A = 70^{\circ}C$ | 1 |
| Junction and Storage Temperature Range | T_J, T_{STG} | - 55 to 150 | $^{\circ}C$ |

◆ THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Maximum | Unit |
|----------------------------------|-----------------|---------|---------------|
| Junction-to-Ambient ¹ | $R_{\theta JA}$ | 80 | $^{\circ}C/W$ |

◆ ELECTRICAL CHARACTERISTICS (Tj=25°C Unless Otherwise Noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---------------|---|------|------|----------|------------|
| ◆ Static Parameters | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0V, I_D = 250 \mu A$ | 20 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS} = V_{DS}, I_D = 250 \mu A$ | 0.5 | 0.7 | 1.2 | V |
| Gate Leakage Current | I_{GSS} | $V_{DS} = 0V, V_{GS} = \pm 12V$ | | | ± 10 | μA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 18V, V_{GS} = 0V, T_j = 25^\circ C$ | | | 1 | μA |
| | | $V_{DS} = 18V, V_{GS} = 0V, T_j = 55^\circ C$ | | | 5 | |
| Forward Trans conductance | g_{fs} | $V_{DS} = 5V, I_D = 5.5A$ | | 36 | | S |
| Drain-Source On Resistance | $R_{DS(ON)}$ | $V_{GS} = 4.5V, I_D = 5.5A$ | 4.5 | 6 | 7.2 | m Ω |
| | | $V_{GS} = 4.0V, I_D = 5.5A$ | 4.8 | 6.2 | 7.5 | |
| | | $V_{GS} = 3.7V, I_D = 5.5A$ | 5 | 6.5 | 8.2 | |
| | | $V_{GS} = 3.1V, I_D = 5.5A$ | 5.3 | 7 | 9 | |
| | | $V_{GS} = 2.5V, I_D = 5.5A$ | 6 | 8.2 | 10.2 | |
| Diode Forward Voltage ² | V_{SD} | $I_S = 11A, V_{GS} = 0V, T_j = 25^\circ C$ | | | 1.2 | V |
| Maximum Body-Diode Continuous Current ¹ | | | | | 11 | A |
| ◆ Dynamic Parameters | | | | | | |
| Input Cap. | C_{iss} | $V_{DS} = 10V, V_{GS} = 0V, F = 1MHz$ | | 1767 | | pF |
| Output Cap. | C_{oss} | | | 164 | | |
| Reverse Transfer Cap. | C_{rss} | | | 155 | | |
| Total Gate Charge | Q_g | $V_{DS} = 16V, V_{GS} = 4.5V, I_D = 10A$ | | 23 | | nC |
| Gate-Source Charge | Q_{gs} | | | 3.5 | | |
| Gate-Drain Charge | Q_{gd} | | | 8.4 | | |
| Turn-On DelayTime | $T_{D(ON)}$ | $V_{DS} = 16V, V_{GS} = 4.5V, R_G = 6\Omega, I_D = 5.5A$ | | 10.2 | | nS |
| Turn-On Rise Time | t_r | | | 41 | | |
| Turn-Off DelayTime | $T_{D(OFF)}$ | | | 67 | | |
| Turn-Off Fall Time | t_f | | | 31 | | |
| Body Diode Reverse Recovery Time | t_{rr} | $V_{GS} = 0V, I_S = 1A, di/dt = 100A/\mu s, T_j = 25^\circ C$ | | 43 | | nS |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 8.9 | | nC |

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, t ≤ 10s.

2.The data tested by pulsed , pulse width ≤ 10us , duty cycle ≤ 1%

◆ TYPICAL CHARACTERISTICS

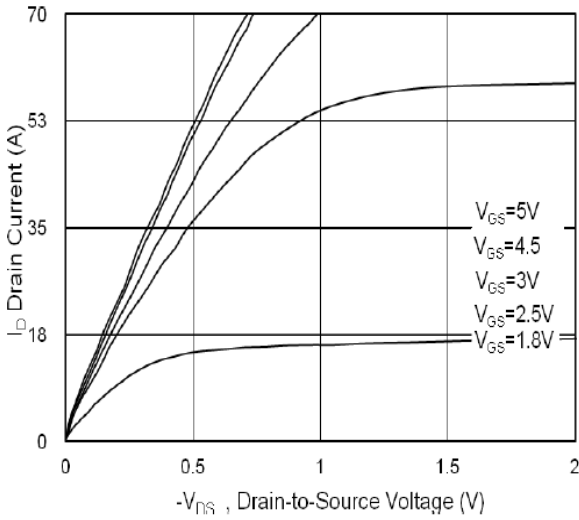


Fig.1 Typical Output Characteristics

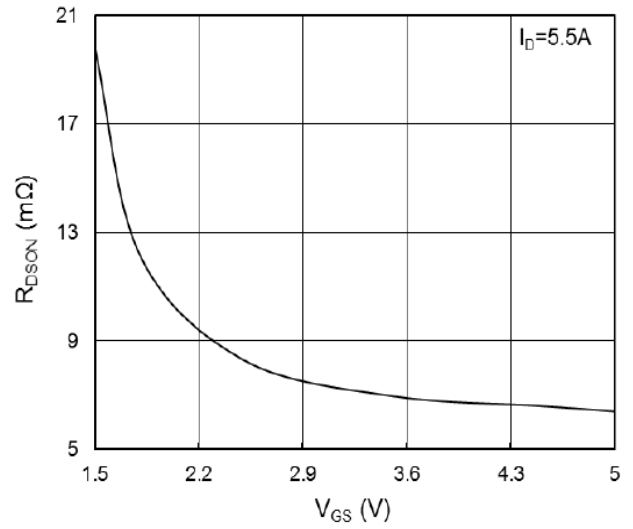


Fig.2 On-Resistance vs. Gate-Source

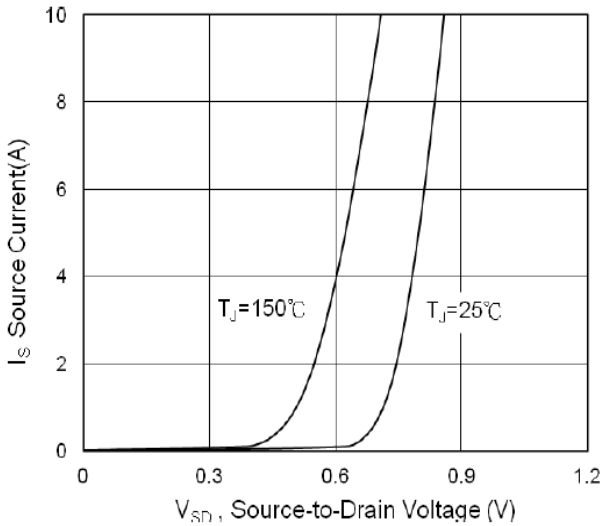


Fig.3 Forward Characteristics of Reverse

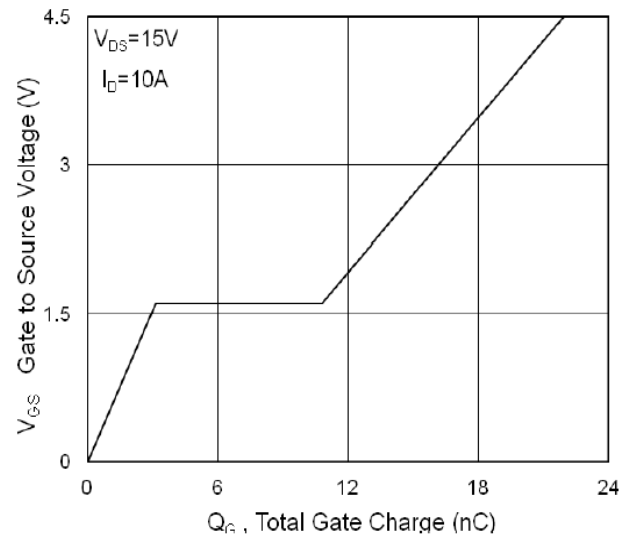


Fig.4 Gate-Charge Characteristics

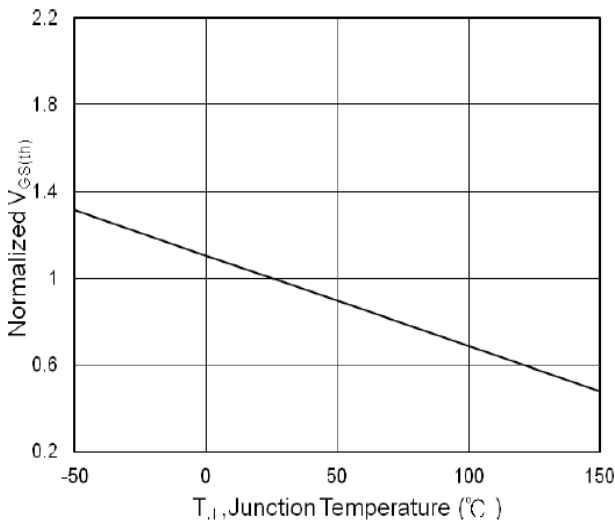


Fig.5 $V_{GS(th)}$ vs. T_J

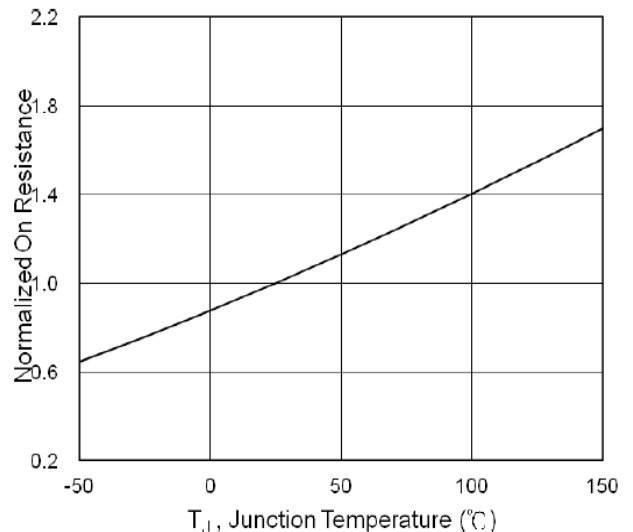


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

◆ TYPICAL CHARACTERISTICS

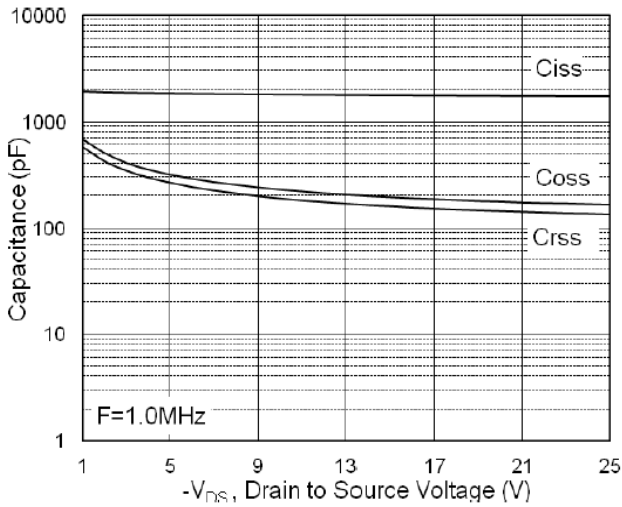


Fig.7 Capacitance

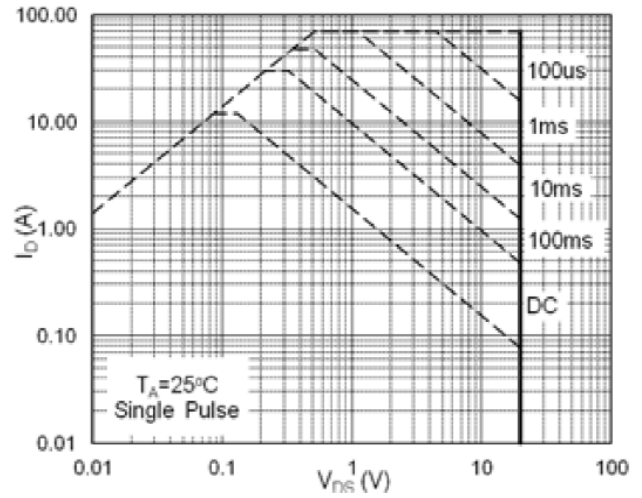


Fig.8 Safe Operating Area

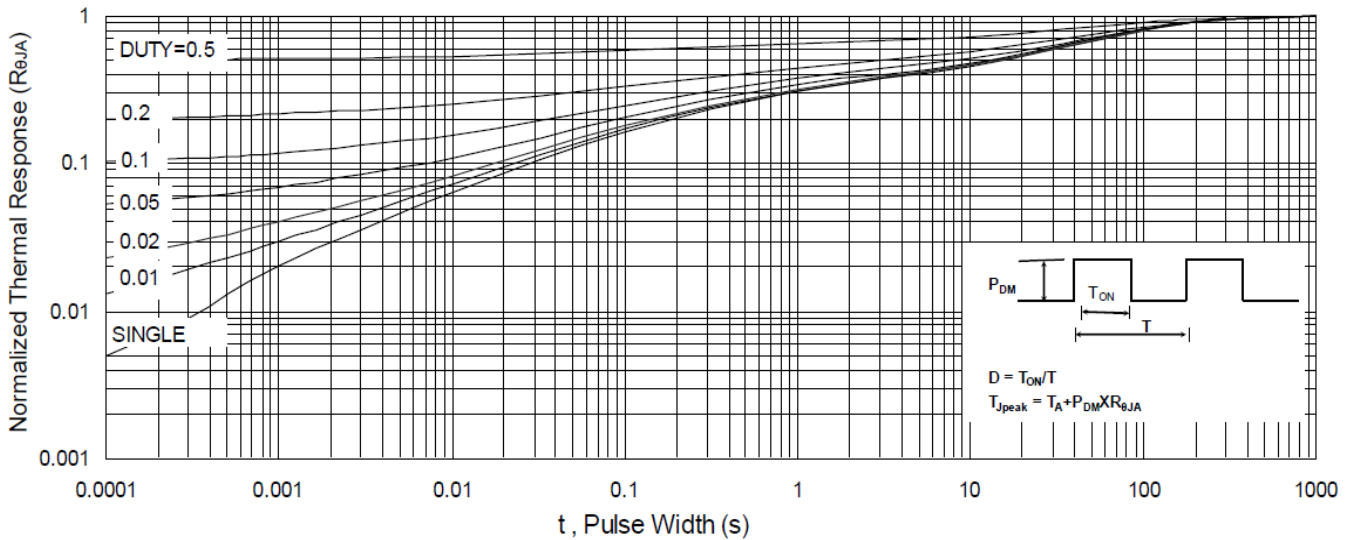


Fig.9 Normalized Maximum Transient Thermal Impedance

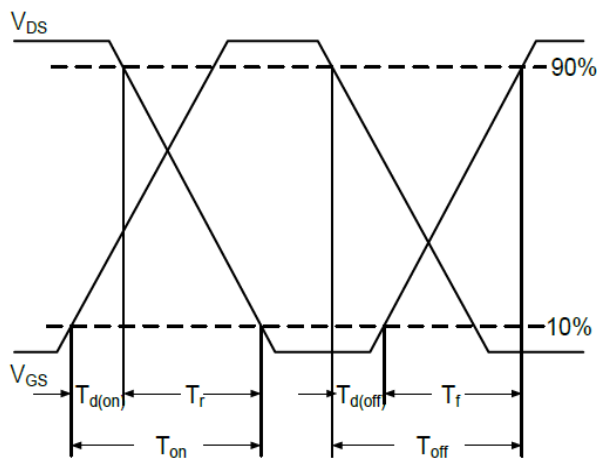


Fig.10 Switching Time Waveform

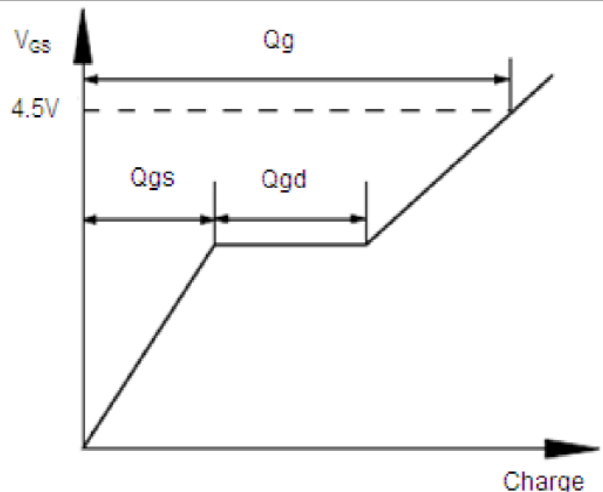
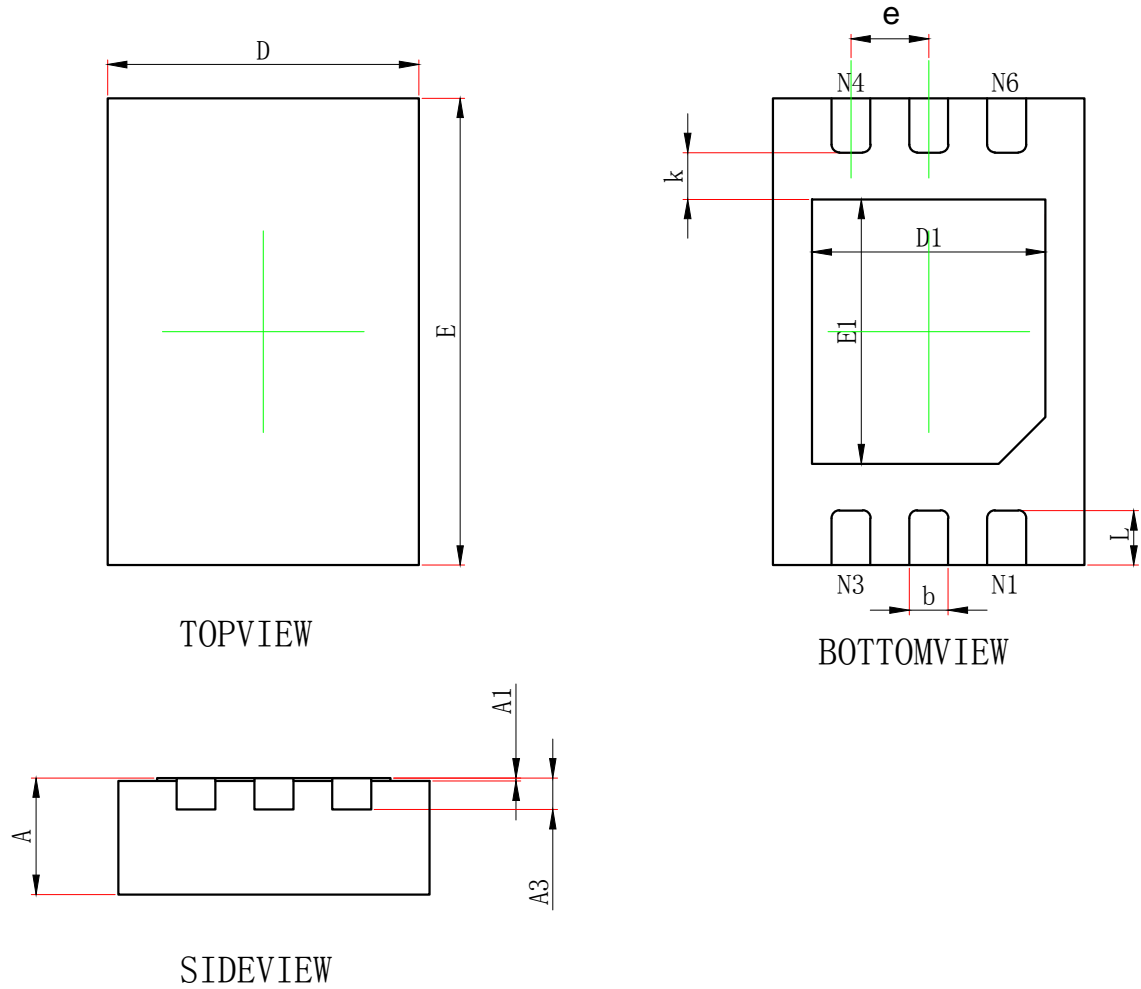


Fig.11 Gate Charge Waveform

Package Outline Dimensions : DFN2x3-6L



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF. | | 0.008REF. | |
| D | 1.950 | 2.050 | 0.077 | 0.081 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| D1 | 1.450 | 1.550 | 0.057 | 0.061 |
| E1 | 1.650 | 1.750 | 0.065 | 0.069 |
| k | 0.200MIN. | | 0.008MIN. | |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| e | 0.500TYP. | | 0.020TYP. | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

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