XD13085 DIP8 / XL13085 SOP8

General Description

The XD13085 +5.0V, ±15kV ESD-protected, RS-485/ RS-422 transceiver features one driver and one receiver. The device includes fail-safe circuitry, guaranteeing a logic-high receiver output when receiver inputs are open or shorted. The receiver outputs a logic-high if all transmitters on a terminated bus are disabled (high impedance). The XD13085 includes a hot-swap capability to eliminate false transitions on the bus during power-up or hot insertion.

The XD13085 features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

The XD13085 is ideal for half-duplex communications and it draws 1.2mA of supply current when unloaded or when fully loaded with the drivers disabled. The XD13085 has a 1/8-unit load receiver input imped - ance, allowing up to 256 transceivers on the bus.

The XD13085 is available in an 8-pin SO and PDIP packages.

Features

- **+5.0V Operation**
- **Extended ESD Protection for RS-485/RS-422 I/O Pins ±15kV Human Body Model**
- **True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility**
- **Hot-Swap Input Structures on DE and $\overline{RE}$**
- **Enhanced Slew-Rate Limiting Facilitates Error-Free Data Transmission**
- **Low-Current Shutdown Mode**
- **Allow Up to 256 Transceivers on the Bus**
- **Available in Industry-Standard 8-Pin SO and PDIP Packages**

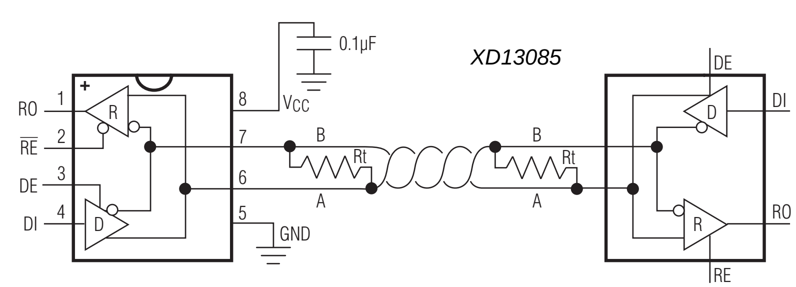
Applications

Utility Meters
Lighting Systems
Industrial Control
Telecom
Security Systems
Instrumentation
Profibus

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
13085	-40°C to +85°C	8 SO

Typical Operating Circuit



TYPICAL HALF-DUPLEX OPERATING CIRCUIT

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
Supply Voltage (V_{CC}).. +6V
Control Input Voltage ($\overline{RE}$, DE) ....-0.3V to +6V
Driver Input Voltage (DI) ....-0.3V to +6V
Driver Output Voltage (A, B) ....-8V to +13V
Receiver Input Voltage (A, B) ....-8V to +13V
Receiver Output Voltage (RO) .... -0.3V to (V_{CC} + 0.3V)
Driver Output Current.. ±250mA

Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.9mW/°C above +70°C) 471mW
Operating Temperature Range......................... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range.......................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
V_{CC} Supply-Voltage Range	V_{CC}		4.5		5.5	V
Differential Driver Output	V_{OD}	R_L = 100Ω (RS-422), Figure 1	3		V_{CC}	V
		R_L = 54Ω (RS-485), Figure 1	2		V_{CC}	
		No load			V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1 (Note 2)			0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1		$V_{CC}/2$	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 2)			0.2	V
Input-High Voltage	V_{IH}	DE, DI, $\overline{RE}$	3			V
Input-Low Voltage	V_{IL}	DE, DI, $\overline{RE}$			0.8	V
Input Hysteresis	V_{HYS}	DE, DI, $\overline{RE}$		100		mV
Input Current	I_{IN1}	DE, DI, $\overline{RE}$			±1	µA
Input Impedance First Transition at Power-Up	R_{PWUP}	V_{DE}, $V_{\overline{RE}}$ = $V_{\overline{RE}}$ = 2V	3.65		8.8	kΩ
Input Impedance on First Transition after POR Delay	R_{ft}	V_{DE} = $V_{\overline{RE}}$ = 2V	7		60	kΩ
Driver Short-Circuit Output Current	I_{OSD}	0 ≤ V_{OUT} ≤ +12V (Note 3)	40		250	mA
		-7V ≤ V_{OUT} ≤ V_{CC} (Note 3)	-250		-40	
Driver Short-Circuit Foldback Output Current	I_{OSDF}	(V_{CC} - 1V) ≤ V_{OUT} ≤ +12V (Note 3)	20			mA
		-7V ≤ V_{OUT} ≤ +1V (Note 3)			-20	
Thermal-Shutdown Threshold	T_{TS}			175		°C
Thermal-Shutdown Hysteresis	T_{TSH}			15		°C
Input Current (A and B)	$I_{A, B}$	V_{DE} = 0V, V_{CC} = 0V or V_{CC}; V_{IN} = +12V			125	µA
		V_{DE} = 0V, V_{CC} = 0V or V_{CC}; V_{IN} = -7V	-100			
RECEIVER						
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V	-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_A + V_B = 0V		15		mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RO Output-High Voltage	V_{OH}	I_O = -1mA	V_{CC} - 0.6		V	
RO Output-Low Voltage	V_{OL}	I_O = 1mA			0.4	V
Three-State Output Current at Receiver	I_{OZR}	$0 \le V_O \le V_{CC}$			≤ 1	µA
Receiver Input Resistance	R_{IN}	$-7V \le V_{CM} \le +12V$	96			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	$0V \le V_{RO} \le V_{CC}$			≤ 110	mA
SUPPLY CURRENT						
Supply Current	I_{CC}	No load, $V_{\overline{RE}}$ = 0V, DE = V_{CC}		1.2	1.8	mA
		No load, $\overline{RE}$ = V_{CC}, DE = V_{CC}		1.2	1.8	
		No load, $V_{\overline{RE}}$ = 0V, V_{DE} = 0V		1.2	1.8	
Supply Current in Shutdown Mode	I_{SHDN}	$\overline{RE}$ = V_{CC}, V_{DE} = 0V		2.8	10	µA
ESD PROTECTION						
ESD Protection for A and B		Human Body Model		±15		kV
		Contact Discharge IEC 61000-4-2, level 4		±8		
		Air-Gap Discharge IEC 61000-4-2		±15		

DRIVER SWITCHING CHARACTERISTICS WITH INTERNAL SRL (500kbps)

(V_{CC} = +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{DPLH}	C_L = 50pF, R_L = 54Ω, Figures 2 and 3	200		1000	ns
	t_{DPHL}		200		1000	
Driver Differential Output Rise or Fall Time	t_R , t_F	C_L = 50pF, R_L = 54Ω, Figures 2 and 3	250		900	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	C_L = 50pF, R_L = 54Ω, Figures 2 and 3			140	ns
Maximum Data Rate			500			kbps
Driver Enable to Output High	t_{DZH}	Figure 4			2500	ns
Driver Enable to Output Low	t_{DZL}	Figure 5			2500	ns
Driver Disable Time from Low	t_{DLZ}	Figure 5			100	ns
Driver Disable Time from High	t_{DHZ}	Figure 4			100	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figure 4			5500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figure 5			5500	ns
Time to Shutdown	t_{SHDN}		50	340	700	ns

RECEIVER SWITCHING CHARACTERISTICS WITH INTERNAL SRL (500kbps)

(V_{CC} = +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Propagation Delay	t_{RPLH}	C_L = 15pF, Figures 6 and 7			200	ns
	t_{RPHL}				200	
Receiver Output Skew $\lvert t_{RPLH} - t_{RPHL} \rvert$	t_{RSKEW}	C_L = 15pF, Figures 6 and 7			30	ns
Maximum Data Rate			500			kbps
Receiver Enable to Output Low	t_{RZL}	Figure 8			50	ns
Receiver Enable to Output High	t_{RZH}	Figure 8			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 8			50	ns
Receiver Disable Time from High	t_{RHZ}	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figure 8			5500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figure 8			5500	ns
Time to Shutdown	t_{SHDN}		50	340	700	ns

Note 1: All currents into the device are positive. All currents out of the device are negative. All voltages are referred to device ground, unless otherwise noted.

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 3: The short-circuit output current applies to peak current just prior to foldback current limiting. The short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

Test Circuits and Waveforms

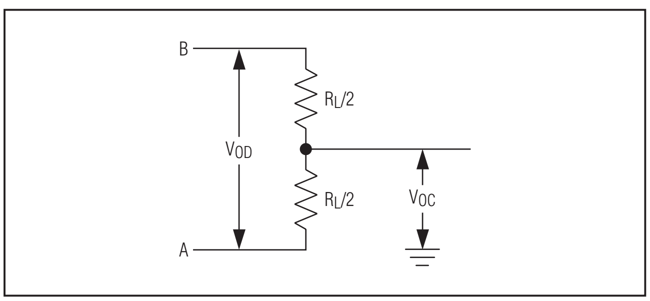


Figure 1. Driver DC Test Load

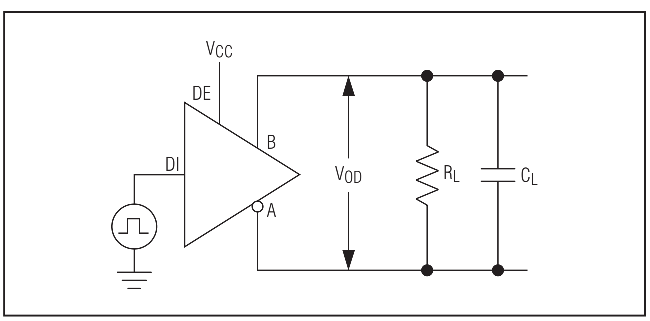


Figure 2. Driver Timing Test Circuit

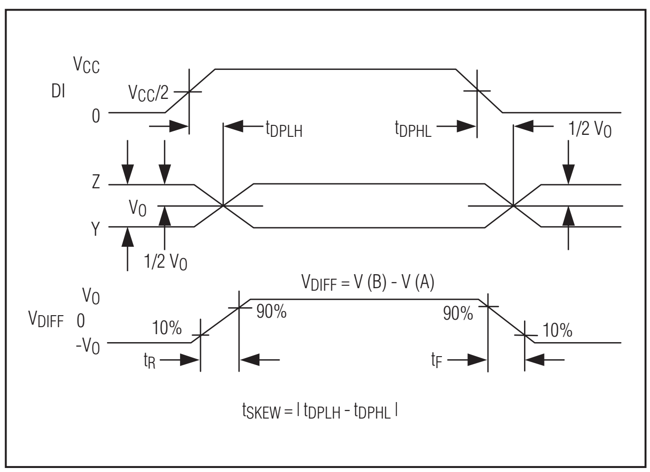


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

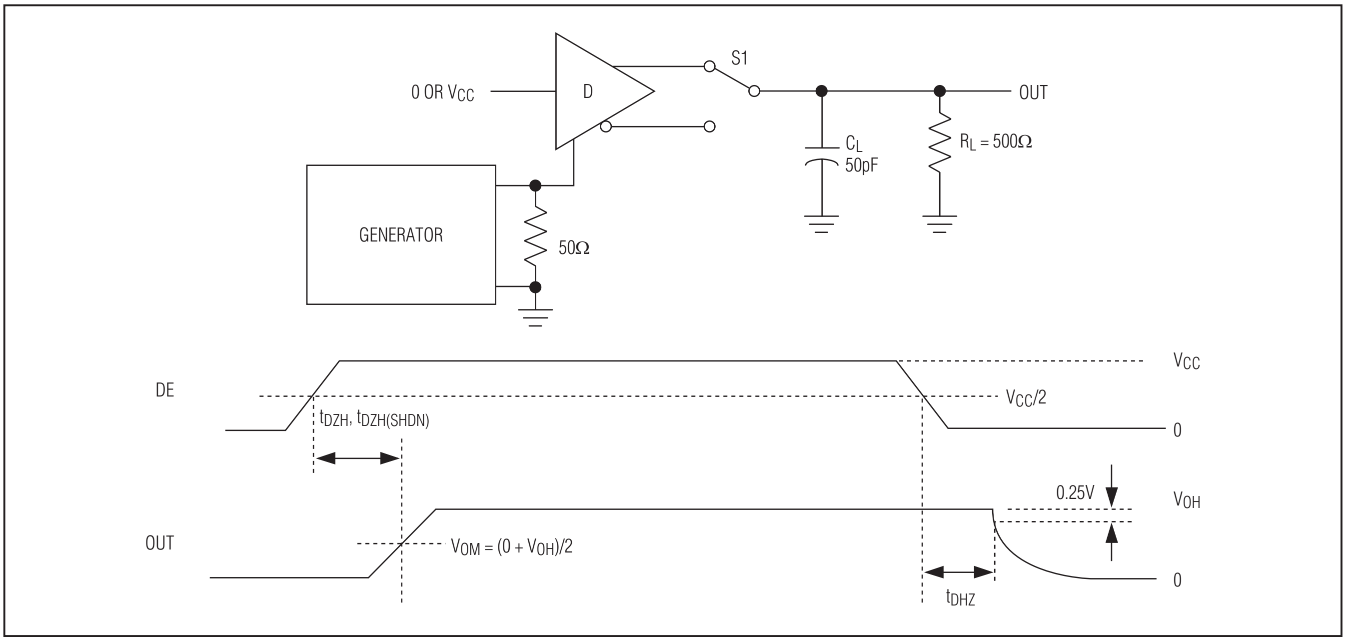


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)

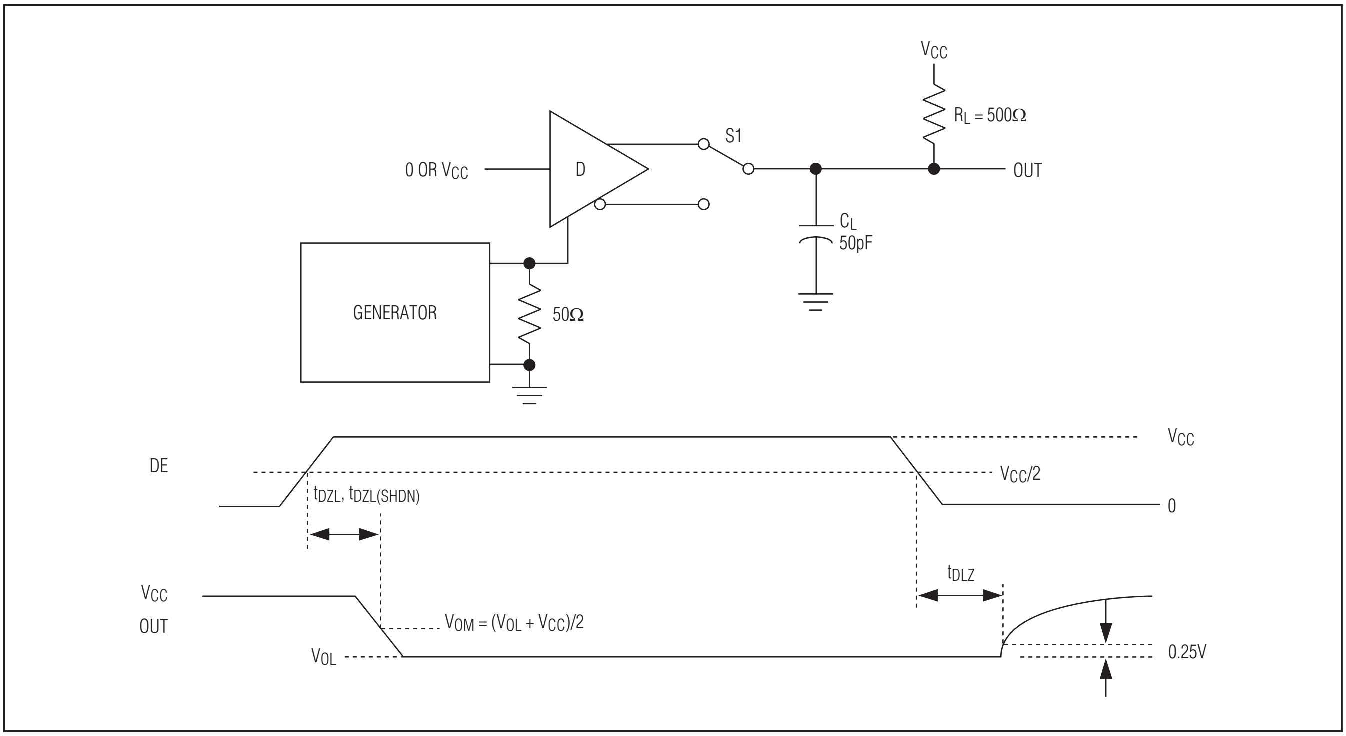


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ}, $t_{DLZ(SHDN)}$)

Test Circuits and Waveforms (continued)

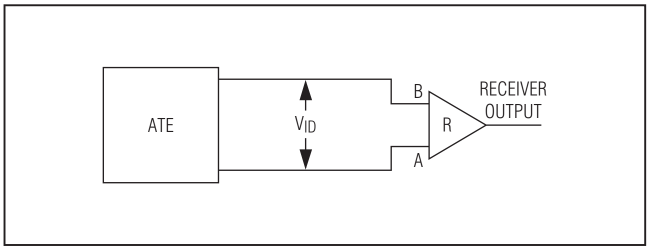


Figure 6. Receiver Propagation Delay Test Circuit

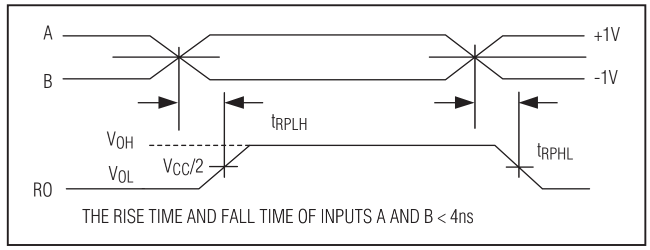


Figure 7. Receiver Propagation Delays

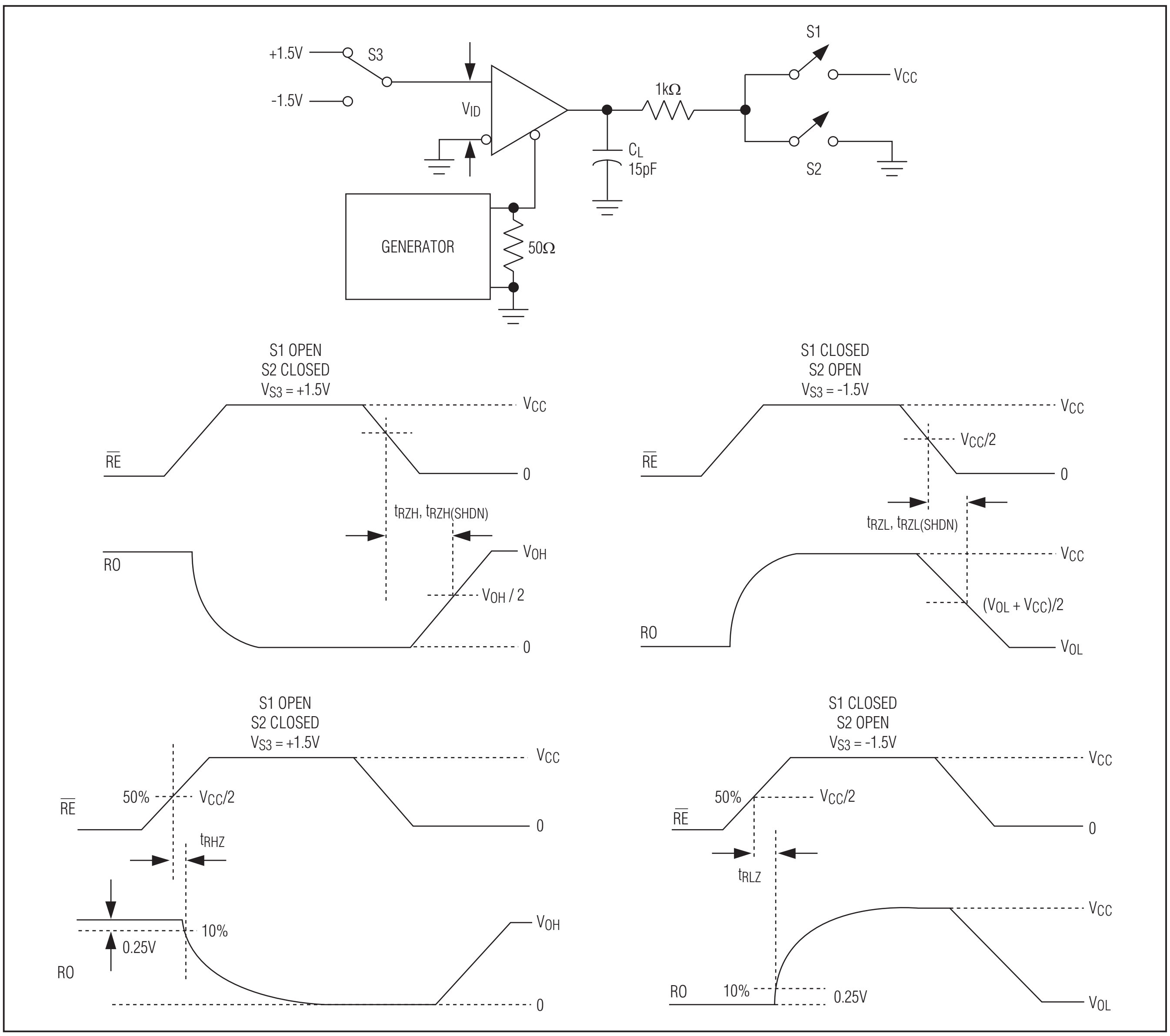
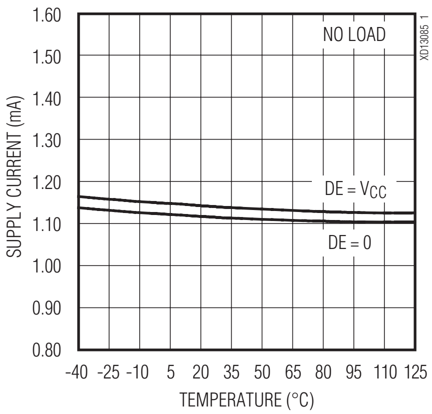


Figure 8. Receiver Enable and Disable Times

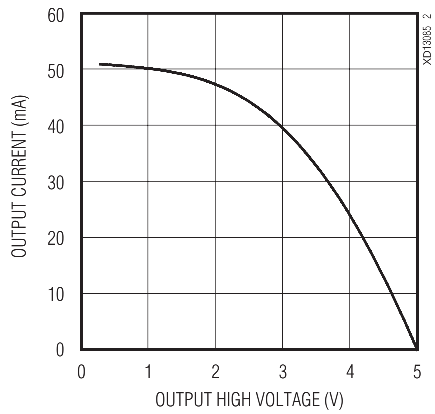
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

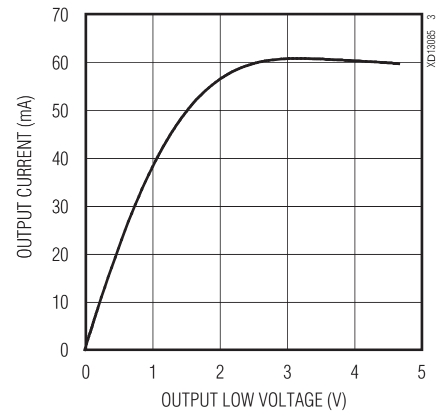
SUPPLY CURRENT vs. TEMPERATURE



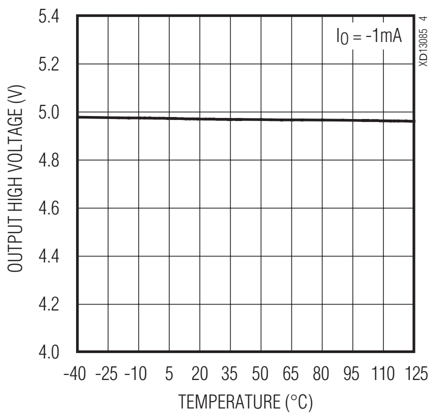
OUTPUT CURRENT vs. RECEIVER OUTPUT-HIGH VOLTAGE



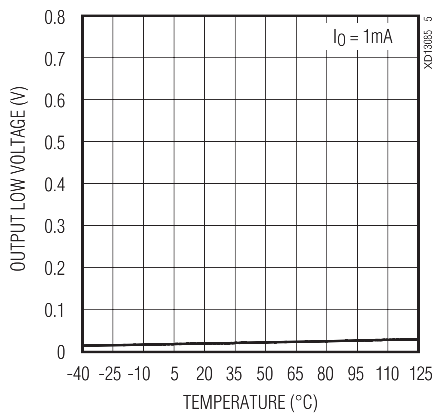
OUTPUT CURRENT vs. RECEIVER OUTPUT-LOW VOLTAGE



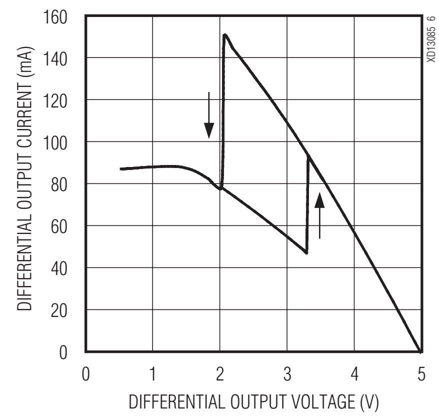
RECEIVER OUTPUT-HIGH VOLTAGE vs. TEMPERATURE



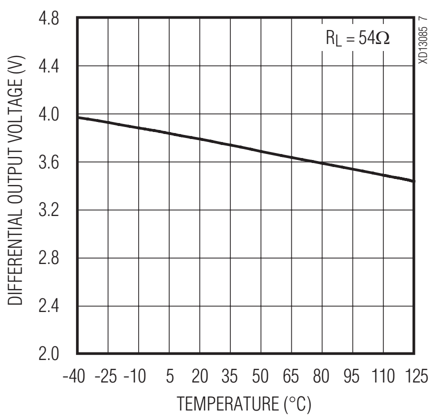
RECEIVER OUTPUT-LOW VOLTAGE vs. TEMPERATURE



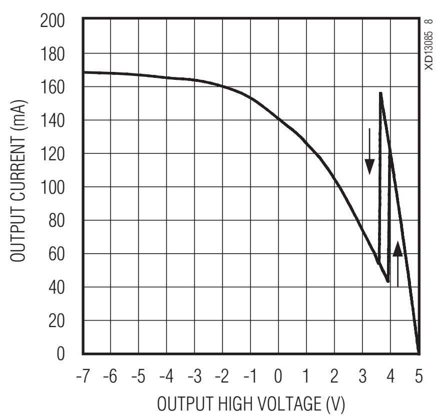
DRIVER DIFFERENTIAL OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



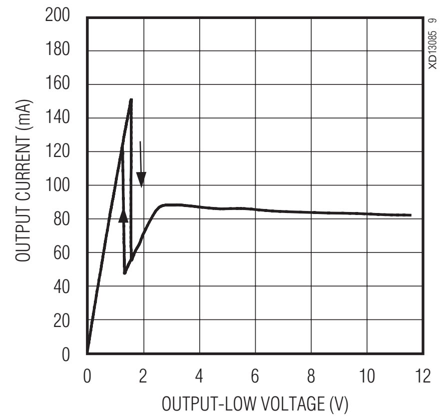
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



OUTPUT CURRENT vs. TRANSMITTER OUTPUT-HIGH VOLTAGE



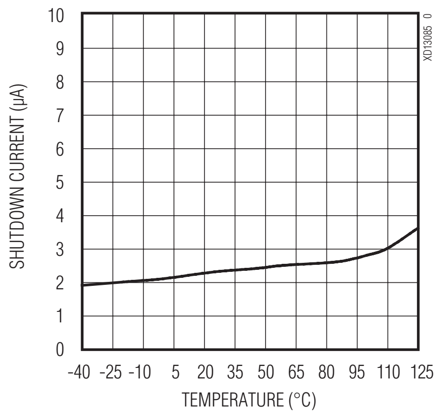
OUTPUT CURRENT vs. TRANSMITTER OUTPUT-LOW VOLTAGE



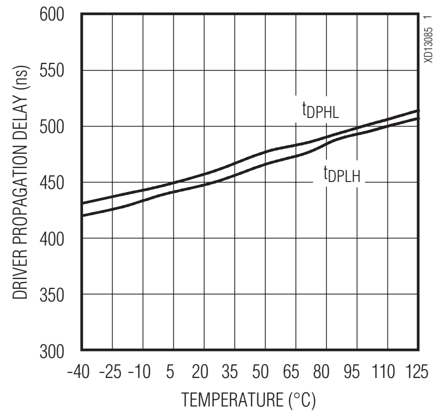
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

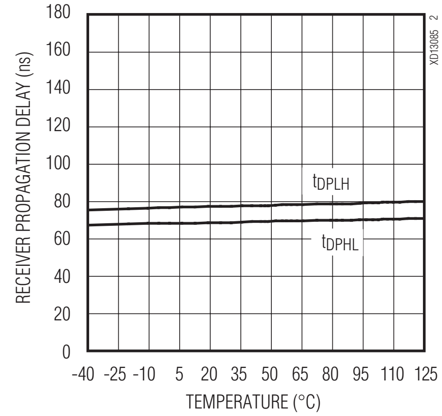
SHUTDOWN CURRENT vs. TEMPERATURE



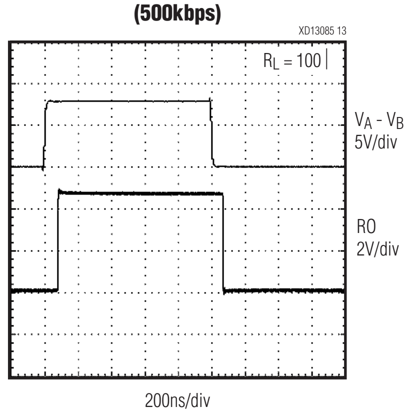
DRIVER PROPAGATION DELAY vs. TEMPERATURE (500kbps)



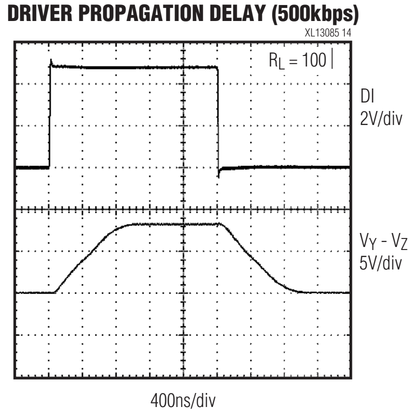
RECEIVER PROPAGATION DELAY vs. TEMPERATURE (500kbps)



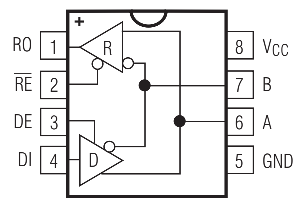
RECEIVER PROPAGATION DELAY (500kbps)



DRIVER PROPAGATION DELAY (500kbps)



Pin Configuration



SO

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. When $\overline{RE}$ is low and if (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input (see the *Hot-Swap Capability* section for details).
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the *Hot-Swap Capability* section for details).
4	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces noninverting output high and inverting output low.
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	V_{CC}	Positive Supply V_{CC} = +5.0V ±10%. Bypass V_{CC} to GND with a 0.1µF capacitor.

Function Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUTS
$\overline{RE}$	DE	A-B	RO
0	X	≥ -50mV	1
0	X	≤ -200mV	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Detailed Description

The XD13085 high-speed transceiver for RS-485/ RS-422 communication contains one driver and one receiver. This device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *Fail-Safe* section). The XD13085 also features a hot-swap capability allowing line insertion without erroneous data transfer (see the *Hot-Swap Capability* section). The XD13085 features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

The XD13085 is a half-duplex transceiver and operates from a single +5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

Fail-Safe

The XD13085 guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver threshold of the XD13085, this results in a logic-high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of these devices to a defined logic level. Leakage currents up to ±10μA from the high-impedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver.

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

The enable inputs feature hot-swap capability. At the input there are two nMOS devices, M1 and M2 (Figure 9). When V_{CC} ramps from zero, an internal 7μs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 500μA current sink, and M1, a 100μA current sink, pull DE to GND through a 5kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 7μs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance

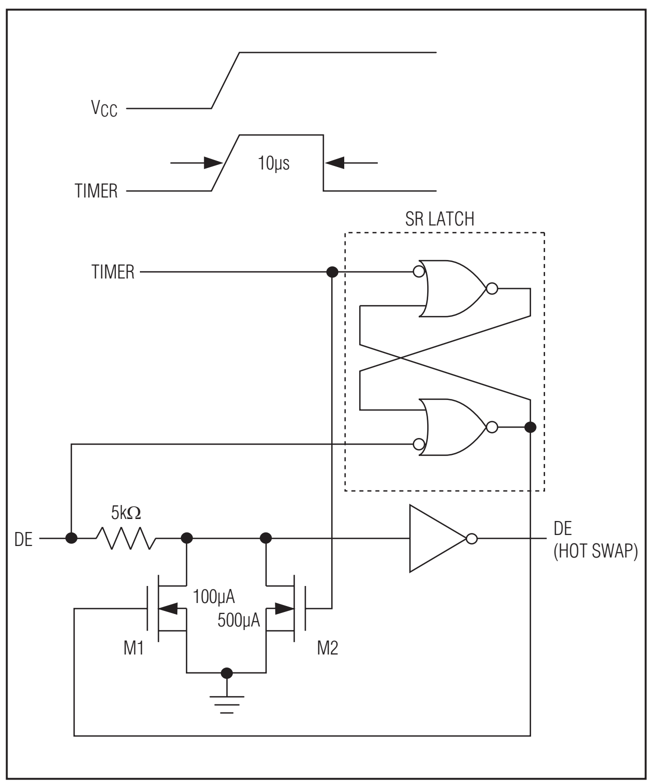


Figure 9. Simplified Structure of the Driver Enable Pin (DE)

CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{RE}$ there is a complementary circuit employing two pMOS devices pulling $\overline{RE}$ to V_{CC}.

±30kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver input of the XD13085 have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the XD13085 keeps working without latchup or damage.

ESD protection can be tested in various ways. The transmitter output and receiver input of the XD13085 are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2
- ±15kV using the Air-Gap Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The XD13085 helps you design equipment to meet IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 61000-4-2 model, and Figure 10d shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly. Of course, all pins require this protection, not just RS-485 inputs and outputs.

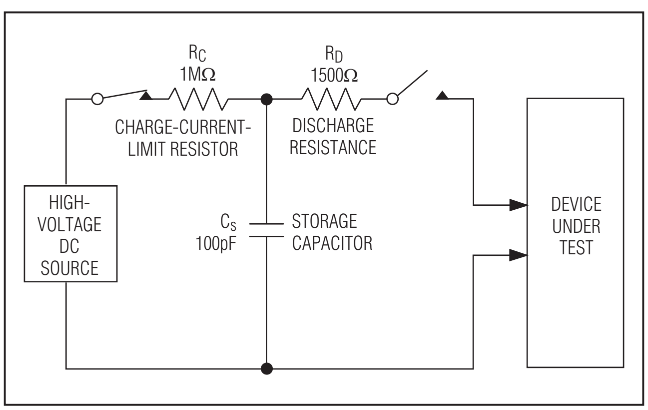


Figure 10a. Human Body ESD Test Model

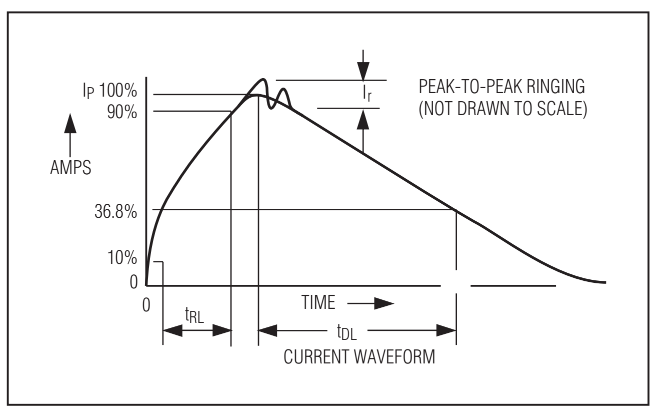


Figure 10b. Human Body Current Waveform

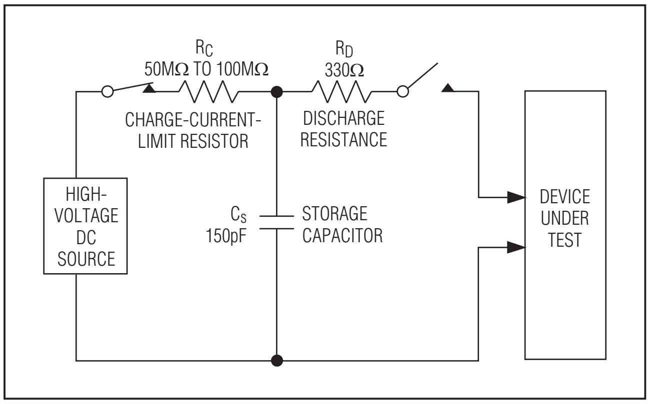


Figure 10c. IEC 61000-4-2 ESD Test Model

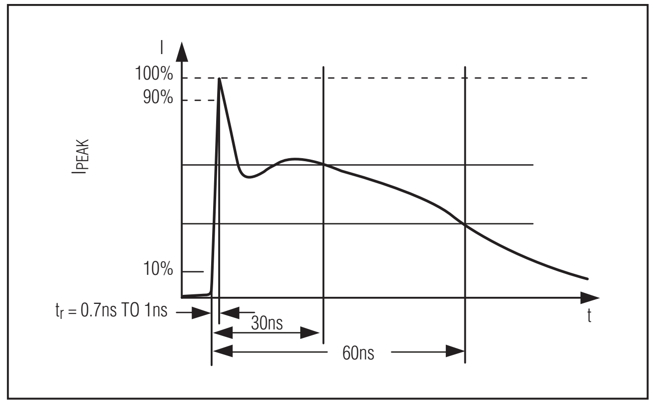


Figure 10d. IEC 61000-4-2 ESD Generator Current Waveform

Applications Information

The standard RS-485 receiver input impedance is 12kΩ (1-unit load), and the standard driver can drive up to 32-unit loads. The XD13085 has a 1/8-unit load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of the XD13085, as well as other RS-485 transceivers with a total of 32-unit loads or fewer, can be connected to the line.

Reduced EMI and Reflections

The XD13085 features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. In shutdown, the devices typically draw only 2.8µA of supply current.

$\overline{RE}$ and DE can be driven simultaneously; the devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 700ns, the devices are guaranteed to enter shutdown.

Enable times t_{ZH} and t_{ZL} (see the *Switching Characteristics* section) assume the devices were not in a low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ assume the devices were in shutdown state. It takes drivers and receivers longer to become enabled from low-power shutdown mode ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +175°C (typ).

Line Length

The RS-485/RS-422 standard covers line lengths up to 4000ft. For line lengths greater than 4000ft, it may be necessary to implement a line repeater.

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