

The XD14016 quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each XD14016 consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise – $12 \text{ nV}/\sqrt{\text{Cycle}}$, $f \geq 1.0 \text{ kHz}$ typical
- Pin-for-Pin Replacements for XD4016, XD4066 (Note Improved Transfer Characteristic Design Causes More Parasitic Coupling Capacitance than XD4016)
- For Lower R_{ON} , Use The HC4016 High-Speed CMOS Device or The XD14016
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient) per Control Pin	± 10	mA
I_{SW}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

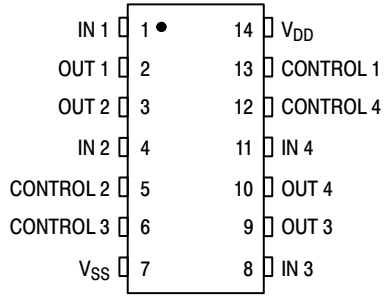
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

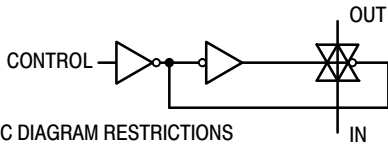
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



LOGIC DIAGRAM

(1/4 OF DEVICE SHOWN)

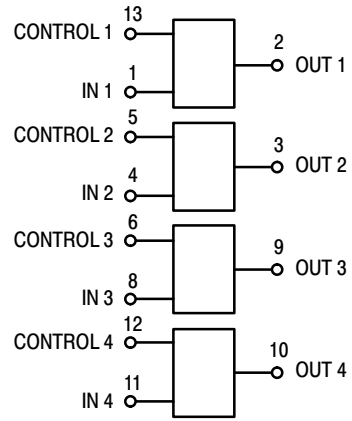


LOGIC DIAGRAM RESTRICTIONS

$$V_{SS} \leq V_{in} \leq V_{DD}$$

$$V_{SS} \leq V_{out} \leq V_{DD}$$

BLOCK DIAGRAM



$V_{DD} = \text{PIN } 14$
 $V_{SS} = \text{PIN } 7$

Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Input Voltage Control Input	1	V_{IL}	5.0	-	-	-	1.5	0.9	-	-	Vdc
			10	-	-	-	1.5	0.9	-	-	
			15	-	-	-	1.5	0.9	-	-	
		V_{IH}	5.0	-	-	3.0	2.0	-	-	-	Vdc
			10	-	-	8.0	6.0	-	-	-	
			15	-	-	13	11	-	-	-	
Input Current Control	-	I_{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc
Input Capacitance Control Switch Input Switch Output Feed Through	-	C_{in}	-	-	-	-	5.0	-	-	-	pF
			-	-	-	-	5.0	-	-	-	
			-	-	-	-	5.0	-	-	-	
			-	-	-	-	0.2	-	-	-	
Quiescent Current (Per Package) (Note 3)	2,3	I_{DD}	5.0	-	0.25	-	0.0005	0.25	-	7.5	µAdc
			10	-	0.5	-	0.0010	0.5	-	15	
			15	-	1.0	-	0.0015	1.0	-	30	
"ON" Resistance ($V_C = V_{DD}$, $R_L = 10\text{ k}\Omega$) ($V_{in} = +10\text{ Vdc}$) ($V_{in} = +0.25\text{ Vdc}$) $V_{SS} = 0\text{ Vdc}$ ($V_{in} = +5.6\text{ Vdc}$) ($V_{in} = +15\text{ Vdc}$) ($V_{in} = +0.25\text{ Vdc}$) $V_{SS} = 0\text{ Vdc}$ ($V_{in} = +9.3\text{ Vdc}$)	4,5,6	R_{ON}	-	-	600	-	260	660	-	840	Ω
			-	-	600	-	310	660	-	840	
			10	-	600	-	310	660	-	840	
			-	-	360	-	260	400	-	520	
			-	-	360	-	260	400	-	520	
			15	-	360	-	300	400	-	520	
Δ "ON" Resistance Between any 2 circuits in a common package ($V_C = V_{DD}$) ($V_{in} = +5.0\text{ Vdc}$, $V_{SS} = -5.0\text{ Vdc}$) ($V_{in} = +7.5\text{ Vdc}$, $V_{SS} = -7.5\text{ Vdc}$)	-	ΔR_{ON}	-	-	-	-	-	-	-	-	Ω
			5.0	-	-	-	15	-	-	-	
			7.5	-	-	-	10	-	-	-	
Input/Output Leakage Current ($V_C = V_{SS}$) ($V_{in} = +7.5$, $V_{out} = -7.5\text{ Vdc}$) ($V_{in} = -7.5$, $V_{out} = +7.5\text{ Vdc}$)	-	-	7.5	-	±0.1	-	±0.0015	±0.1	-	±1.0	µAdc
			7.5	-	±0.1	-	±0.0015	±0.1	-	±1.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

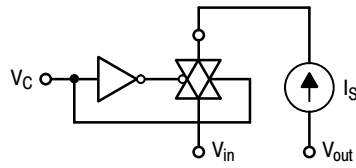
2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

ELECTRICAL CHARACTERISTICS (Note 4) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	V _{DD} Vdc	Min	Typ (Note 5)	Max	Unit
Propagation Delay Time ($V_{SS} = 0 \text{ Vdc}$) V_{in} to V_{out} ($V_C = V_{DD}$, $R_L = 10 \text{ k}\Omega$)	7	t_{PLH} ,	5.0	–	15	45	ns
		t_{PHL}	10 15	– –	7.0 6.0	20 15	
Control to Output ($V_{in} \leq 10 \text{ Vdc}$, $R_L = 10 \text{ k}\Omega$)	8	t_{PHZ} ,	5.0	–	34	120	ns
		t_{PLZ} ,	10	–	20	110	
		t_{PZH} ,	15	–	15	100	
		t_{PZL}					
Crosstalk, Control to Output ($V_{SS} = 0 \text{ Vdc}$) ($V_C = V_{DD}$, $R_{in} = 10 \text{ k}\Omega$, $R_{out} = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	9	–	5.0	–	30	–	mV
			10	–	50	–	
			15	–	100	–	
Crosstalk between any two switches ($V_{SS} = 0 \text{ Vdc}$) ($R_L = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ MHz}$, crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)	–	–	5.0	–	–80	–	dB
Noise Voltage ($V_{SS} = 0 \text{ Vdc}$) ($V_C = V_{DD}$, $f = 100 \text{ Hz}$) ($V_C = V_{DD}$, $f = 100 \text{ kHz}$)	10,11	–	5.0	–	24	–	nV/ $\sqrt{\text{Cycle}}$
			10	–	25	–	
			15	–	30	–	
			5.0	–	12	–	
			10	–	12	–	
			15	–	15	–	
Second Harmonic Distortion ($V_{SS} = -5.0 \text{ Vdc}$) ($V_{in} = 1.77 \text{ Vdc}$, RMS Centered @ 0.0 Vdc , $R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	–	–	5.0	–	0.16	–	%
Insertion Loss ($V_C = V_{DD}$, $V_{in} = 1.77 \text{ Vdc}$, $V_{SS} = -5.0 \text{ Vdc}$, RMS centered = 0.0 Vdc , $f = 1.0 \text{ MHz}$) $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	12	–	5.0				dB
				–	2.3	–	
				–	0.2	–	
				–	0.1	–	
				–	0.05	–	
Bandwidth (-3.0 dB) ($V_C = V_{DD}$, $V_{in} = 1.77 \text{ Vdc}$, $V_{SS} = -5.0 \text{ Vdc}$, RMS centered @ 0.0 Vdc) ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	12,13	BW	5.0				MHz
				–	54	–	
				–	40	–	
				–	38	–	
				–	37	–	
OFF Channel Feedthrough Attenuation ($V_{SS} = -5.0 \text{ Vdc}$) ($V_C = V_{SS}$, $20 \log_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB}$) ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	–	–	5.0				kHz
				–	1250	–	
				–	140	–	
				–	18	–	
				–	2.0	–	
				–			

4. The formulas given are for typical characteristics only at 25°C .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



V_{IL} : V_C is raised from V_{SS} until $V_C = V_{IL}$.
 at $V_C = V_{IL}$: $I_S = \pm 10 \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.
 V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

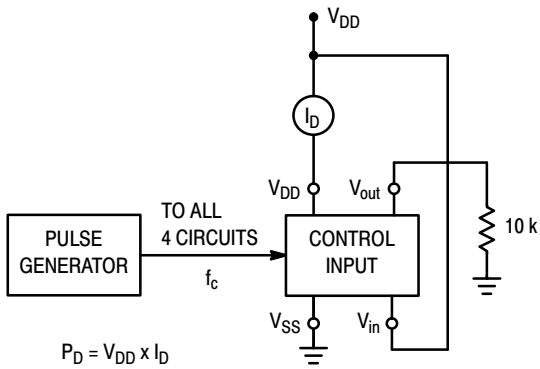


Figure 2. Quiescent Power Dissipation Test Circuit

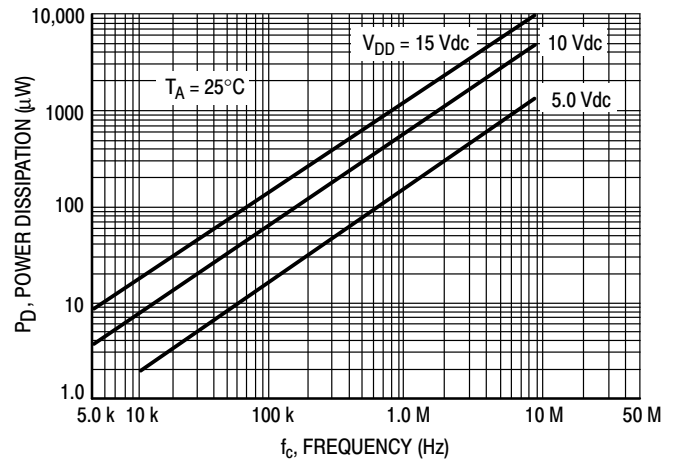


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

TYPICAL R_{ON} versus INPUT VOLTAGE

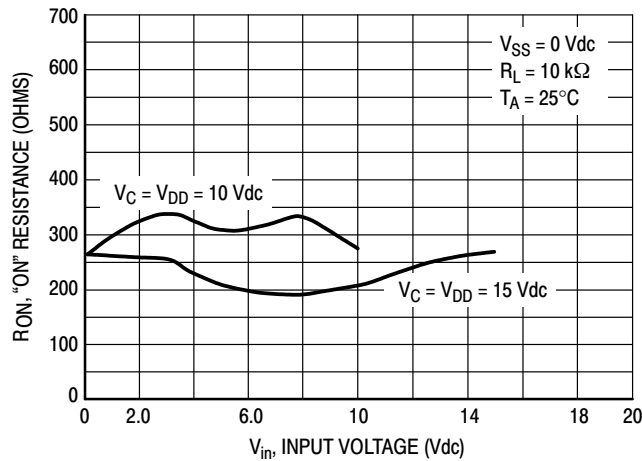


Figure 4. $V_{SS} = 0 V$

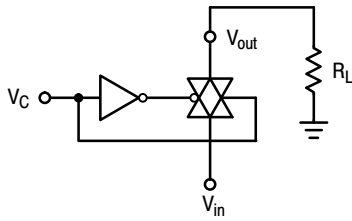


Figure 5. R_{ON} Characteristics Test Circuit

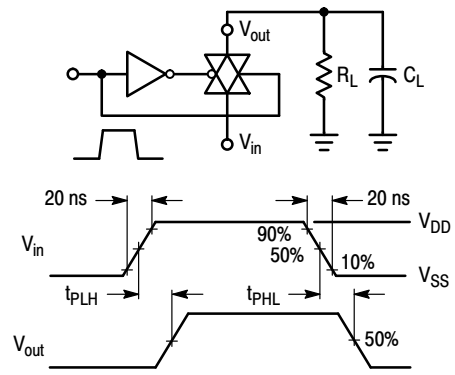


Figure 6. Propagation Delay Test Circuit and Waveforms

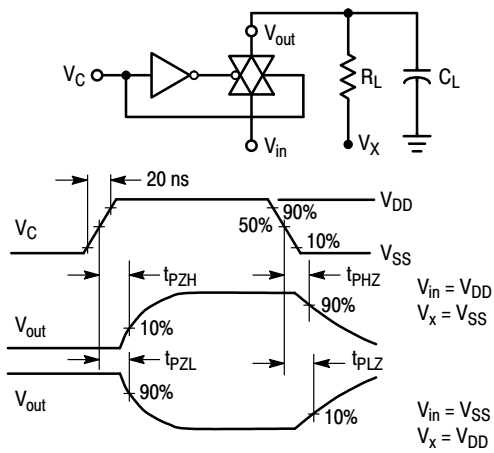


Figure 7. Turn-On Delay Time Test Circuit and Waveforms

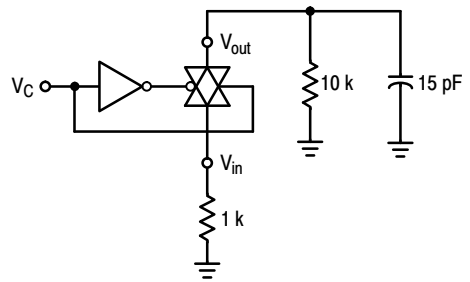


Figure 8. Crosstalk Test Circuit

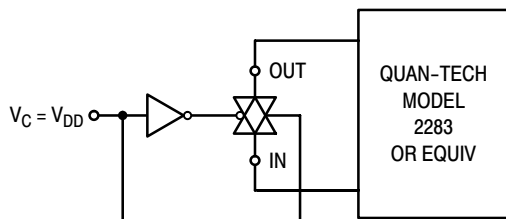


Figure 9. Noise Voltage Test Circuit

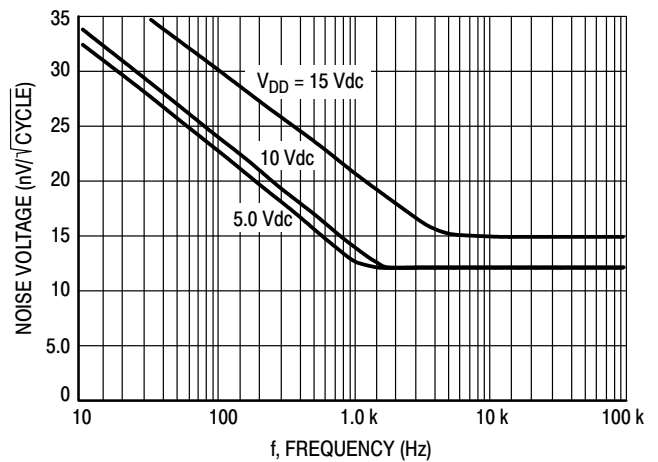


Figure 10. Typical Noise Characteristics

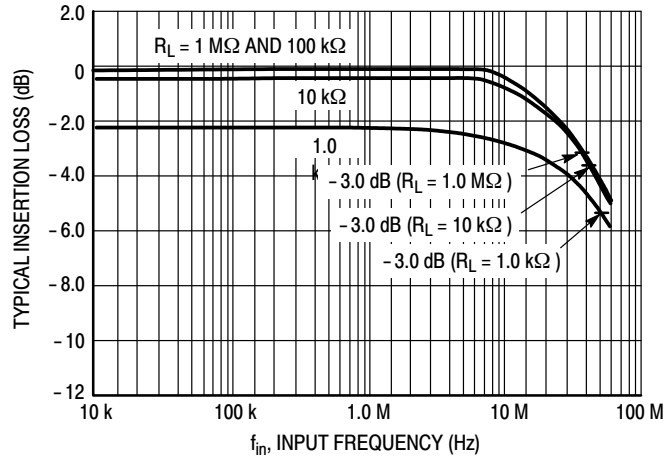


Figure 11. Typical Insertion Loss/Bandwidth Characteristics

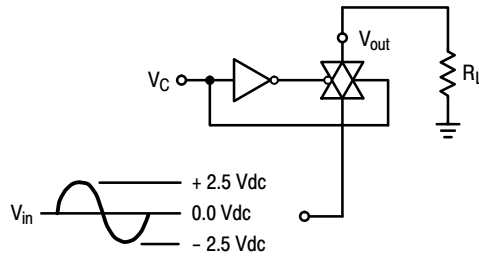


Figure 12. Frequency Response Test Circuit

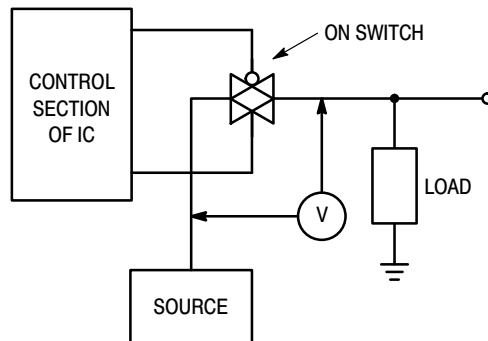


Figure 13. ΔV Across Switch

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V logic high at the control inputs; V_{SS} = GND = 0 V logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

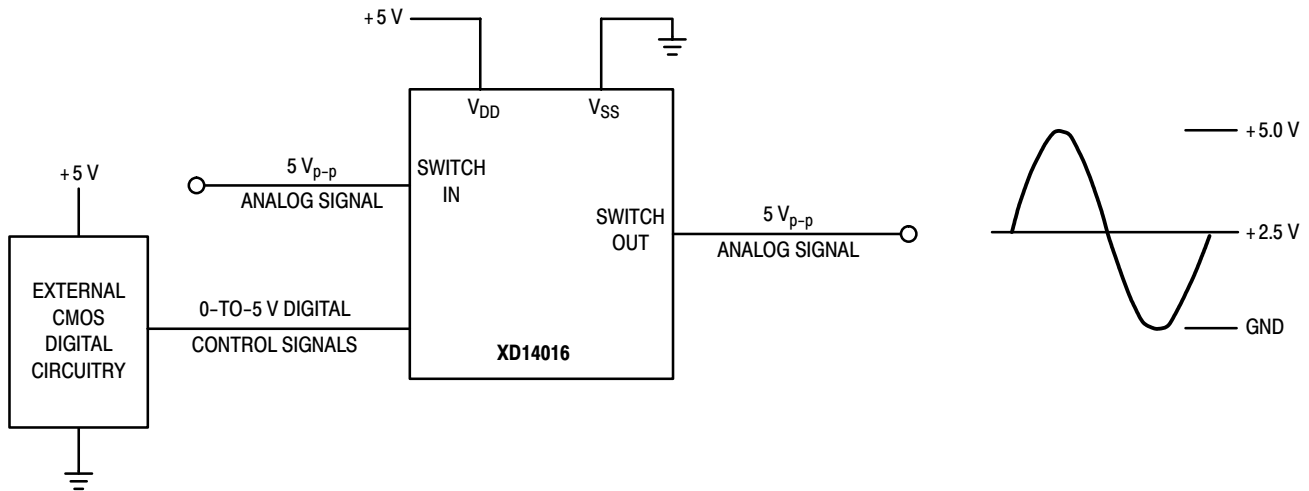
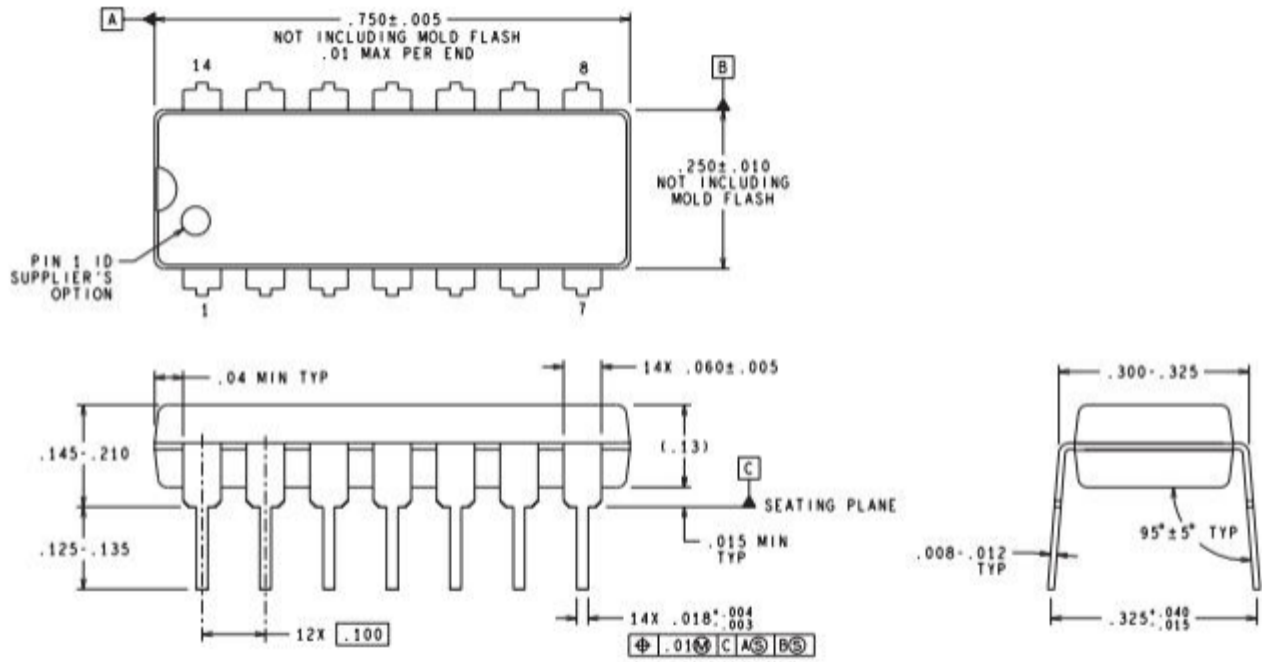


Figure A. Application Example



Figure B. External Germanium or Schottky Clipping Diodes

DIP14



DIMENSIONS ARE IN INCHES
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