

The XD14051, XD14052, and XD14053 analog multiplexers are digitally-controlled analog switches. The XD14051 effectively implements an SP8T solid state switch, the XD14052 a DP4T, and the XD14053 a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

#### Features

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ( $V_{DD} - V_{EE}$ ) = 3.0 to 18 V  
Note:  $V_{EE}$  must be  $\leq V_{SS}$

- Linearized Transfer Characteristics
- Low-noise –  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  Typical
- Pin-for-Pin Replacement for XD4051, XD4052, and XD4053
- For 4PDT Switch, See XD14551
- For Lower  $R_{ON}$ , Use the XD4051, XD4052, or XD4053 High-Speed CMOS Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

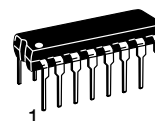
| Symbol                  | Parameter   | Value                  | Unit               |
|-------------------------|---|------------------------|--------------------|
| $V_{DD}$                | DC Supply Voltage Range (Referenced to $V_{EE}$ , $V_{SS} \geq V_{EE}$ )  | -0.5 to +18.0          | V                  |
| $V_{in}$ ,<br>$V_{out}$ | Input or Output Voltage Range (DC or Transient) (Referenced to $V_{SS}$ for Control Inputs and $V_{EE}$ for Switch I/O) | -0.5 to $V_{DD} + 0.5$ | V                  |
| $I_{in}$                | Input Current (DC or Transient) per Control Pin   | +10                    | mA                 |
| $I_{SW}$                | Switch Through Current  | $\pm 25$               | mA                 |
| $P_D$                   | Power Dissipation per Package (Note 1)  | 500                    | mW                 |
| $T_A$                   | Ambient Temperature Range   | -55 to +125            | $^{\circ}\text{C}$ |
| $T_{stg}$               | Storage Temperature Range   | -65 to +150            | $^{\circ}\text{C}$ |
| $T_L$                   | Lead Temperature (8-Second Soldering)   | 260                    | $^{\circ}\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

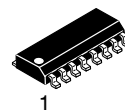
1. Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$ ,  $V_{EE}$  or  $V_{DD}$ ). Unused outputs must be left open.

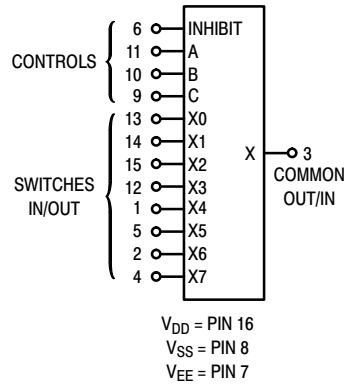


**PDIP-16**  
**P SUFFIX**  
**CASE 648**

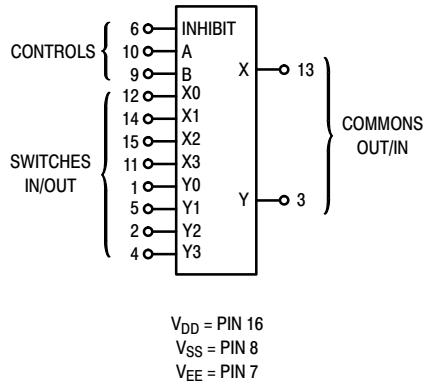


**SOIC-16**  
**D SUFFIX**  
**CASE 751B**

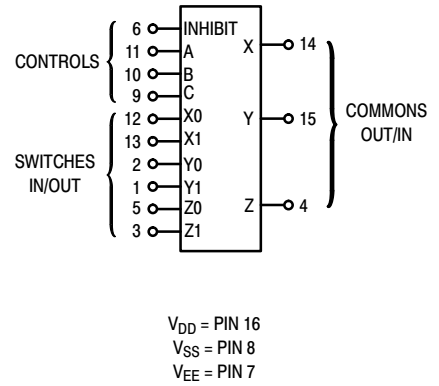
**XD14051**  
**8-Channel Analog**  
**Multiplexer/Demultiplexer**



**XD14052**  
**Dual 4-Channel Analog**  
**Multiplexer/Demultiplexer**

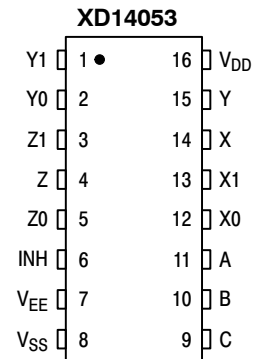
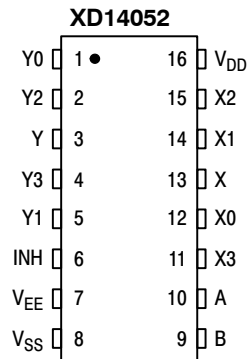
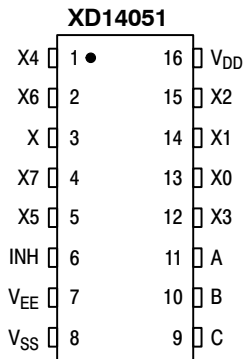


**XD14053**  
**Triple 2-Channel Analog**  
**Multiplexer/Demultiplexer**



Note: Control Inputs referenced to  $V_{SS}$ , Analog Inputs and Outputs reference to  $V_{EE}$ .  $V_{EE}$  must be  $\leq V_{SS}$ .

**PIN ASSIGNMENT**



**ELECTRICAL CHARACTERISTICS**

| Characteristic | Symbol | V <sub>DD</sub> | Test Conditions | - 55°C |     | 25°C |                 |     | 125°C |     | Unit |
|----------------|--------|-----------------|-----------------|--------|-----|------|-----------------|-----|-------|-----|------|
|                |        |                 |                 | Min    | Max | Min  | Typ<br>(Note 2) | Max | Min   | Max |      |

**SUPPLY REQUIREMENTS** (Voltages Referenced to V<sub>EE</sub>)

|  |                    |                 |  |         |     |     |       |     |   |     |    |
|--|--------------------|-----------------|--|---------|-----|-----|-------|-----|---|-----|----|
| Power Supply Voltage Range                                       | V <sub>DD</sub>    | -               | V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>  | 3.0     | 18  | 3.0 | -     | 18  | 3.0   | 18  | V  |
| Quiescent Current Per Package                                    | I <sub>DD</sub>    | 5.0             | Control Inputs:<br>V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> ,<br>Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤<br>V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤<br>500 mV (Note 3) | -       | 5.0 | -   | 0.005 | 5.0 | -   | 150 | μA |
|  |                    | 10              |  | -       | 10  | -   | 0.010 | 10  | -   | 300 |    |
|  |                    | 15              |  | -       | 20  | -   | 0.015 | 20  | -   | 600 |    |
| Total Supply Current<br>(Dynamic Plus<br>Quiescent, Per Package) | I <sub>D(AV)</sub> | 5.0<br>10<br>15 | T <sub>A</sub> = 25°C only (The<br>channel component,<br>(V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is<br>not included.)  | Typical |     |     |       |     | (0.07 μA/kHz) f + I <sub>DD</sub><br>(0.20 μA/kHz) f + I <sub>DD</sub><br>(0.36 μA/kHz) f + I <sub>DD</sub> |     | μA |

**CONTROL INPUTS — INHIBIT, A, B, C** (Voltages Referenced to V<sub>SS</sub>)

|                          |                 |     |  |     |       |     |           |       |     |     |    |
|--------------------------|-----------------|-----|--|-----|-------|-----|-----------|-------|-----|-----|----|
| Low-Level Input Voltage  | V <sub>IL</sub> | 5.0 | R <sub>on</sub> = per spec,<br>I <sub>off</sub> = per spec | -   | 1.5   | -   | 2.25      | 1.5   | -   | 1.5 | V  |
|                          |                 | 10  |  | -   | 3.0   | -   | 4.50      | 3.0   | -   | 3.0 |    |
|                          |                 | 15  |  | -   | 4.0   | -   | 6.75      | 4.0   | -   | 4.0 |    |
| High-Level Input Voltage | V <sub>IH</sub> | 5.0 | R <sub>on</sub> = per spec,<br>I <sub>off</sub> = per spec | 3.5 | -     | 3.5 | 2.75      | -     | 3.5 | -   | V  |
|                          |                 | 10  |  | 7.0 | -     | 7.0 | 5.50      | -     | 7.0 | -   |    |
|                          |                 | 15  |  | 11  | -     | 11  | 8.25      | -     | 11  | -   |    |
| Input Leakage Current    | I <sub>in</sub> | 15  | V <sub>in</sub> = 0 or V <sub>DD</sub>                     | -   | ± 0.1 | -   | ± 0.00001 | ± 0.1 | -   | 1.0 | μA |
| Input Capacitance        | C <sub>in</sub> | -   |  | -   | -     | -   | 5.0       | 7.5   | -   | -   | pF |

**SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z** (Voltages Referenced to V<sub>EE</sub>)

|   |                      |     |   |   |                 |      |        |                 |   |                 |                 |
|---|----------------------|-----|---|---|-----------------|------|--------|-----------------|---|-----------------|-----------------|
| Recommended Peak-to-Peak Voltage Into or Out of the Switch                  | V <sub>I/O</sub>     | -   | Channel On or Off   | 0 | V <sub>DD</sub> | 0    | -      | V <sub>DD</sub> | 0 | V <sub>DD</sub> | V <sub>PP</sub> |
| Recommended Static or Dynamic Voltage Across the Switch (Note 3) (Figure 5) | ΔV <sub>switch</sub> | -   | Channel On  | 0 | 600             | 0    | -      | 600             | 0 | 300             | mV              |
| Output Offset Voltage   | V <sub>OO</sub>      | -   | V <sub>in</sub> = 0 V, No Load  | - | -               | -    | 10     | -               | - | -               | μV              |
| ON Resistance   | R <sub>on</sub>      | 5.0 | ΔV <sub>switch</sub> ≤ 500 mV<br>(Note 3) V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>(Control), and V <sub>in</sub> =<br>0 to V <sub>DD</sub> (Switch) | - | 800             | -    | 250    | 1050            | - | 1200            | Ω               |
|   |                      | 10  |   | - | 400             | -    | 120    | 500             | - | 520             |                 |
|   |                      | 15  |   | - | 220             | -    | 80     | 280             | - | 300             |                 |
| ΔON Resistance Between Any Two Channels in the Same Package                 | ΔR <sub>on</sub>     | 5.0 |   | - | 70              | -    | 25     | 70              | - | 135             | Ω               |
|   |                      | 10  |   | - | 50              | -    | 10     | 50              | - | 95              |                 |
|   |                      | 15  |   | - | 45              | -    | 10     | 45              | - | 65              |                 |
| Off-Channel Leakage Current (Figure 10)                                     | I <sub>off</sub>     | 15  | V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>(Control) Channel to<br>Channel or Any One<br>Channel   | - | ± 100           | -    | ± 0.05 | ± 100           | - | ± 1000          | nA              |
| Capacitance, Switch I/O   | C <sub>I/O</sub>     | -   | Inhibit = V <sub>DD</sub>   | - | -               | -    | 10     | -               | - | -               | pF              |
| Capacitance, Common O/I   | C <sub>O/I</sub>     | -   | Inhibit = V <sub>DD</sub><br>(XD14051)<br>(XD14052)<br>(XD14053)  | - | -               | -    | 60     | -               | - | -               | pF              |
|   |                      | -   |   | - | -               | 32   | -      | -               | - |                 |                 |
|   |                      | -   |   | - | -               | 17   | -      | -               | - |                 |                 |
| Capacitance, Feedthrough (Channel Off)                                      | C <sub>I/O</sub>     | -   | Pins Not Adjacent<br>Pins Adjacent  | - | -               | -    | 0.15   | -               | - | -               | pF              |
|   |                      | -   |   | - | -               | 0.47 | -      | -               | - |                 |                 |

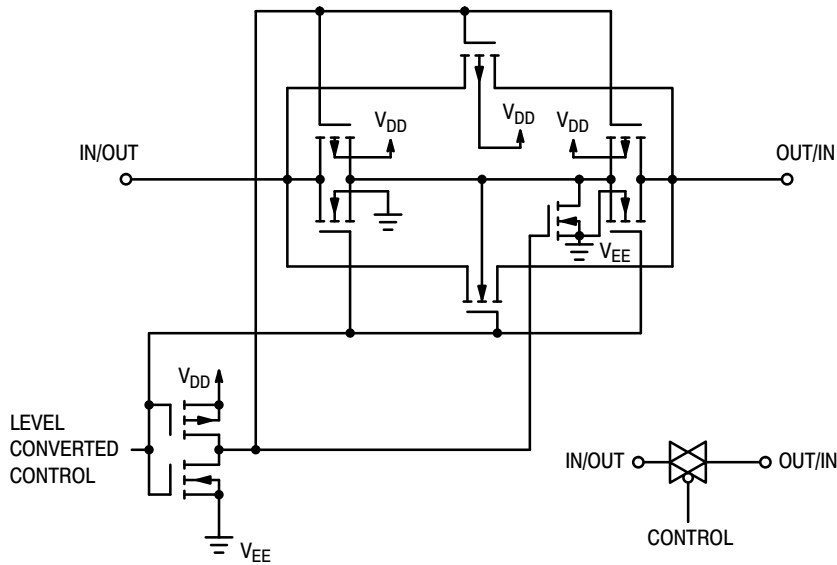
2. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
3. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn, i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

**ELECTRICAL CHARACTERISTICS** (Note 4) ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ) ( $V_{EE} \leq V_{SS}$  unless otherwise indicated)

| Characteristic   | Symbol                                    | $V_{DD} - V_{EE}$<br>Vdc | Typ (Note 5)<br>All Types | Max | Unit |
|--|---|--------------------------|---------------------------|-----|------|
| Propagation Delay Times (Figure 6)<br>Switch Input to Switch Output ( $R_L = 1 \text{ k}\Omega$ )<br>XD14051<br>$t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$<br>XD14052<br>$t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 21.5 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 8.0 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 7.0 \text{ ns}$<br>XD14053<br>$t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 16.5 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 4.0 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 3.0 \text{ ns}$ | $t_{PLH}, t_{PHL}$                        | 5.0                      | 35                        | 90  | ns   |
|  |   | 10                       | 15                        | 40  |      |
|  |   | 15                       | 12                        | 30  |      |
|  |   | 5.0                      | 30                        | 75  | ns   |
|  |   | 10                       | 12                        | 30  |      |
|  |   | 15                       | 10                        | 25  |      |
|  |   | 5.0                      | 25                        | 65  | ns   |
|  |   | 10                       | 8.0                       | 20  |      |
|  |   | 15                       | 6.0                       | 15  |      |
| Inhibit to Output ( $R_L = 10 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ )<br>Output "1" or "0" to High Impedance, or<br>High Impedance to "1" or "0" Level<br>XD14051<br><br>XD14052<br><br>XD14053   | $t_{PHZ}, t_{PLZ},$<br>$t_{PZH}, t_{PZL}$ | 5.0                      | 350                       | 700 | ns   |
|  |   | 10                       | 170                       | 340 |      |
|  |   | 15                       | 140                       | 280 |      |
|  |   | 5.0                      | 300                       | 600 | ns   |
|  |   | 10                       | 155                       | 310 |      |
|  |   | 15                       | 125                       | 250 |      |
|  |   | 5.0                      | 275                       | 550 | ns   |
|  |   | 10                       | 140                       | 280 |      |
|  |   | 15                       | 110                       | 220 |      |
| Control Input to Output ( $R_L = 1 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ )<br>XD14051<br><br>XD14052<br><br>XD14053   | $t_{PLH}, t_{PHL}$                        | 5.0                      | 360                       | 720 | ns   |
|  |   | 10                       | 160                       | 320 |      |
|  |   | 15                       | 120                       | 240 |      |
|  |   | 5.0                      | 325                       | 650 | ns   |
|  |   | 10                       | 130                       | 260 |      |
|  |   | 15                       | 90                        | 180 |      |
|  |   | 5.0                      | 300                       | 600 | ns   |
|  |   | 10                       | 120                       | 240 |      |
|  |   | 15                       | 80                        | 160 |      |
| Second Harmonic Distortion<br>( $R_L = 10\text{K}\Omega$ , $f = 1 \text{ kHz}$ ) $V_{in} = 5 V_{PP}$   | -   | 10                       | 0.07                      | -   | %    |
| Bandwidth (Figure 7)<br>( $R_L = 50 \Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $C_L = 50\text{pF}$<br>$20 \text{ Log } (V_{out}/V_{in}) = -3 \text{ dB}$ )  | BW  | 10                       | 17                        | -   | MHz  |
| Off Channel Feedthrough Attenuation (Figure 7)<br>$R_L = 1\text{K}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p<br>$f_{in} = 4.5 \text{ MHz}$ — XD14051<br>$f_{in} = 30 \text{ MHz}$ — XD14052<br>$f_{in} = 55 \text{ MHz}$ — XD14053   | -   | 10                       | -50                       | -   | dB   |
| Channel Separation (Figure 8)<br>( $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p,<br>$f_{in} = 3.0 \text{ MHz}$ )   | -   | 10                       | -50                       | -   | dB   |
| Crosstalk, Control Input to Common O/I (Figure 9)<br>( $R_1 = 1 \text{ k}\Omega$ , $R_L = 10 \text{ k}\Omega$<br>Control $t_{TLH} = t_{THL} = 20 \text{ ns}$ , Inhibit = $V_{SS}$ )  | -   | 10                       | 75                        | -   | mV   |

4. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

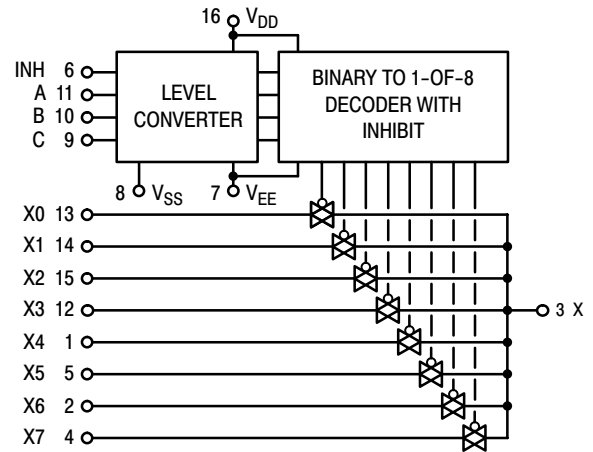


**Figure 1. Switch Circuit Schematic**

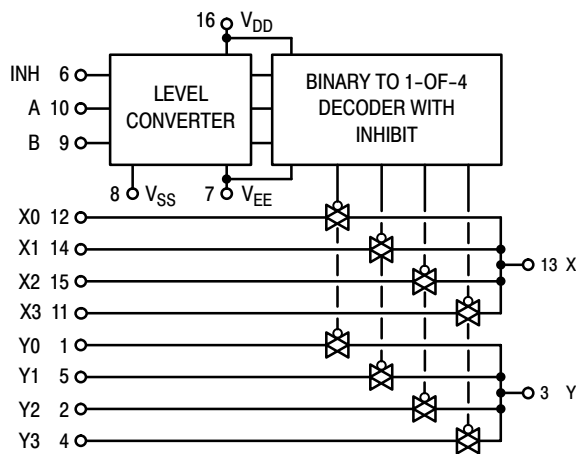
**TRUTH TABLE**

| Control Inputs |        |      | ON Switches |          |         |
|----------------|--------|------|-------------|----------|---------|
| Inhibit        | Select |      | XD14051     | XD14052  | XD14053 |
|                | C*     | B A  |             |          |         |
| 0              | 0 0 0  | X0   | Y0 X0       | Z0 Y0 X0 |         |
| 0              | 0 0 1  | X1   | Y1 X1       | Z0 Y0 X1 |         |
| 0              | 0 1 0  | X2   | Y2 X2       | Z0 Y1 X0 |         |
| 0              | 0 1 1  | X3   | Y3 X3       | Z0 Y1 X1 |         |
| 0              | 1 0 0  | X4   |             | Z1 Y0 X0 |         |
| 0              | 1 0 1  | X5   |             | Z1 Y0 X1 |         |
| 0              | 1 1 0  | X6   |             | Z1 Y1 X0 |         |
| 0              | 1 1 1  | X7   |             | Z1 Y1 X1 |         |
| 1              | x x x  | None | None        | None     |         |

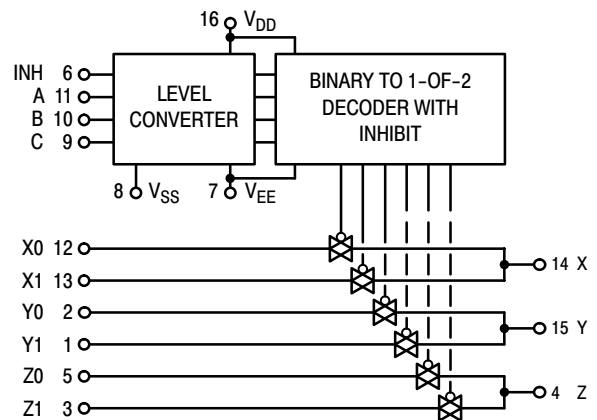
\*Not applicable for XD14052  
 x = Don't Care



**Figure 2. XD14051 Functional Diagram**

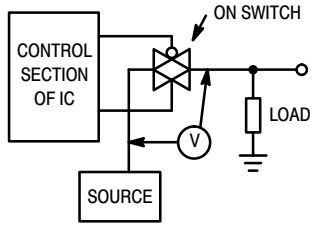


**Figure 3. XD14052 Functional Diagram**

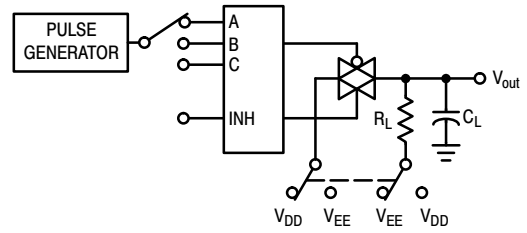


**Figure 4. XD14053 Functional Diagram**

**TEST CIRCUITS**

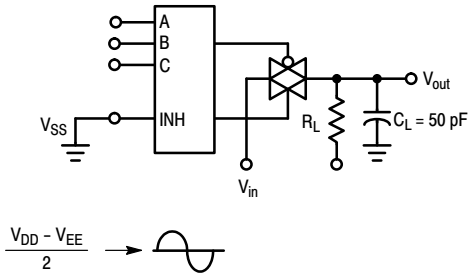


**Figure 5.  $\Delta V$  Across Switch**

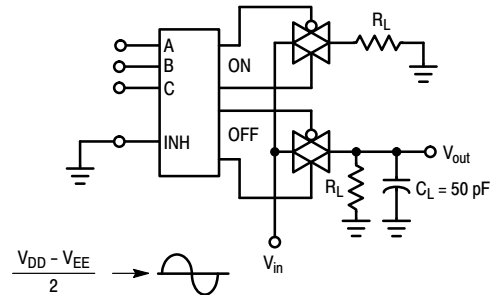


**Figure 6. Propagation Delay Times, Control and Inhibit to Output**

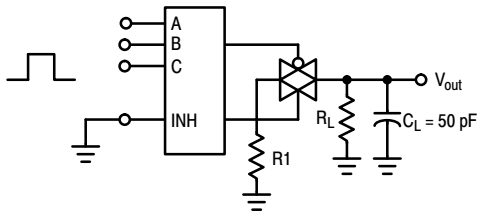
A, B, and C inputs used to turn ON or OFF the switch under test.



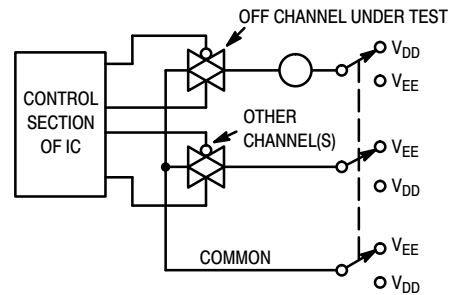
**Figure 7. Bandwidth and Off-Channel Feedthrough Attenuation**



**Figure 8. Channel Separation (Adjacent Channels Used For Setup)**

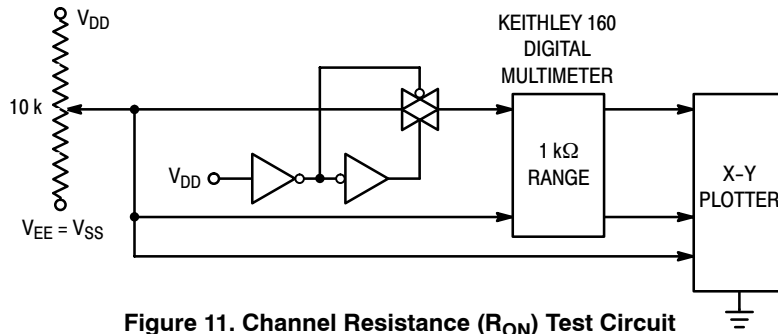


**Figure 9. Crosstalk, Control Input to Common O/I**

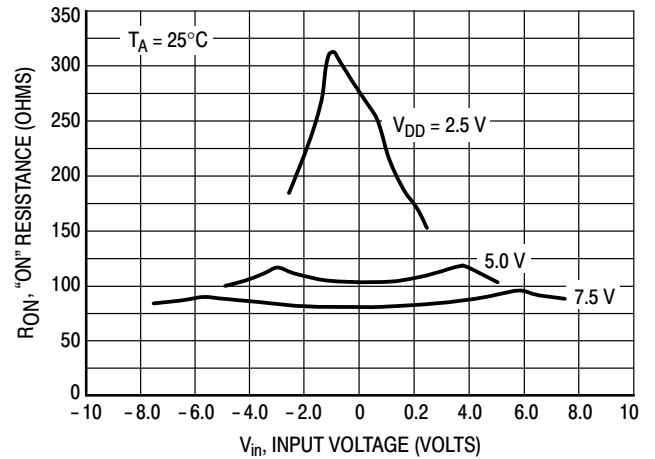
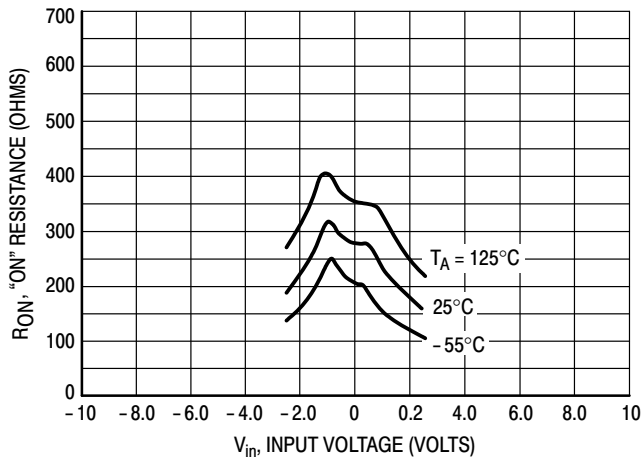
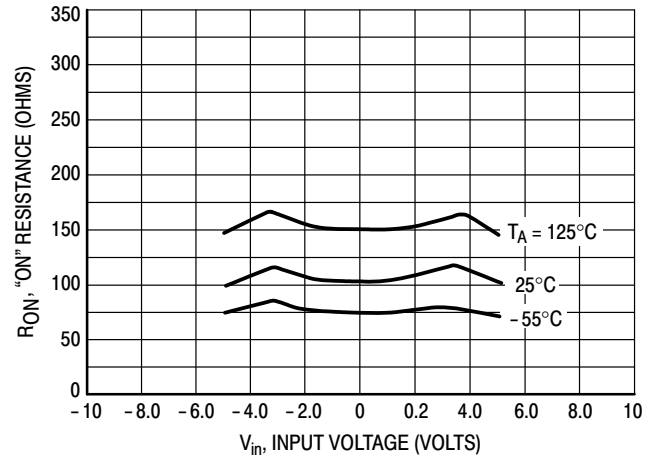
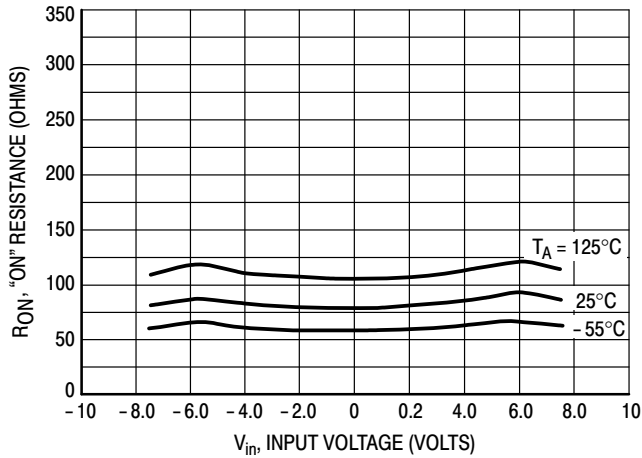


**Figure 10. Off Channel Leakage**

NOTE: See also Figures 7 and 8 in the XD14016 data sheet.



**TYPICAL RESISTANCE CHARACTERISTICS**



### APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V<sub>p-p</sub> analog signal.

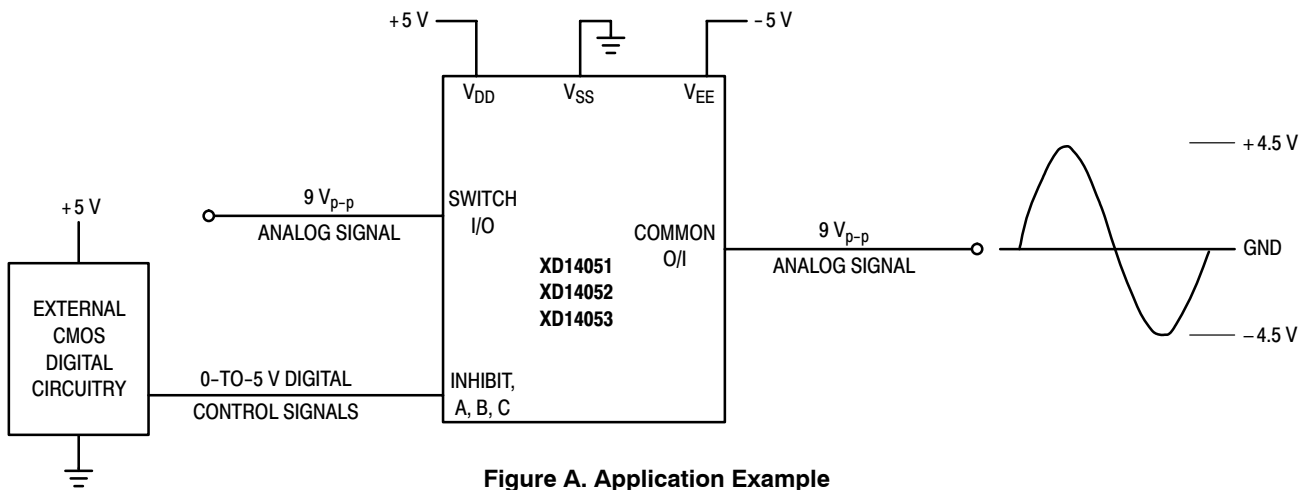
The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>EE</sub>. The V<sub>DD</sub> voltage determines the maximum recommended peak above V<sub>SS</sub>. The V<sub>EE</sub> voltage determines the maximum swing below V<sub>SS</sub>. For the example, V<sub>DD</sub> - V<sub>SS</sub> = 5 V maximum swing above V<sub>SS</sub>; V<sub>SS</sub> - V<sub>EE</sub> = 5 V maximum swing below V<sub>SS</sub>. The example shows a ±4.5 V signal which allows a 1/2 volt margin at each

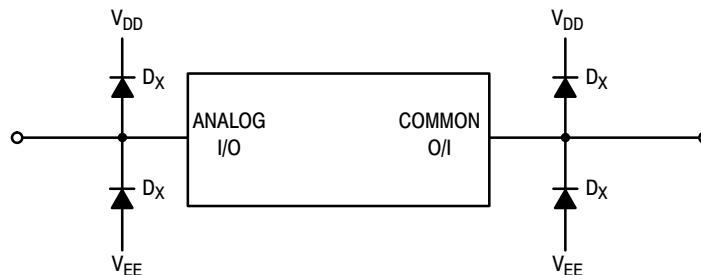
peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V<sub>DD</sub> and V<sub>EE</sub> is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V<sub>DD</sub> and V<sub>EE</sub>.

Balanced supplies are not required. However, V<sub>SS</sub> must be greater than or equal to V<sub>EE</sub>. For example, V<sub>DD</sub> = +10 V, V<sub>SS</sub> = +5 V, and V<sub>EE</sub> = -3 V is acceptable. See the Table below.



**Figure A. Application Example**



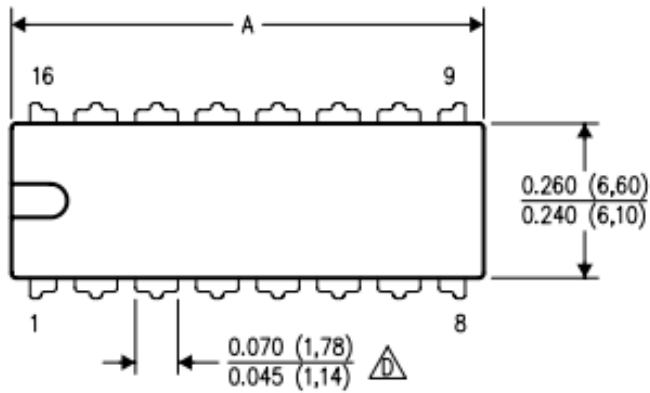
**Figure B. External Germanium or Schottky Clipping Diodes**

#### POSSIBLE SUPPLY CONNECTIONS

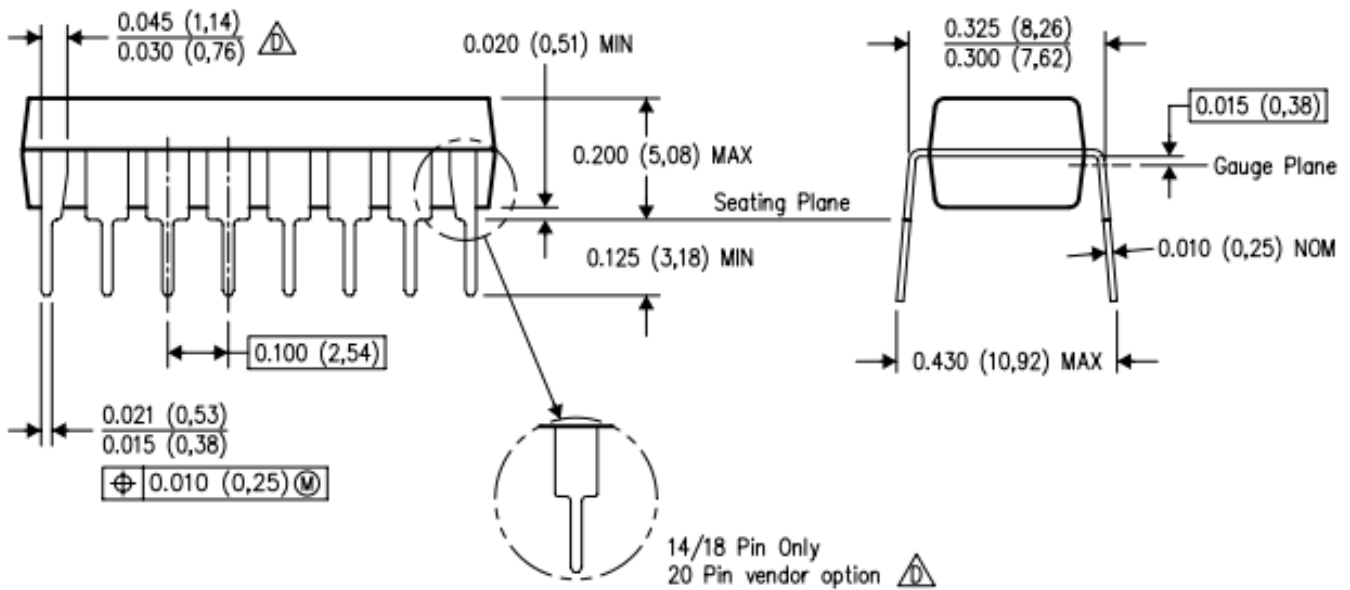
| V <sub>DD</sub><br>In Volts | V <sub>SS</sub><br>In Volts | V <sub>EE</sub><br>In Volts | Control Inputs<br>Logic High/Logic Low<br>In Volts | Maximum Analog Signal Range<br>In Volts |
|-----------------------------|-----------------------------|-----------------------------|--|---|
| + 8                         | 0                           | - 8                         | + 8/0  | + 8 to - 8 = 16 V <sub>p-p</sub>        |
| + 5                         | 0                           | - 12                        | + 5/0  | + 5 to - 12 = 17 V <sub>p-p</sub>       |
| + 5                         | 0                           | 0                           | + 5/0  | + 5 to 0 = 5 V <sub>p-p</sub>           |
| + 5                         | 0                           | - 5                         | + 5/0  | + 5 to - 5 = 10 V <sub>p-p</sub>        |
| + 10                        | + 5                         | - 5                         | + 10/+ 5   | + 10 to - 5 = 15 V <sub>p-p</sub>       |



XD14051 XD14052 XD14053  
 XL14051 XL14052 XL14053



| DIM \ PINS **    | 14               | 16               | 18               | 20               |
|------------------|------------------|------------------|------------------|------------------|
| A MAX            | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN            | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001 VARIATION | AA               | BB               | AC               | AD               |



以上信息仅供参考. 如需帮助联系客服人员. 谢谢 XINLU DA

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