1 Features

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

2 Applications

- Relay Drivers
- Stepper and DC Brushed Motor Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

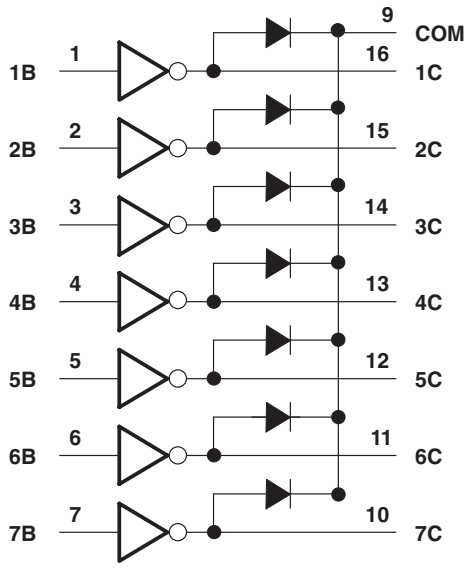
The XD/L200X devices are high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads.

The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the 2003 devices, see the SLRS023 data sheet for the SN75468 and SN75469 devices.

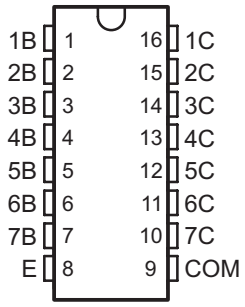
The XD/L200X device is designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode and resistor in series to control the input current to a safe limit. The 2003 devices have a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

The 2004 devices have a 10.5-kΩ series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the 2004 device is below that of the 2003 devices, and the required voltage is less than that required by the XD/L200X device.

4 Simplified Block Diagram



5 Pin Configuration and Functions



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 7 Darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
1C	16	O	Channel 1 through 7 Darlington collector output
2C	15		
3C	14		
4C	13		
5C	12		
6C	11		
7C	10		
COM	9	—	Common cathode node for flyback diodes (required for inductive loads)
E	8	—	Common emitter shared by all channels (typically tied to ground)

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Collector-emitter voltage			50	V
	Clamp diode reverse voltage(2)			50	V
V_I	Input voltage(2)			30	V
	Peak collector current, See Figure 4 and Figure 5			500	mA
I_{OK}	Output clamp current			500	mA
	Total emitter-terminal current			–2.5	A
T_A	Operating free-air temperature range	XD/L200X	–20	70	°C
			–40	105	
			–40	85	
			–40	105	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature for 1.6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Collector-emitter voltage (non-V devices)	0	50	V
T_J	Junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		XD/L200X				UNIT
		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	67	64	108	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	54	n/a	33.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	n/a	n/a	n/a	51.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	n/a	n/a	n/a	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	n/a	n/a	n/a	51.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: XD/L2002

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		XD/L2002			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 14	V_{CE} = 2 V,	I_C = 300 mA			13	V
V_{OH}	High-level output voltage after switching	Figure 18	V_S = 50 V, I_O = 300 mA		V_S – 20			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 12	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
V_F	Clamp forward voltage	Figure 15	I_F = 350 mA			1.7	2	V
I_{CEX}	Collector cutoff current	Figure 9	V_{CE} = 50 V,	I_I = 0			50	µA
		Figure 10	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100	
				V_I = 6 V			500	
$I_{I(off)}$	OFF-state input current	Figure 10	V_{CE} = 50 V,	I_C = 500 µA	50	65		µA
I_I	Input current	Figure 11	V_I = 17 V			0.82	1.25	mA
I_R	Clamp reverse current	Figure 14	V_R = 50 V	T_A = 70°C			100	µA
			V_R = 50 V				50	
C_i	Input capacitance		V_I = 0,	f = 1 MHz			25	pF

6.6 Electrical Characteristics: 2003 and 2004

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		2003			2004			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 14	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
V_{OH}	High-level output voltage after switching	Figure 18	V_S = 50 V, I_O = 300 mA		V_S – 20			V_S – 20			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 13	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 9	V_{CE} = 50 V,	I_I = 0			50			50	µA
		Figure 10	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 6 V						500	
V_F	Clamp forward voltage	Figure 16	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 11	V_{CE} = 50 V, T_A = 70°C,	I_C = 500 µA	50	65		50	65		µA
I_I	Input current	Figure 12	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	Figure 15	V_R = 50 V				50			50	µA
			V_R = 50 V	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

6.7 Electrical Characteristics: 2003

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		2003			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 14	V_{CE} = 2 V	I_C = 200 mA			2.4	V
				I_C = 250 mA			2.7	
				I_C = 300 mA			3	
V_{OH}	High-level output voltage after switching	Figure 18	V_S = 50 V, I_O = 300 mA		V_S – 50			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 13	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 9	V_{CE} = 50 V,	I_I = 0			50	µA
V_F	Clamp forward voltage	Figure 16	I_F = 350 mA			1.7	2	V
$I_{I(off)}$	OFF-state input current	Figure 11	V_{CE} = 50 V,	I_C = 500 µA	50	65		µA
I_I	Input current	Figure 12	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	Figure 15	V_R = 50 V				50	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

6.8 Electrical Characteristics: 2003

T_A = –40°C to 105°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		2003			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 14	V_{CE} = 2 V	I_C = 200 mA			2.7	V
				I_C = 250 mA			2.9	
				I_C = 300 mA			3	
V_{OH}	High-level output voltage after switching	Figure 18	V_S = 50 V, I_O = 300 mA		V_S – 50			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 13	I_I = 250 µA,	I_C = 100 mA		0.9	1.2	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7	
I_{CEX}	Collector cutoff current	Figure 9	V_{CE} = 50 V,	I_I = 0			100	µA
V_F	Clamp forward voltage	Figure 16	I_F = 350 mA			1.7	2.2	V
$I_{I(off)}$	OFF-state input current	Figure 11	V_{CE} = 50 V,	I_C = 500 µA	30	65		µA
I_I	Input current	Figure 12	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	Figure 15	V_R = 50 V				100	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

6.9 Electrical Characteristics: 2003 and 2004

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		2003			2004			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 14	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.7			6	
				I_C = 250 mA			2.9				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
V_{OH}	High-level output voltage after switching	Figure 18	V_S = 50 V, I_O = 300 mA		V_S – 50			V_S – 50			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 13	I_I = 250 µA,	I_C = 100 mA		0.9	1.2		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 9	V_{CE} = 50 V,	I_I = 0			100			50	µA
		Figure 10	V_{CE} = 50 V, T_A = 70°C	I_I = 0						100	
				V_I = 6 V						500	
V_F	Clamp forward voltage	Figure 16	I_F = 350 mA			1.7	2.3		1.7	2	V
$I_{I(off)}$	OFF-state input current	Figure 11	V_{CE} = 50 V, T_A = 70°C,	I_C = 500 µA		65		50	65		µA
I_I	Input current	Figure 12	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	Figure 15	V_R = 50 V	T_A = 25°C			100			50	µA
			V_R = 50 V				100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

6.10 Switching Characteristics: XD/L2002, 2003, 2004

T_A = 25°C

PARAMETER		TEST CONDITIONS	XD/L2002, 2003, 2004			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 17		0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 17		0.25	1	µs

6.11 Switching Characteristics: 2003

T_A = 25°C

PARAMETER		TEST CONDITIONS	2003			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 17		0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 17		0.25	1	µs

6.12 Switching Characteristics: 2003

T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	2003			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 17		1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 17		1	10	µs

6.13 Switching Characteristics: 2003, 2004

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	2003, 2004			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 17		1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 17		1	10	µs

6.14 Typical Characteristics

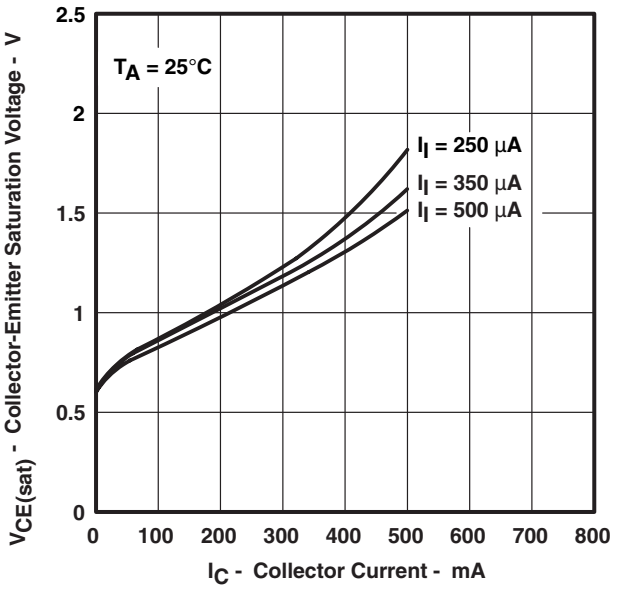


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

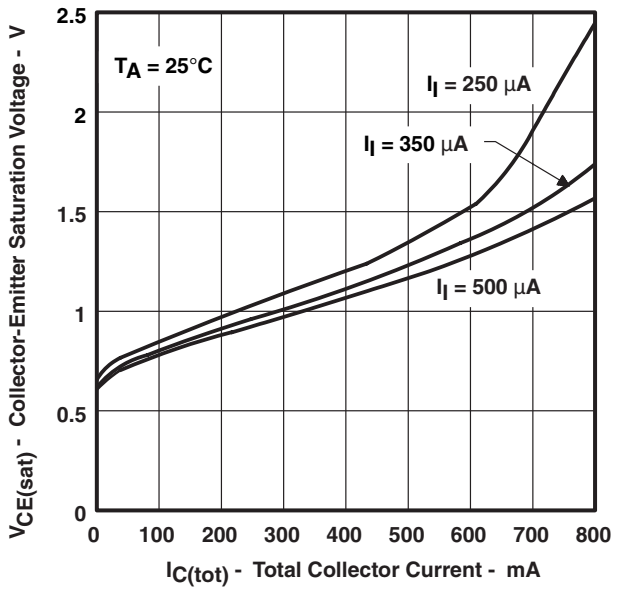


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

Typical Characteristics (continued)

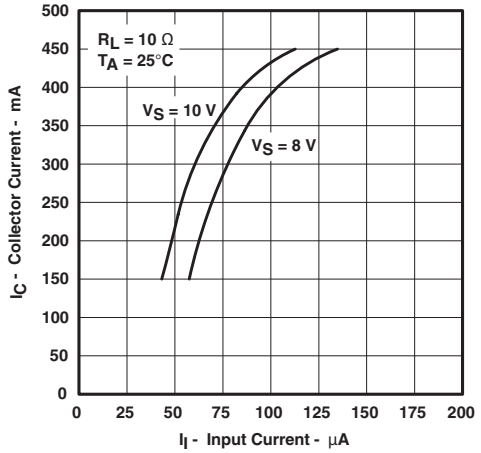


Figure 3. Collector Current vs Input Current

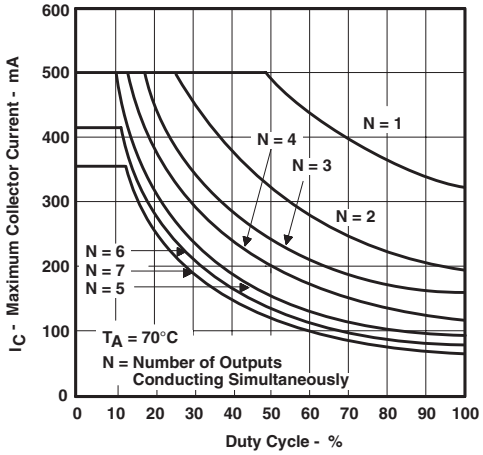


Figure 4. D Package Maximum Collector Current vs Duty Cycle

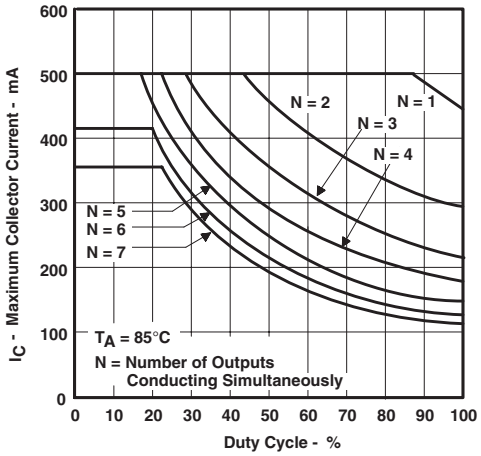


Figure 5. N Package Maximum Collector Current vs Duty Cycle

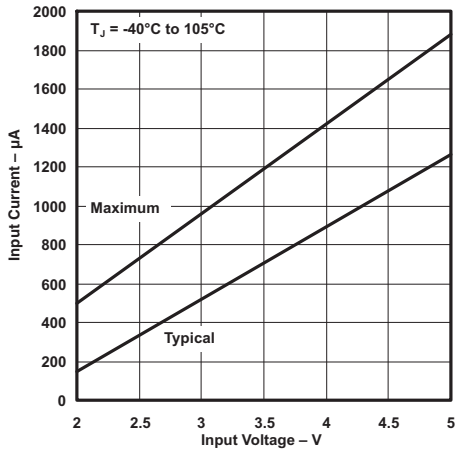


Figure 6. Maximum and Typical Input Current vs Input Voltage

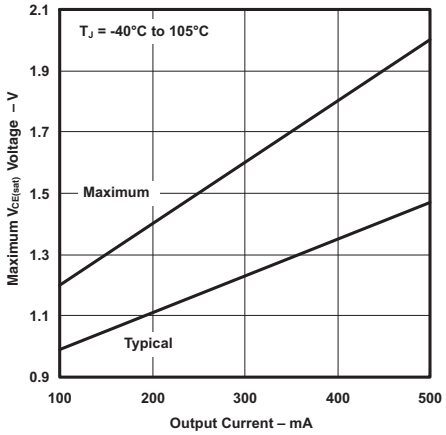


Figure 7. Maximum and Typical Saturated V_{CE} vs Output Current

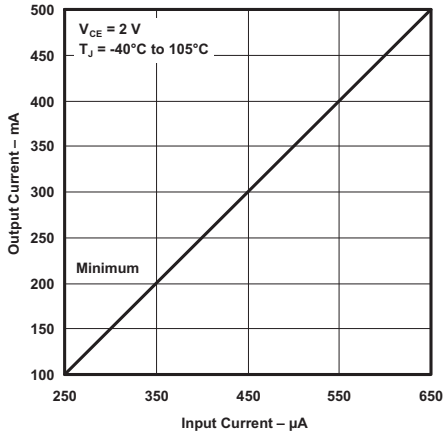


Figure 8. Minimum Output Current vs Input Current

7 Parameter Measurement Information

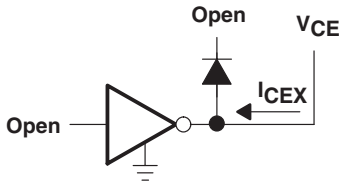


Figure 9. I_{CEX} Test Circuit

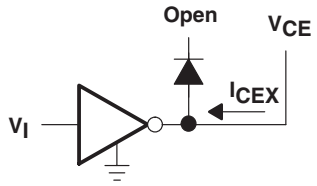


Figure 10. I_{CEX} Test Circuit

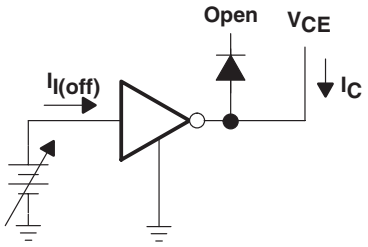


Figure 11. $I_{I(off)}$ Test Circuit

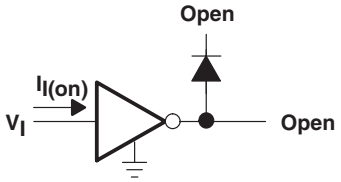


Figure 12. I_I Test Circuit

I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

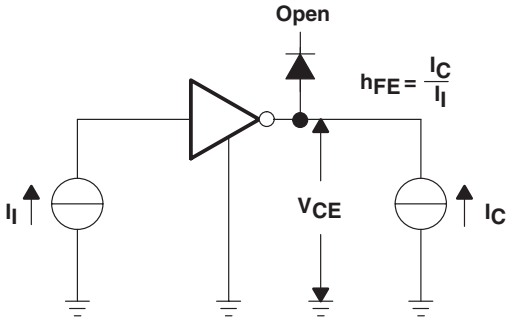


Figure 13. h_{FE}, $V_{CE(sat)}$ Test Circuit

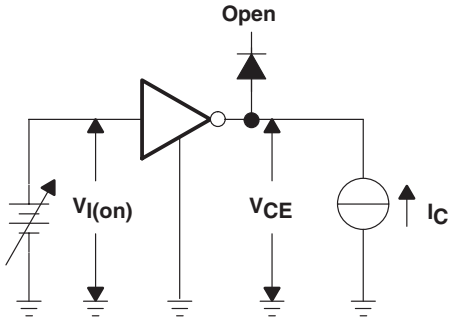


Figure 14. $V_{I(on)}$ Test Circuit

Parameter Measurement Information (continued)

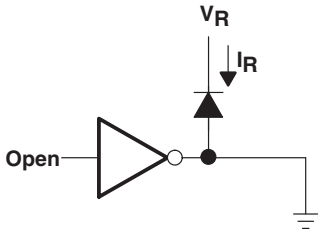


Figure 15. I_R Test Circuit

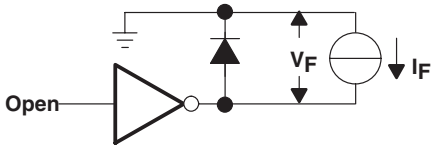


Figure 16. V_F Test Circuit

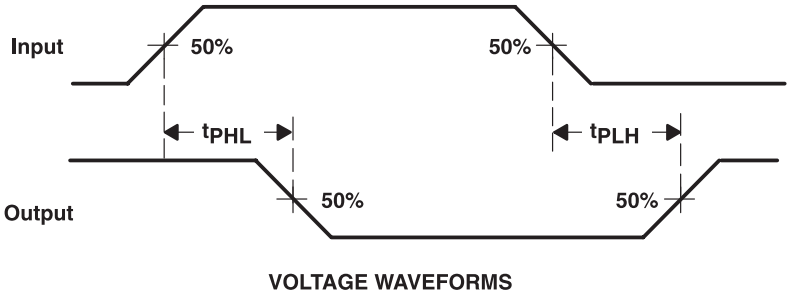
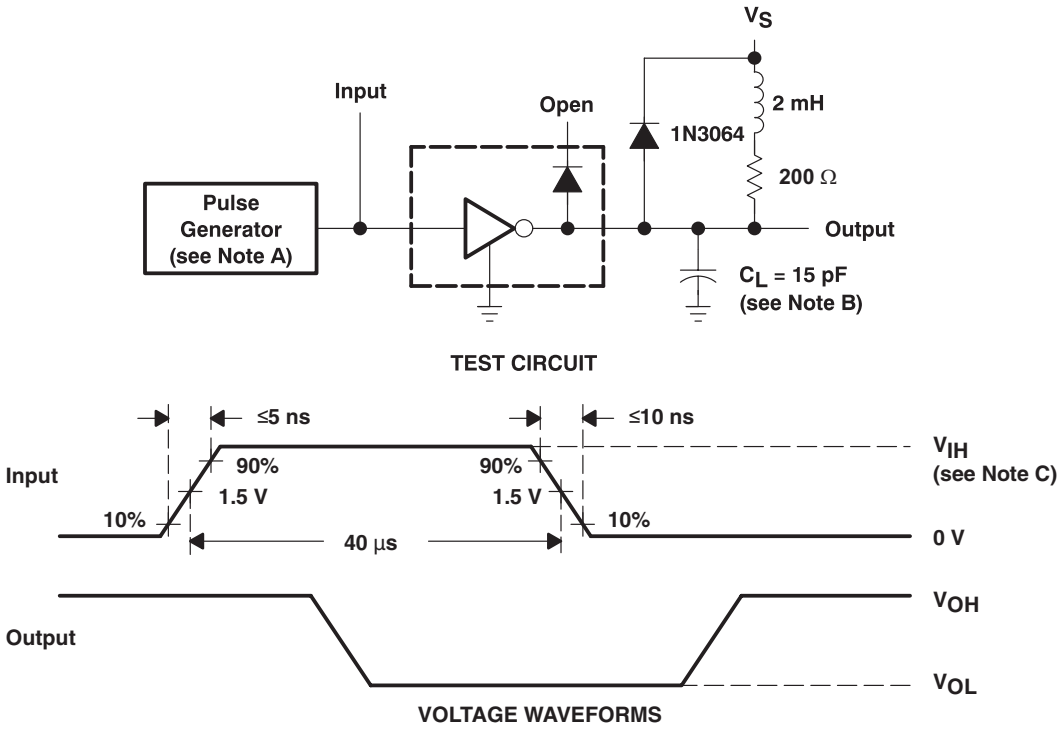


Figure 17. Propagation Delay-Time Waveforms



The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

C_L includes probe and jig capacitance.

For testing the 2003 device, 2003 device, and 2003 devices, V_{IH} = 3 V; for the XD/L2002 device, V_{IH} = 13 V; for the 2004 and the 2004 devices, V_{IH} = 8 V.

Figure 18. Latch-Up Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to integration of 7 Darlington transistors of the device that are capable of sinking up to 500 mA and wide GPIO range capability.

The 2003 device comprises seven high-voltage, high-current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The 2003 device has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The 2003 device offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

8.2 Functional Block Diagrams

All resistor values shown are nominal. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collectors go below GND, an external Schottky diode should be added to clamp negative undershoots.

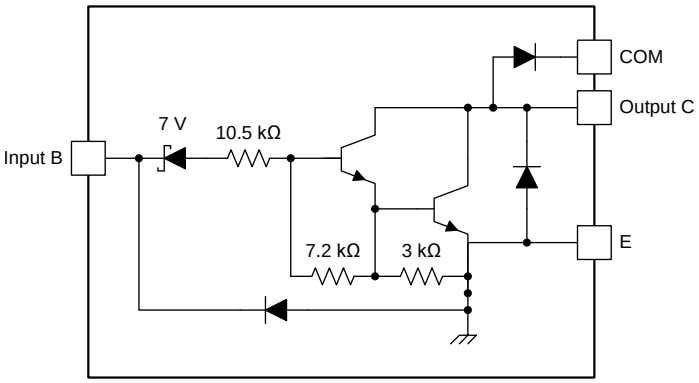


Figure 19. XD/L2002 Block Diagram

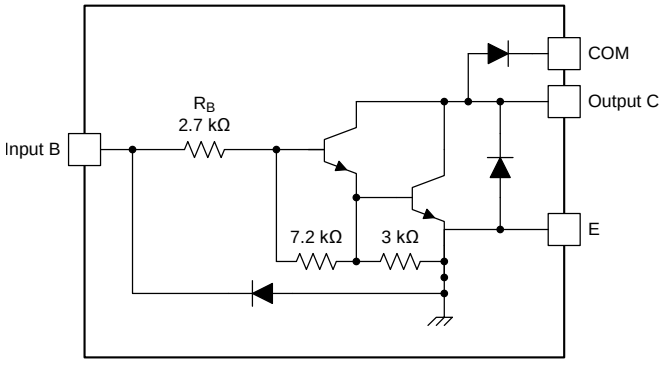


Figure 20.2003 Block Diagram

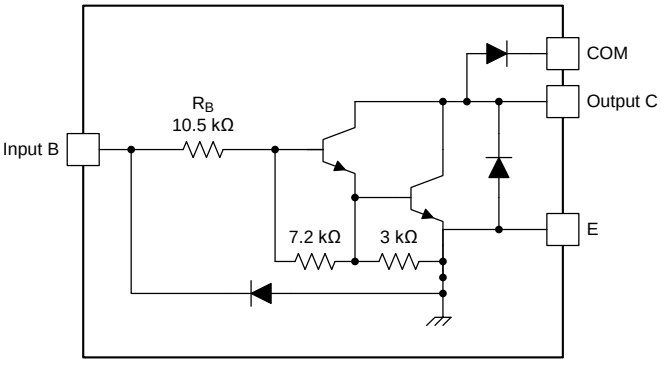


Figure 21. 2004 Block Diagram

8.3 Feature Description

Each channel of the 2003 device consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high-current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high-output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN. The 7.2-kΩ and 3-kΩ resistors connected between the base and emitter of each respective NPN act as pulldowns and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diodes are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, 2003 device is able to drive inductive loads and suppress the kick-back voltage through the internal free-wheeling diodes.

8.4.2 Resistive Load Drive

When driving a resistive load, a pullup resistor is needed in order for 2003 device to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

9 Application and Implementation

9.1 Application Information

Typically, the 2003 device drives a high-voltage or high-current (or both) peripheral from an MCU or logic device that cannot tolerate these conditions. This design is a common application of 2003 device, driving inductive loads. This includes motors, solenoids and relays. Figure 22 shows a model for each load type.

9.2 Typical Application

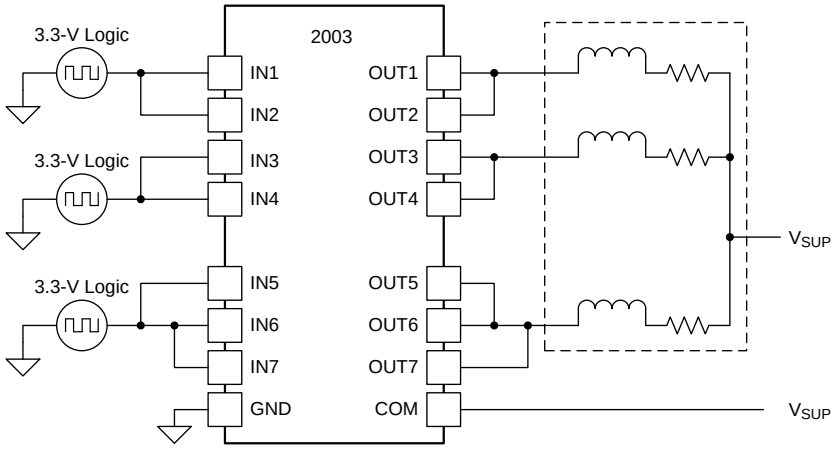


Figure 22. 2003 Device as Inductive Load Driver

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 V or 5 V
Coil supply voltage	12 V to 48 V
Number of channels	7
Output current (R_{COIL})	20 mA to 300 mA per channel
Duty cycle	100%

9.2.2 Detailed Design Procedure

When using 2003 device in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

9.2.2.1 Drive Current

The coil voltage (V_{SUP}), coil resistance (R_{COIL}), and low-level output voltage ($V_{CE(SAT)}$ or V_{OL}) determine the coil current.

$$I_{COIL} = (V_{SUP} – V_{CE(SAT)}) / R_{COIL} \quad (1)$$

9.2.2.2 Low-Level Output Voltage

The low-level output voltage (V_{OL}) is the same as $V_{CE(SAT)}$ and can be determined by, Figure 1, Figure 2, or Figure 7.

9.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by Figure 4 or Figure 5.

For a more accurate determination of number of coils possible, use the below equation to calculate 2003 device on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (2)

To ensure reliability of 2003 device and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by below equation Equation 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA}$$

where

- $T_{J(max)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- $R_{\theta JA}$ is the package junction to ambient thermal resistance (3)

Limit the die junction temperature of the 2003 device to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

9.2.3 Application Curves

The characterization data shown in Figure 23 and Figure 24 were generated using the 2003 device drivingan OMRON G5NB relay and under the following conditions: V_{IN} = 5 V, V_{SUP}= 12 V, and R_{COIL}= 2.8 kΩ.

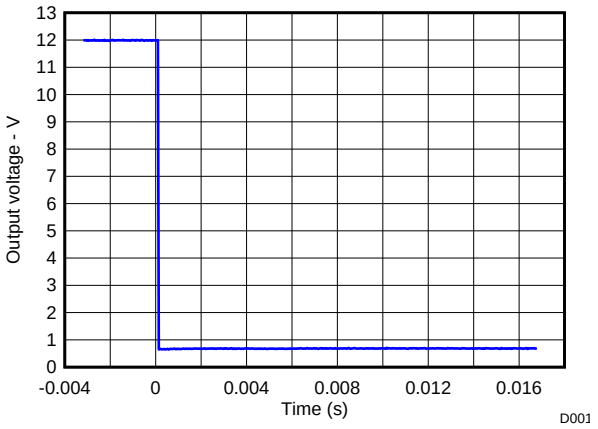


Figure 23. Output Response With Activation of Coil (Turnon)

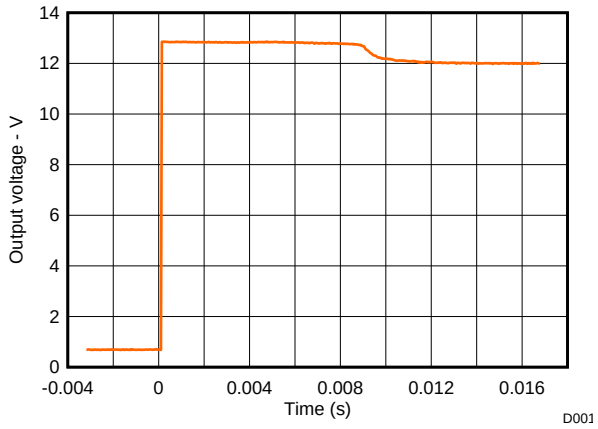


Figure 24. Output Response With De-activation of Coil (Turnoff)

9.3 System Examples

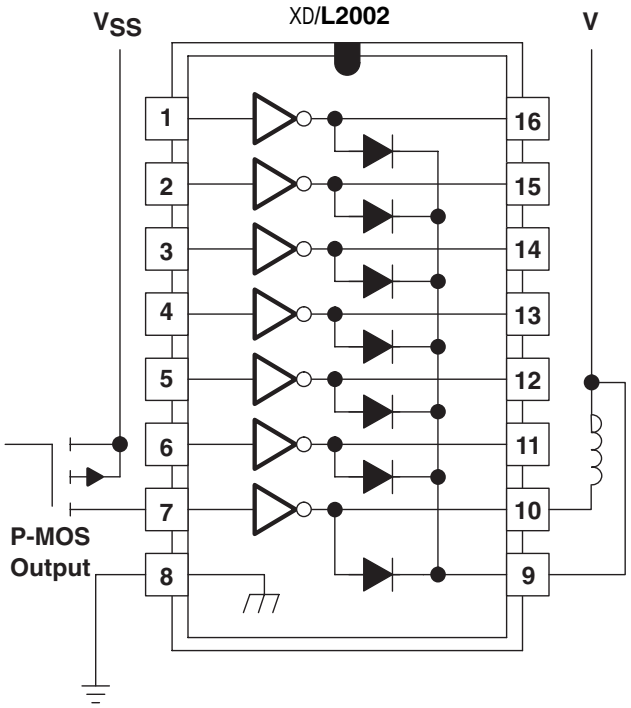


Figure 25. P-MOS to Load

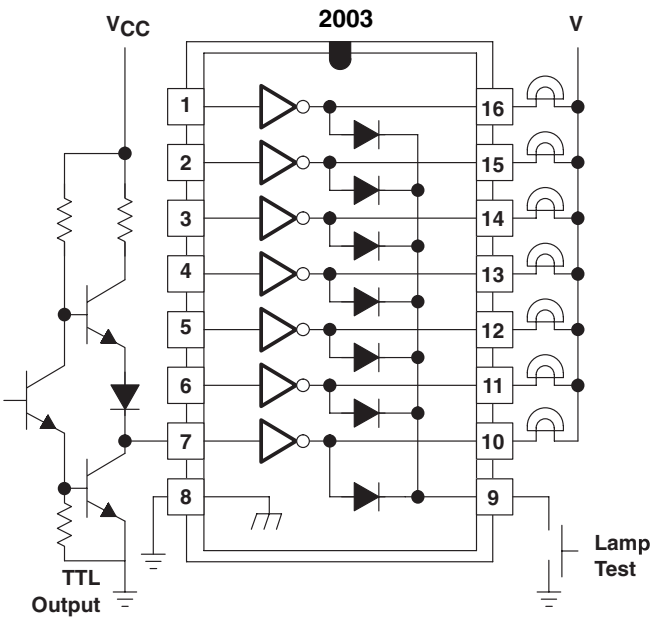


Figure 26. TTL to Load

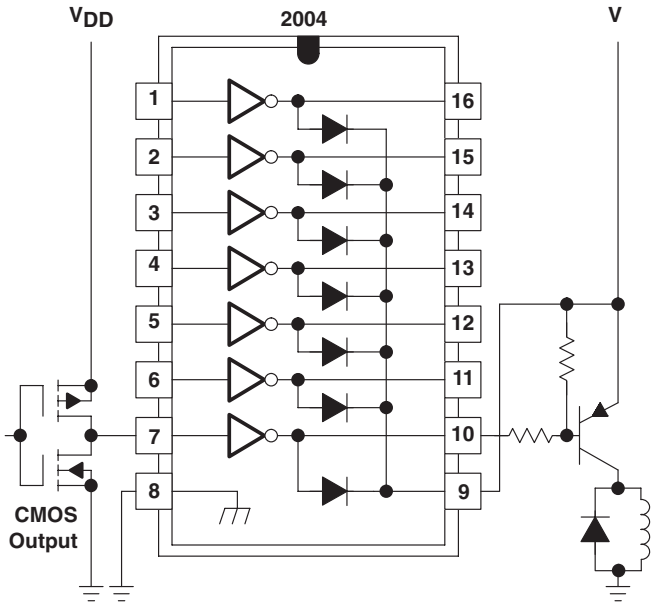


Figure 27. Buffer for Higher Current Loads

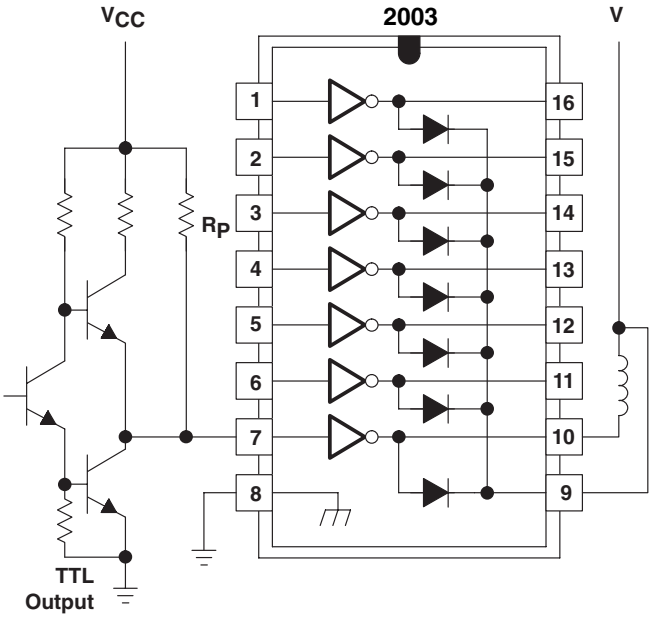


Figure 28. Use of Pullup Resistors to Increase Drive Current

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA

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