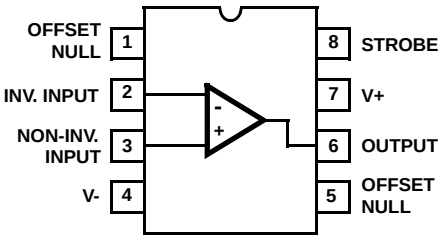
## 4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

The 3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The 3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The 3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The 3140 are intended for operation at supply voltages up to 36V (±18V).

**3140 DIP/SOP**
TOP VIEW




## Features

- MOSFET Input Stage
  - Very High Input Impedance ($Z_{IN}$) -1.5TΩ (Typ)
  - Very Low Input Current ($I_I$) -10pA (Typ) at ±15V
  - Wide Common Mode Input Voltage Range ($V_{ICR}$) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Applications

- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (μseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

## Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) . . . . . 36V
Differential Mode Input Voltage . . . . . 8V
DC Input Voltage . . . . . (V+ +8V) To (V- -0.5V)
Input Terminal Current . . . . . 1mA
Output Short Circuit Duration∞ (Note 2) . . . . . Indefinite

Operating Conditions
Temperature Range . . . . . $-55^oC$ to $125^oC$

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^oC/W$) | $\theta_{JC}$ ($^oC/W$) |
|---|---|---|
| PDIP Package* | 115 | N/A |
| SOIC Package | 165 | N/A |

Maximum Junction Temperature (Plastic Package) . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details
2. Short circuit may be applied to ground or to either supply.

## Electrical Specifications

$V_{SUPPLY} = \pm15V$, $T_A = 25^oC$

| PARAMETER | SYMBOL | TEST CONDITIONS | | TYPICAL VALUES 3140 | | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage Adjustment Resistor | | Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max $V_{IO}$ | | 4.7 | 18 | kΩ |
| Input Resistance | $R_I$ | | | 1.5 | 1.5 | TΩ |
| Input Capacitance | $C_I$ | | | 4 | 4 | pF |
| Output Resistance | $R_O$ | | | 60 | 60 | Ω |
| Equivalent Wideband Input Noise Voltage (See Figure 27) | $e_N$ | BW = 140kHz, $R_S$ = 1MΩ | | 48 | 48 | µV |
| Equivalent Input Noise Voltage (See Figure 35) | $e_N$ | $R_S$ = 100Ω | f = 1kHz | 40 | 40 | $nV/\sqrt{Hz}$ |
| | | | f = 10kHz | 12 | 12 | $nV/\sqrt{Hz}$ |
| Short Circuit Current to Opposite Supply | $I_{OM}+$ | | Source | 40 | 40 | mA |
| | $I_{OM}-$ | | Sink | 18 | 18 | mA |
| Gain-Bandwidth Product, (See Figures 6, 30) | $f_T$ | | | 4.5 | 4.5 | MHz |
| Slew Rate, (See Figure 31) | SR | | | 9 | 9 | V/µs |
| Sink Current From Terminal 8 To Terminal 4 to Swing Output Low | | | | 220 | 220 | µA |
| Transient Response (See Figure 28) | $t_r$ | $R_L$ = 2kΩ, $C_L$ = 100pF | Rise Time | 0.08 | 0.08 | µs |
| | OS | | Overshoot | 10 | 10 | % |
| Settling Time at $10V_{P-P}$, (See Figure 5) | $t_S$ | $R_L$ = 2kΩ, $C_L$ = 100pF, Voltage Follower | To 1mV | 4.5 | 4.5 | µs |
| | | | To 10mV | 1.4 | 1.4 | µs |

## Electrical Specifications

For Equipment Design, at $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | 3140 MIN | 3140 TYP | 3140 MAX | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $\|V_{IO}\|$ | - | 5 | 15 | - | 2 | 5 | mV |
| Input Offset Current | $\|I_{IO}\|$ | - | 0.5 | 30 | - | 0.5 | 20 | pA |
| Input Current | $I_I$ | - | 10 | 50 | - | 10 | 40 | pA |

## Electrical Specifications For Equipment Design, at $V_{SUPPLY}$ = ±15V, $T_A$ = 25°C, Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | 3140 | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Large Signal Voltage Gain (Note 3) (See Figures 6, 29) | $A_{OL}$ | 20 | 100 | - | 20 | 100 | - | kV/V |
| | | 86 | 100 | - | 86 | 100 | - | dB |
| Common Mode Rejection Ratio (See Figure 34) | CMRR | - | 32 | 320 | - | 32 | 320 | µV/V |
| | | 70 | 90 | - | 70 | 90 | - | dB |
| Common Mode Input Voltage Range (See Figure 8) | $V_{ICR}$ | -15 | -15.5 to +12.5 | 11 | -15 | -15.5 to +12.5 | 12 | V |
| Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 36) | PSRR | - | 100 | 150 | - | 100 | 150 | µV/V |
| | | 76 | 80 | - | 76 | 80 | - | dB |
| Max Output Voltage (Note 4) (See Figures 2, 8) | $V_{OM}$+ | +12 | 13 | - | +12 | 13 | - | V |
| | $V_{OM}$- | -14 | -14.4 | - | -14 | -14.4 | - | V |
| Supply Current (See Figure 32) | I+ | - | 4 | 6 | - | 4 | 6 | mA |
| Device Dissipation | $P_D$ | - | 120 | 180 | - | 120 | 180 | mW |
| Input Offset Voltage Temperature Drift | $\Delta V_{IO}/\Delta T$ | - | 8 | - | - | 6 | - | µV/°C |

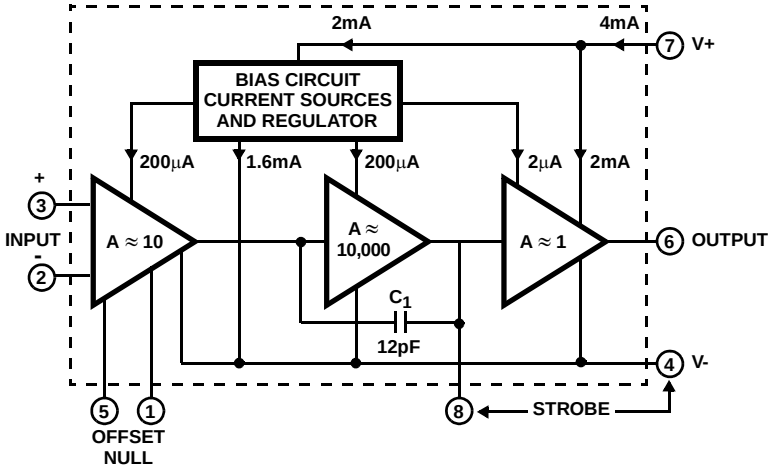
NOTES:

3. At $V_O$ = 26$V_{P-P}$, +12V, -14V and $R_L$ = 2kΩ.
4. At $R_L$ = 2kΩ.

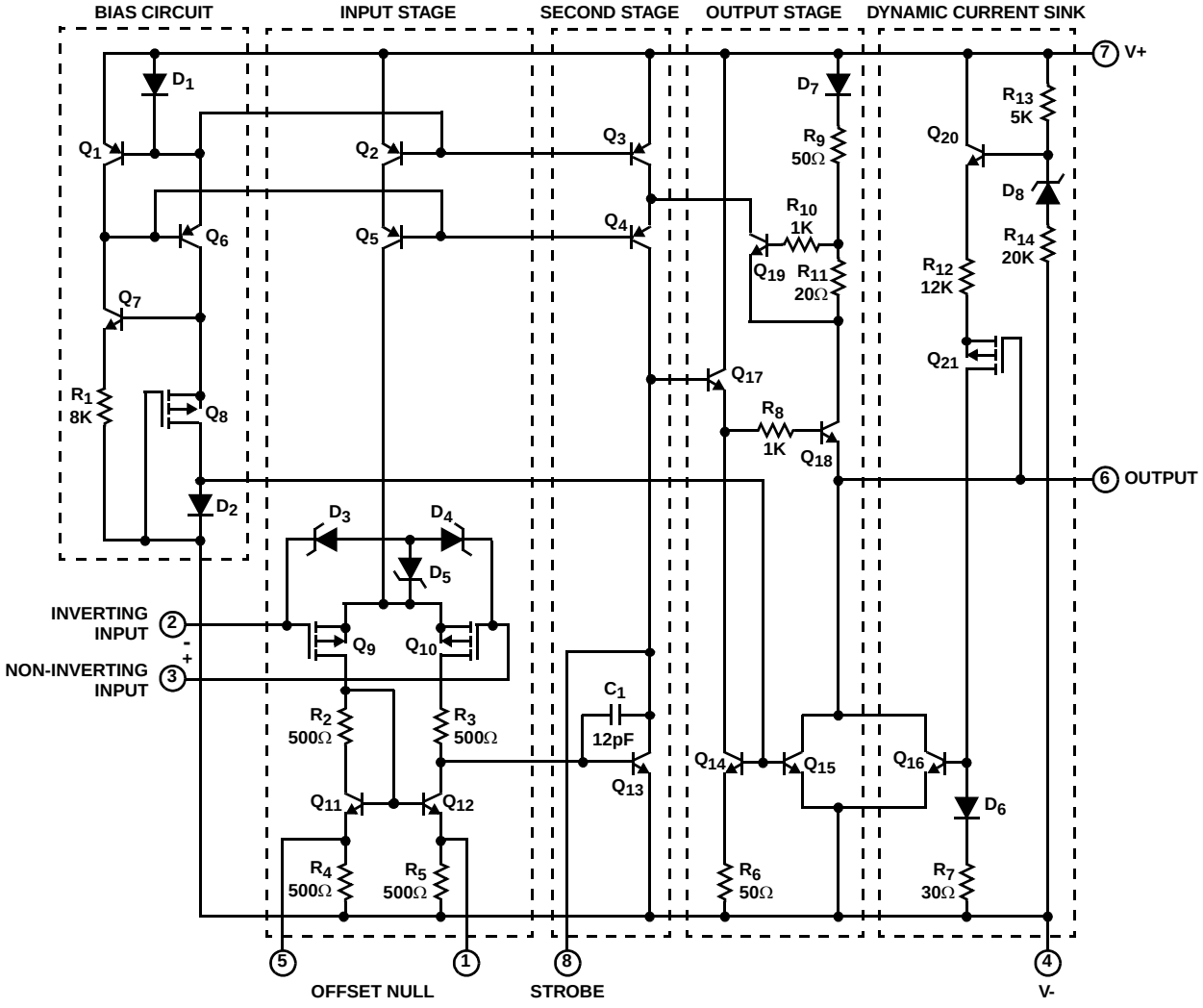
## Electrical Specifications For Design Guidance At V+ = 5V, V- = 0V, $T_A$ = 25°C

| PARAMETER | | SYMBOL | TYPICAL VALUES 3140 | | UNITS |
|---|---|---|---|---|---|
| Input Offset Voltage | | $\|V_{IO}\|$ | 5 | 2 | mV |
| Input Offset Current | | $\|I_{IO}\|$ | 0.1 | 0.1 | pA |
| Input Current | | $I_I$ | 2 | 2 | pA |
| Input Resistance | | $R_I$ | 1 | 1 | TΩ |
| Large Signal Voltage Gain (See Figures 6, 29) | | $A_{OL}$ | 100 | 100 | kV/V |
| | | | 100 | 100 | dB |
| Common Mode Rejection Ratio | | CMRR | 32 | 32 | µV/V |
| | | | 90 | 90 | dB |
| Common Mode Input Voltage Range (See Figure 8) | | $V_{ICR}$ | -0.5 | -0.5 | V |
| | | | 2.6 | 2.6 | V |
| Power Supply Rejection Ratio | | PSRR $\Delta V_{IO}/\Delta V_S$ | 100 | 100 | µV/V |
| | | | 80 | 80 | dB |
| Maximum Output Voltage (See Figures 2, 8) | | $V_{OM}$+ | 3 | 3 | V |
| | | $V_{OM}$- | 0.13 | 0.13 | V |
| Maximum Output Current: | Source | $I_{OM}$+ | 10 | 10 | mA |
| | Sink | $I_{OM}$- | 1 | 1 | mA |
| Slew Rate (See Figure 31) | | SR | 7 | 7 | V/µs |
| Gain-Bandwidth Product (See Figure 30) | | $f_T$ | 3.7 | 3.7 | MHz |
| Supply Current (See Figure 32) | | I+ | 1.6 | 1.6 | mA |
| Device Dissipation | | $P_D$ | 8 | 8 | mW |
| Sink Current from Terminal 8 to Terminal 4 to Swing Output Low | | | 200 | 200 | µA |

## *Block Diagram*




## *Schematic Diagram*




NOTE: All resistance values are in ohms.

### *Output Circuit Considerations*

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to Terminal 8 as shown in Figure 1. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the 3140 . These voltages are independent of the operating supply voltage.

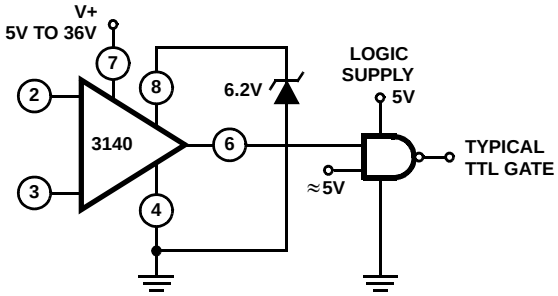



**FIGURE 1. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT 3140 OUTPUT SWING TO TTL LEVELS**

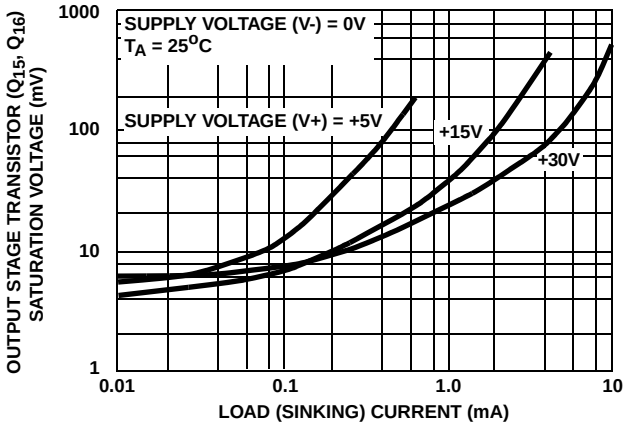



**FIGURE 2. VOLTAGE ACROSS OUTPUT TRANSISTORS ($Q_{15}$ AND $Q_{16}$) vs LOAD CURRENT**

Figure 2 shows output current sinking capabilities of the 3140 at various supply volt ages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 4 shows some typical configurations. Note that a series resistor, $R_L$, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

### *Offset Voltage Nulling*

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between Terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 3A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors (R) that may be placed at either end of the potentiometer, see Figure 3B, to optimize its utilization range are given in the Electrical Specifications table.

An alternate system is shown in Figure 3C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

### *Low Voltage Operation*

Operation at total supply voltages as low as 4V is possible with the 3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the voltage at Terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 8 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

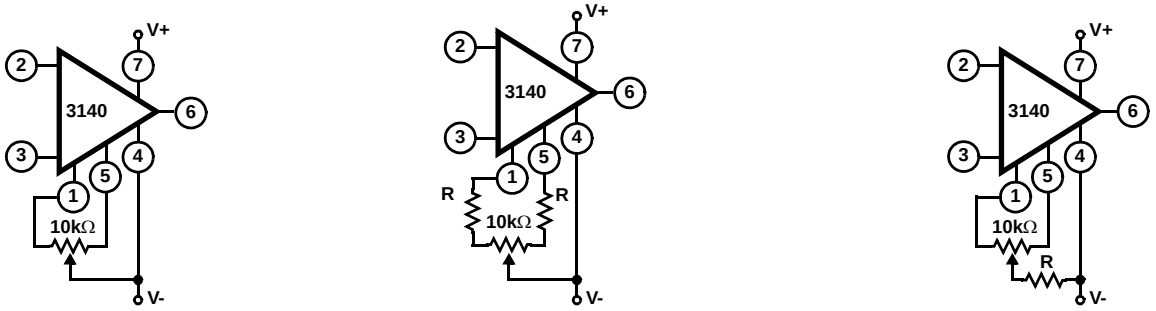



**FIGURE 3A. BASIC** **FIGURE 3B. IMPROVED RESOLUTION** **FIGURE 3C. SIMPLER IMPROVED RESOLUTION**

**FIGURE 3. THREE OFFSET VOLTAGE NULLING METHODS**

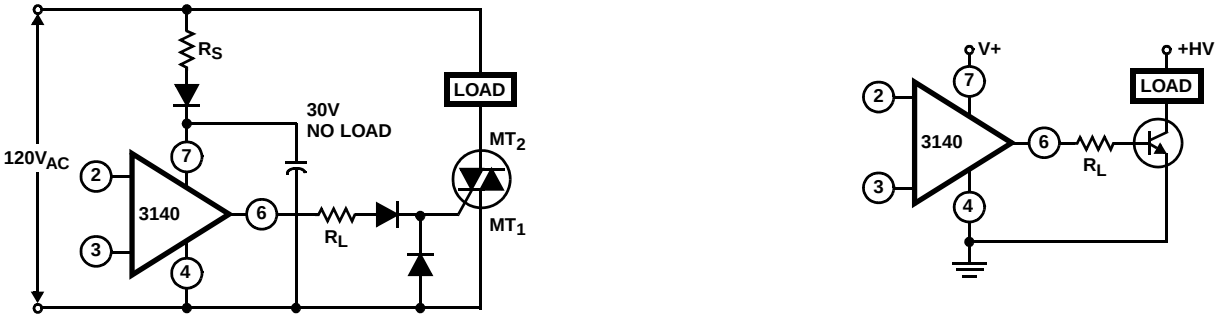



**FIGURE 4. METHODS OF UTILIZING THE $V_{CE(SAT)}$ SINKING CURRENT CAPABILITY OF THE 3140 SERIES**

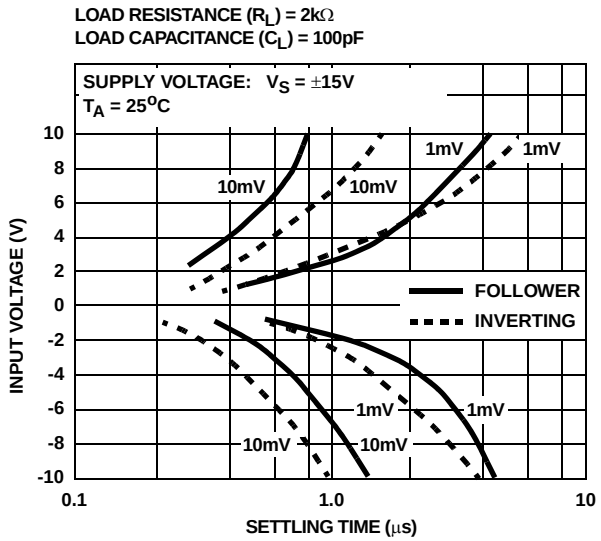



**FIGURE 5A. WAVEFORM**

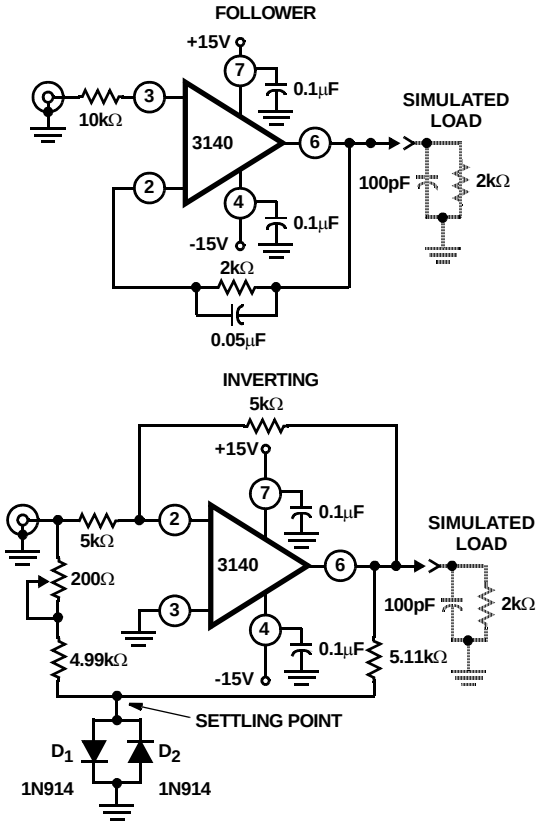



**FIGURE 5B. TEST CIRCUITS**

**FIGURE 5. SETTLING TIME vs INPUT VOLTAGE**

### *Bandwidth and Slew Rate*

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between Terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 5 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers.

The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the 3140; as shown in Figure 6.

### *Input Circuit Considerations*

As mentioned previously, the amplifier inputs can be driven below the Terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when

the 3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and directly driving the internal constant current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

The typical input current is on the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Figure 7 shows typical input terminal current versus ambient temperature for the 3140.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Figure 9 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for metal can); at lower temperatures (metal can and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

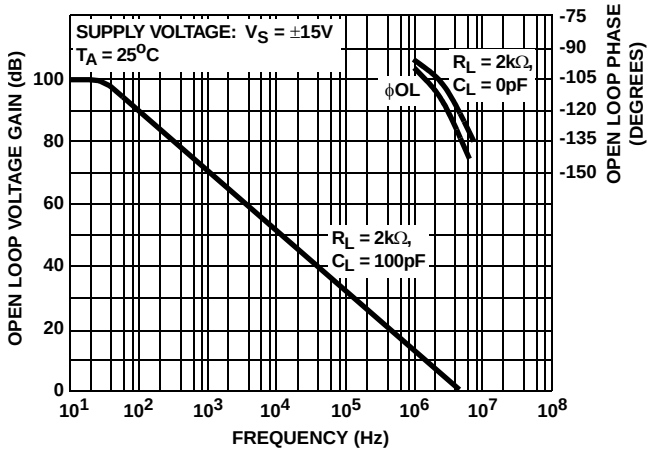



**FIGURE 6. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY**

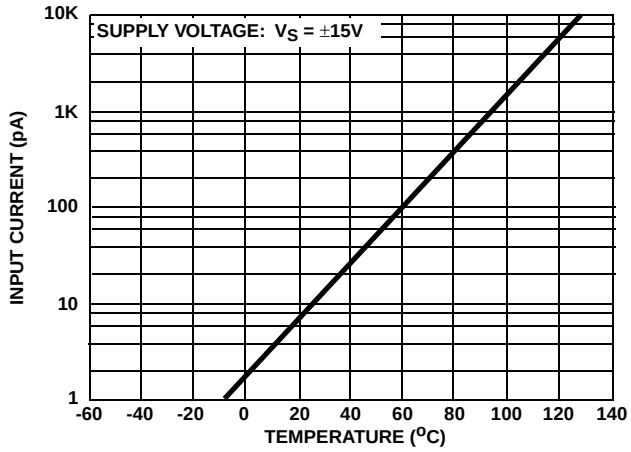



**FIGURE 7. INPUT CURRENT vs TEMPERATURE**

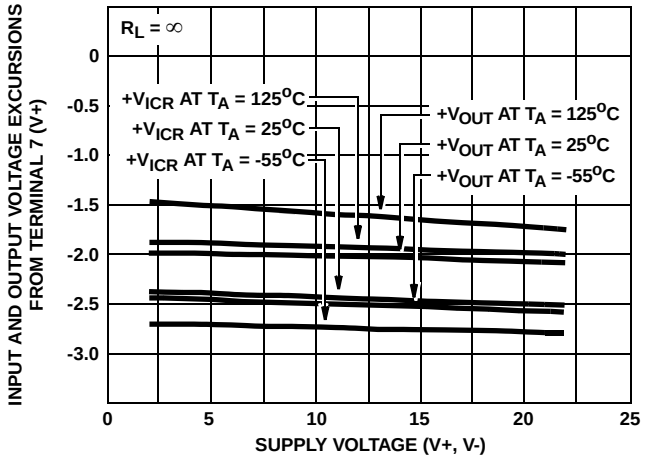



**FIGURE 8. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE**

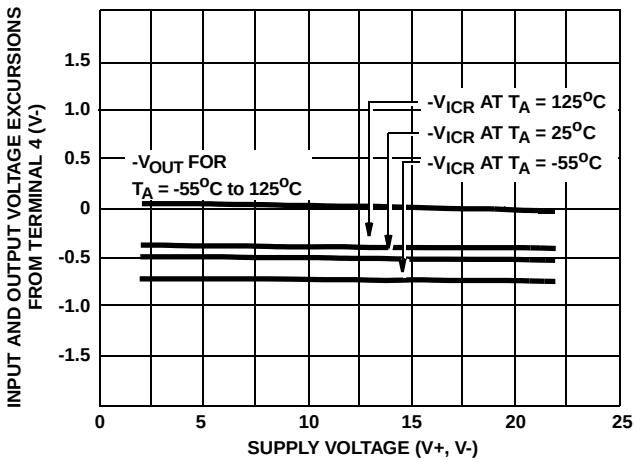



**FIGURE 9.**

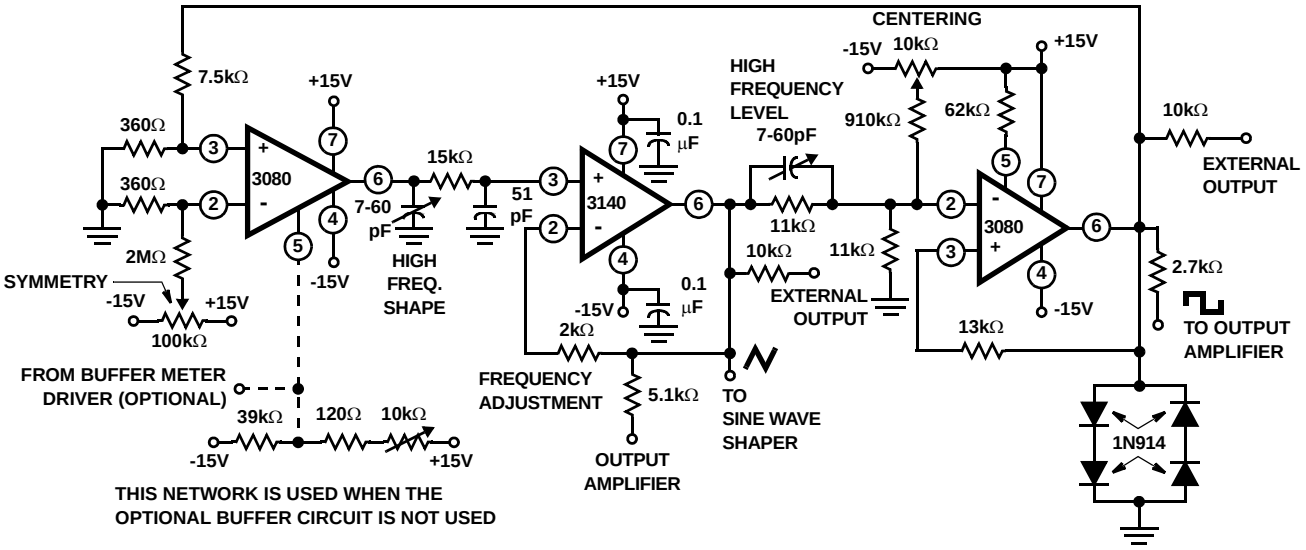
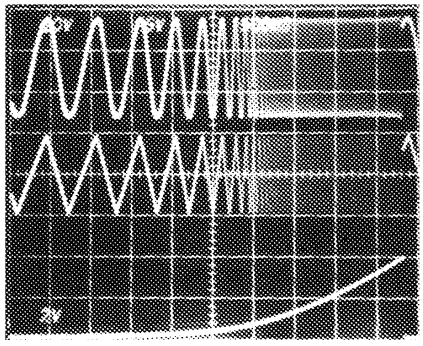



**FIGURE 10A. CIRCUIT**

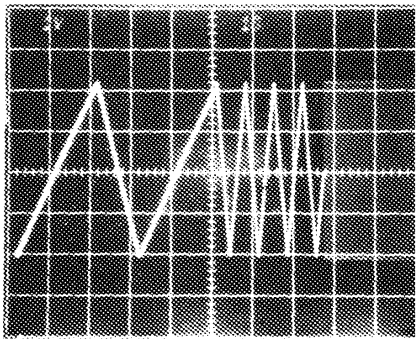


Top Trace: Output at junction of 2.7Ω and 51Ω resistors; 5V/Div., 500ms/Div.

Center Trace: External output of triangular function generator; 2V/Div., 500ms/Div.

Bottom Trace: Output of “Log” generator; 10V/Div., 500ms/Div.

**FIGURE 10B. FIGURE FUNCTION GENERATOR SWEEPING**



1V/Div., 1s/Div.

Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the 3080 and from the PC board and component leakages at the 100pA level.

**FIGURE 10C. FUNCTION GENERATOR WITH FIXED FREQUENCIES**

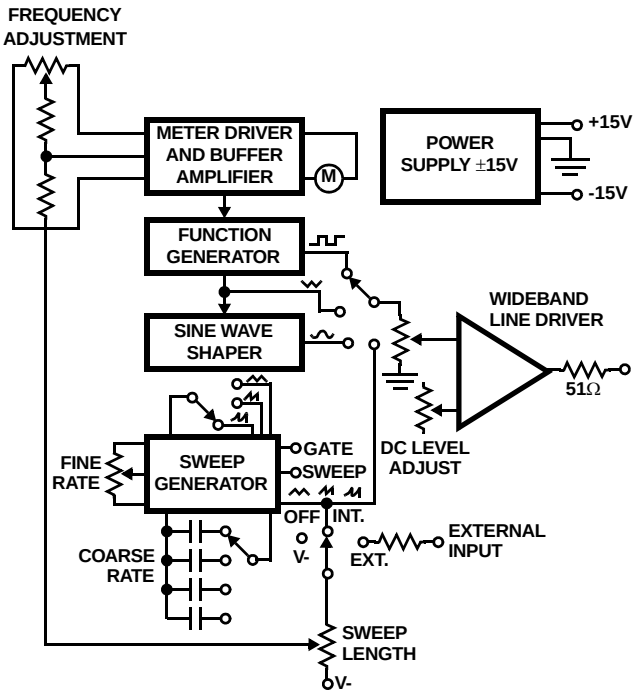



**FIGURE 10D. INTERCONNECTIONS**

**FIGURE 10. FUNCTION GENERATOR**

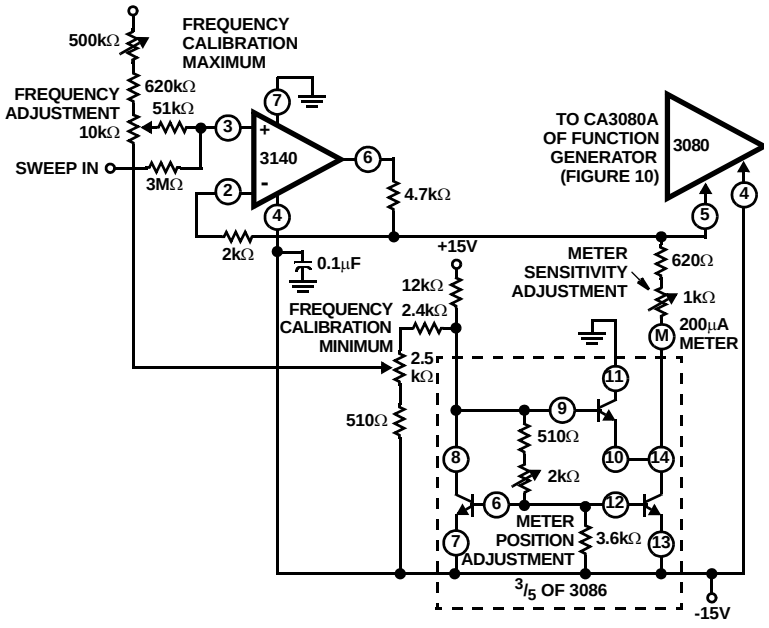



FIGURE 11. METER DRIVER AND BUFFER AMPLIFIER

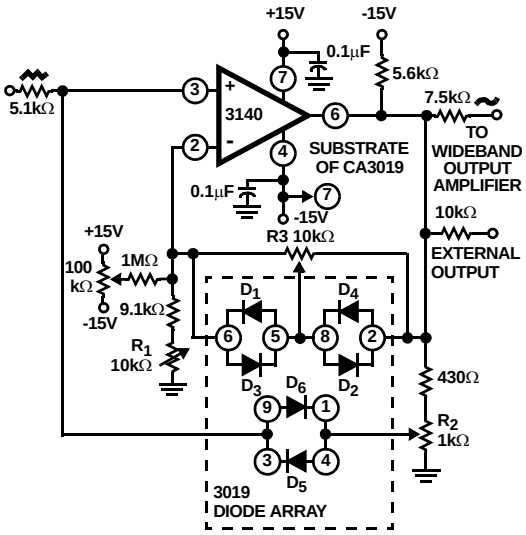



FIGURE 12. SINE WAVE SHAPER

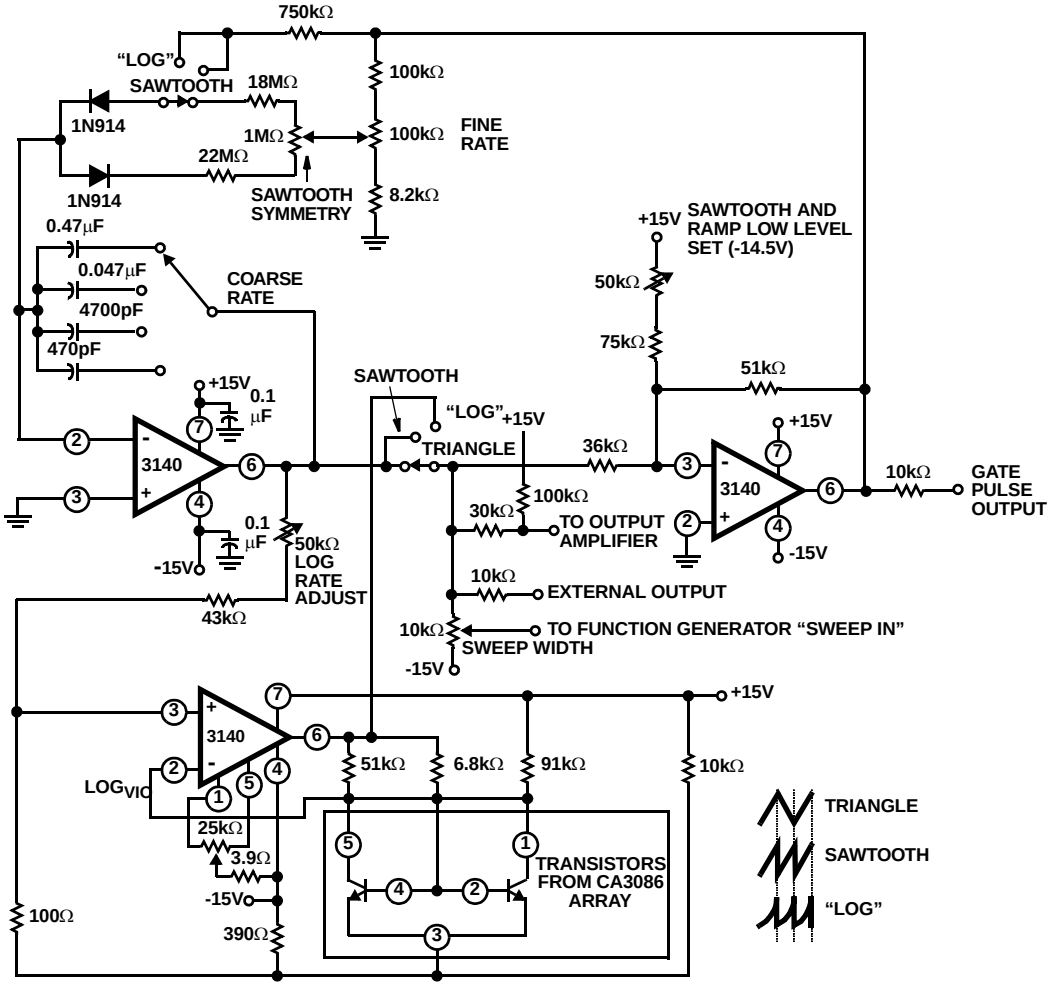



FIGURE 13. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer $R_1$, followed by an adjustment of $R_2$. The final slope is established by adjusting $R_3$, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

**Sweeping Generator**

Figure 13 shows a sweeping generator. Three 3140 are used in this circuit. One 3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third 3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

**Wideband Output Amplifier**

Figure 14 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 10 and 12 provides $18V_{P-P}$ output open circuited, or $9V_{P-P}$ output when terminated in 50Ω. The slew rate required of this amplifier is 28V/μs ($18V_{P-P}$ x π x 0.5MHz).

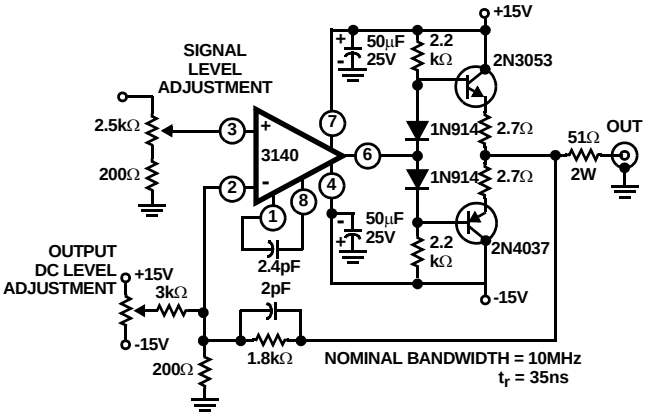



**FIGURE 14. WIDEBAND OUTPUT AMPLIFIER**

**Power Supplies**

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in connection with the 3140 (see Figure 15).

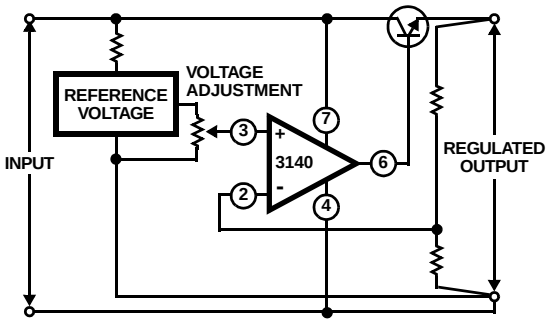



**FIGURE 15. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION**

Essentially, the regulators, shown in Figures 16 and 17, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high $I_{CBO}$ levels will also prevent the output voltage from reaching zero because there is a finite voltage drop ($V_{CESAT}$) across the output of the 3140 (see Figure 2). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by Terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the 3140 in the event of unusual input or output transients on the supply rail.

Figures 16 and 17, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a metal can with heatsink), is used as the series pass element for the conventional current limiting system, Figure 16, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 17, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

Both regulators provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200μV as read with a meter having a 10MHz bandwidth.

Figure 18A shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 18B shows the transient response of the regulator with the switching of a 20Ω load at 20V output.

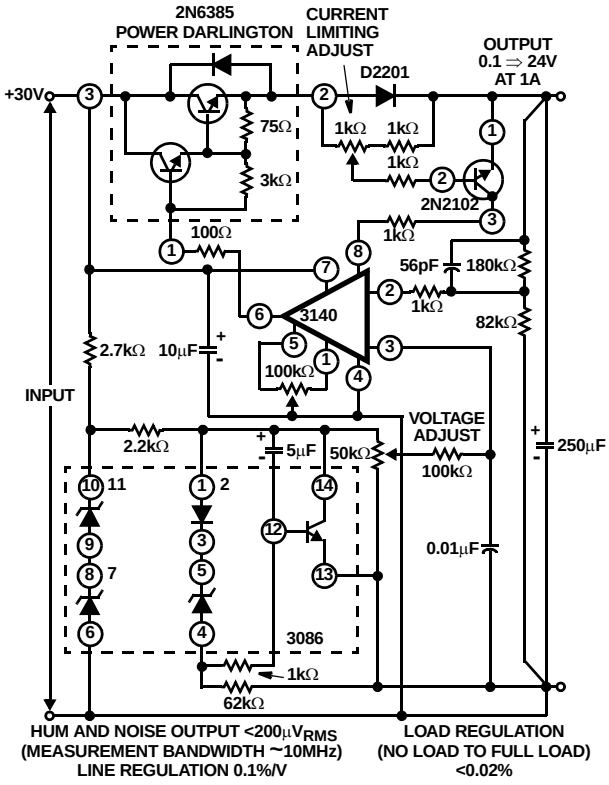



**FIGURE 16. REGULATED POWER SUPPLY**

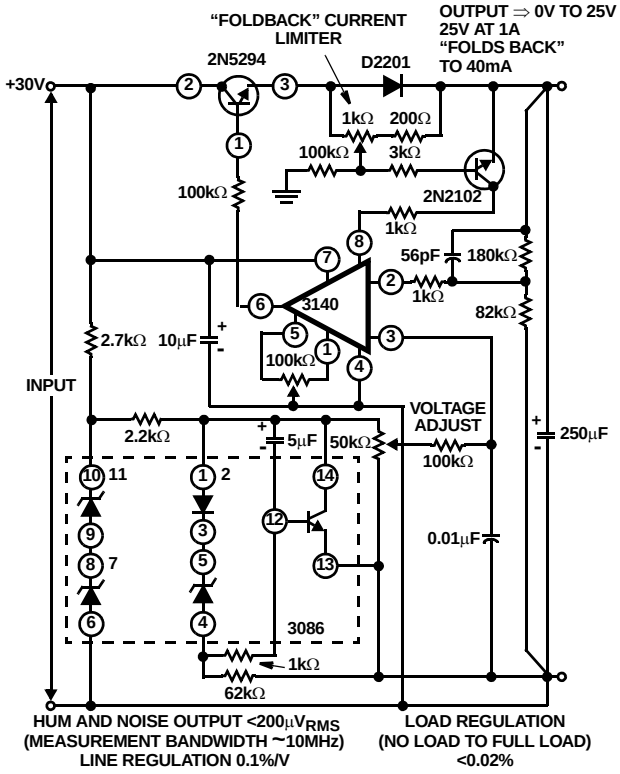
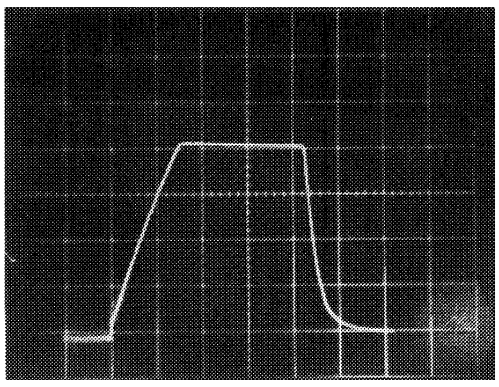
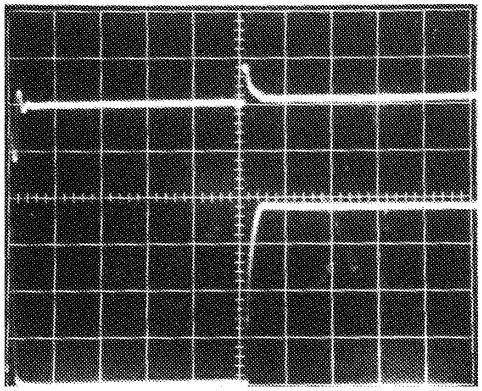



**FIGURE 17. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING**



5V/Div., 1s/Div.

**FIGURE 18A. SUPPLY TURN-ON AND TURNOFF CHARACTERISTICS**



Top Trace: Output Voltage;
200mV/Div., 5μs/Div.

Bottom Trace: Collector of load switching transistor, load = 1A;
5V/Div., 5μs/Div.

**FIGURE 18B. TRANSIENT RESPONSE**

**FIGURE 18. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 16 AND 17**

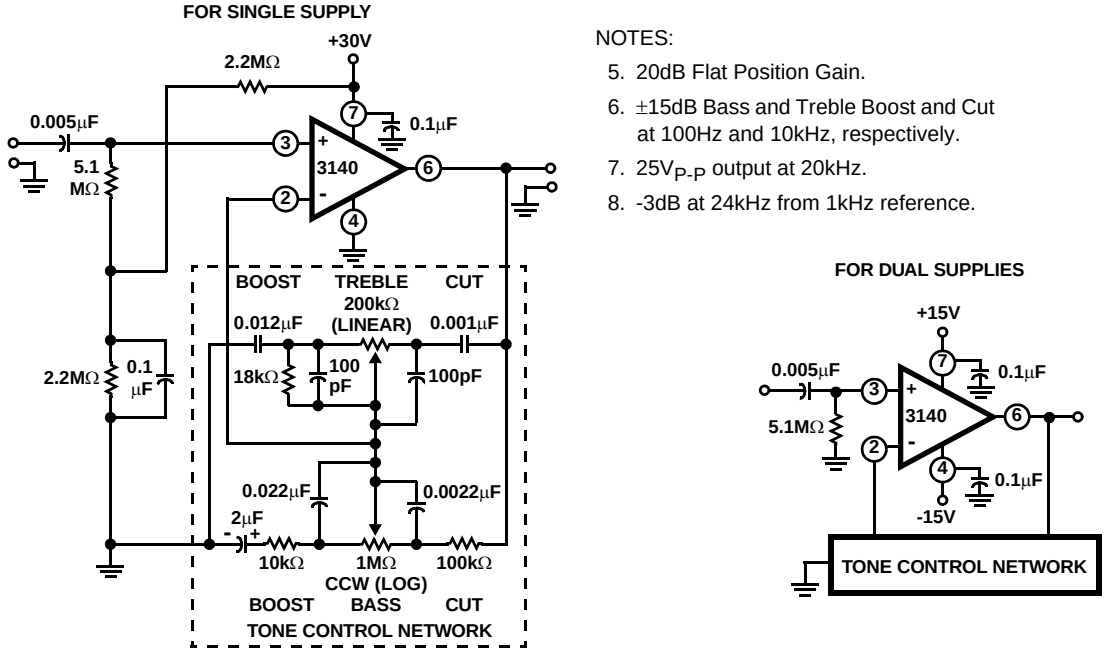
### *Tone Control Circuits*

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the 3140 are shown in Figures 19 and 20.

The first circuit, shown in Figure 20, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the 3140 makes possible the use of low-cost, low-value, small size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the 3140. The amplifier gain is 3dB down from its “flat” position at 70kHz.

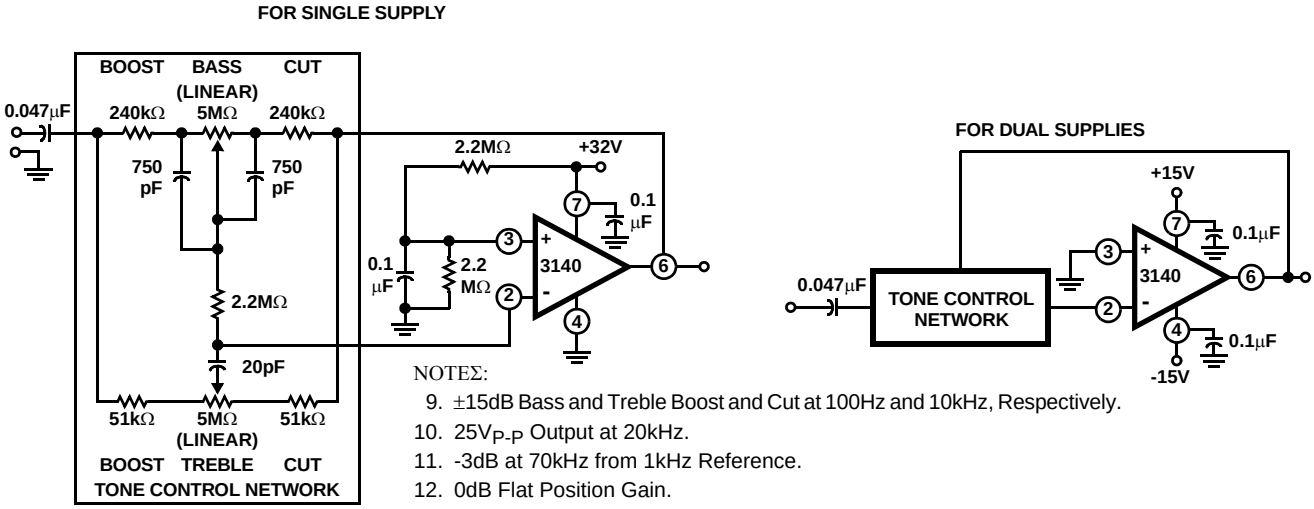
Figure 19 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from Terminal No. 3 to ground. A detailed analysis of this circuit is given in “An IC Operational Transconductance Amplifier (OTA) With Power Capability” by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.




NOTES:

5. 20dB Flat Position Gain.
6. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, respectively.
7. $25V_{P-P}$ output at 20kHz.
8. -3dB at 24kHz from 1kHz reference.

**FIGURE 19. TONE CONTROL CIRCUIT USING CA3130 SERIES (20dB MIDBAND GAIN)**



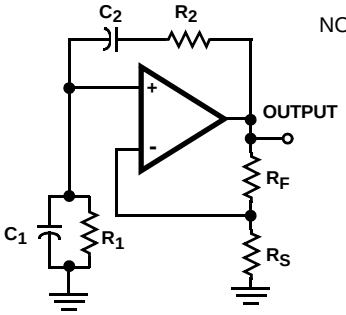

NOTES:

9. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, Respectively.
10. $25V_{P-P}$ Output at 20kHz.
11. -3dB at 70kHz from 1kHz Reference.
12. 0dB Flat Position Gain.

**FIGURE 20. BAXANDALL TONE CONTROL CIRCUIT USING CA3140 SERIES**

### *Wien Bridge Oscillator*

Another application of the 3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 21. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/(2\pi RC)$ and the gain required for oscillation, $A_{OSC}$ is equal to 3. Note that if $C_2$ is increased by a factor of four and $R_2$ is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the 3140.




NOTES:

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$A_{OSC} = 1 + \frac{C_1}{C_2} + \frac{R_2}{R_1}$$

$$A_{CL} = 1 + \frac{R_F}{R_S}$$

**FIGURE 21. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER**

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, $R_S$, is commonly replaced with some variable resistance element. Thus, through some control means, the value of $R_S$ is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance increases as the output amplitude is increased are a few of the elements often utilized.

Figure 22 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor ($R_F$ of Figure 21). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1µF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180kHz will reach a slew rate of approximately 9V/µs when its amplitude is $16V_{P-P}$.

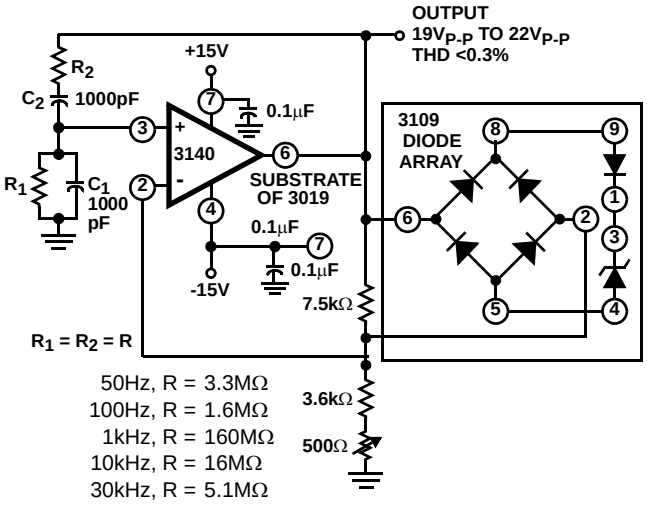



**FIGURE 22. WIEN BRIDGE OSCILLATOR CIRCUIT USING 3140**

### Simple Sample-and-Hold System

Figure 23 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The 3080A serves as both input buffer amplifier and low feed-through transmission switch (see Note 13). System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2kΩ and 30pF is shown in the schematic.

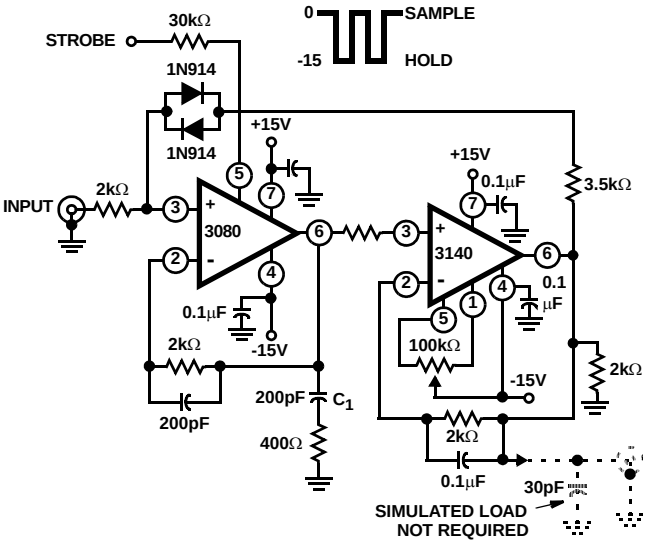



**FIGURE 23. SAMPLE AND HOLD CIRCUIT**

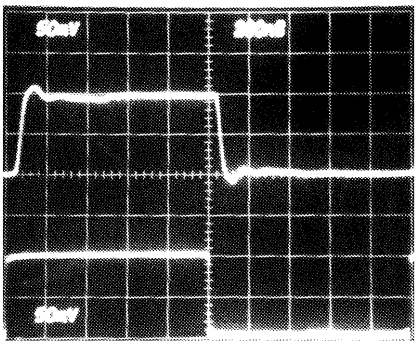
In this circuit, the storage compensation capacitance ($C_1$) is only 200pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate is:

$$\frac{dv}{dt} = \frac{I}{C} = 0.5mA/200pF = 2.5V/\mu s$$

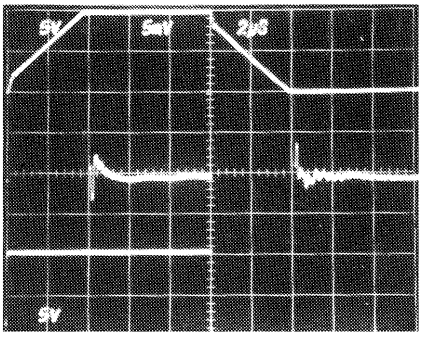
NOTE:

13. AN6668 "Applications of the 3080 and 3080 High Performance Operational Transconductance Amplifiers".

Pulse “droop” during the hold interval is 170pA/200pF which is 0.85μV/μs; (i.e., 170pA/200pF). In this case, 170pA represents the typical leakage current of the 3080 when strobed off. If $C_1$ were increased to 2000pF, the “hold-droop” rate will decrease to 0.085μV/μs, but the slew rate would decrease to 0.25V/μs. The parallel diode network connected between Terminal 3 of the 3080 and Terminal 6 of the 3140 prevents large input signal feedthrough across the input terminals of the 3080 to the 200pF storage capacitor when the 3080 is strobed off. Figure 24 shows dynamic characteristic waveforms of this sample-and-hold system.

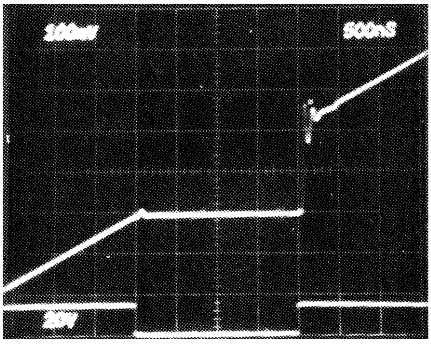


Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.



Top Trace: Output Signal; 5V/Div, 2μs/Div.
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div., 2μs/Div.
Bottom Trace: Input Signal; 5V/Div., 2μs/Div.

**LARGE SIGNAL RESPONSE AND SETTLING TIME**



**SAMPLING RESPONSE**

Top Trace: Output; 100mV/Div., 500ns/Div.
Bottom Trace: Input; 20V/Div., 500ns/Div.

**FIGURE 24. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS**

### *Current Amplifier*

The low input terminal current needed to drive the 3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 25 (see Note 14). In this circuit, low current is supplied at the input potential as the power supply to load resistor $R_L$. This load current is increased by the multiplication factor $R_2/R_1$, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100μA; a much easier current to measure in many systems.

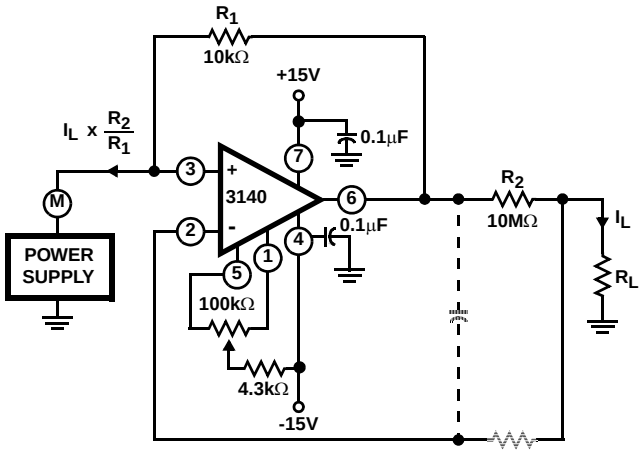



**FIGURE 25. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS**

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

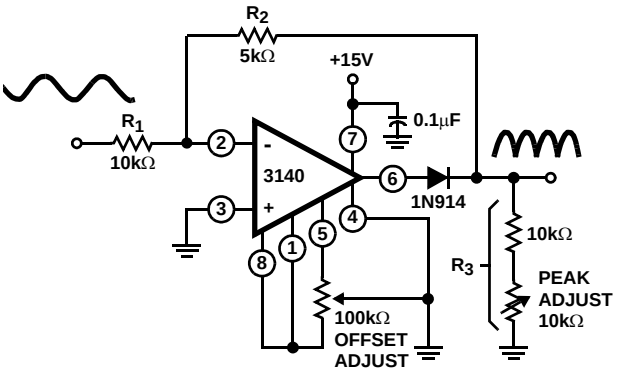
The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

### Full Wave Rectifier

Figure 26 shows a single supply, absolute value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the 3140 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 26 is satisfied, the full wave output is symmetrical.

NOTE:

14. “Operational Amplifiers Design and Applications”, J. G. Graeme, McGraw-Hill Book Company, page 308, “Negative Immittance Converter Circuits”.




$$GAIN = \frac{R_2}{R_1} = X = \frac{R_3}{R_1R_2 + R_3}$$

$$R_3 = \left(\frac{X + X^2}{1 - X}\right)R_1$$

$$\text{FOR } X = 0.5 \quad \frac{5k\Omega}{10k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 10k\Omega\left(\frac{0.75}{0.5}\right) = 15k\Omega$$

$20V_{P-P}$ Input BW (-3dB) = 290kHz, DC Output (Avg) = 3.2V

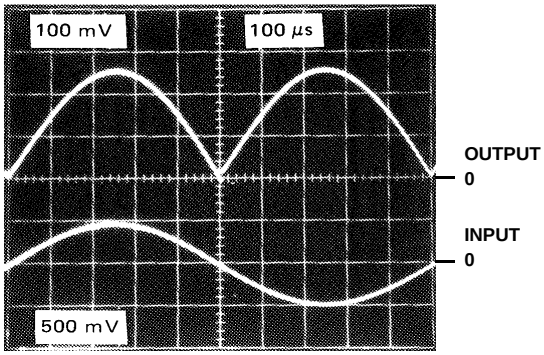



**FIGURE 26. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS**

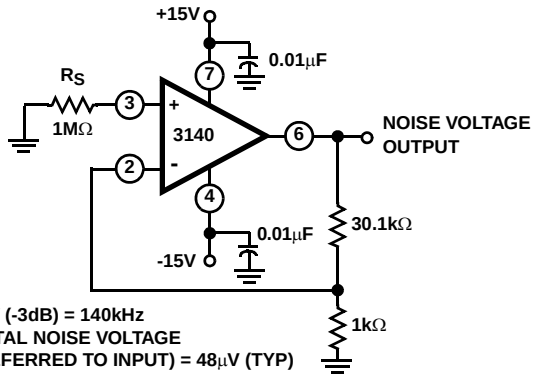



**FIGURE 27. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT**

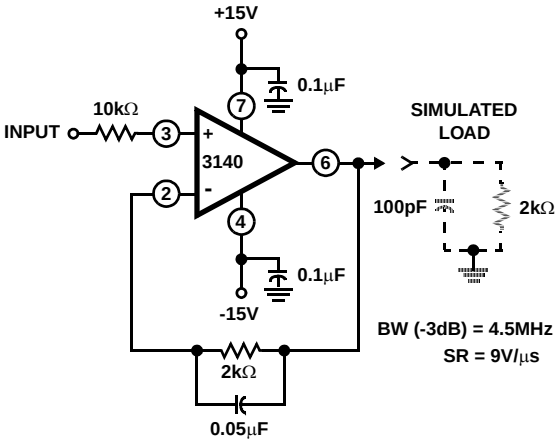
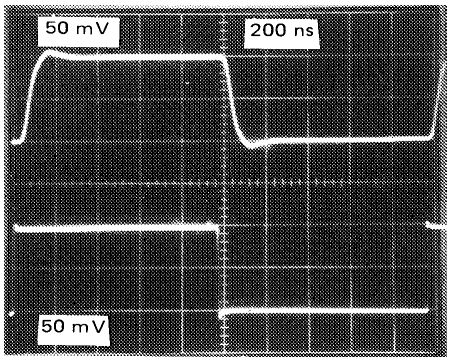
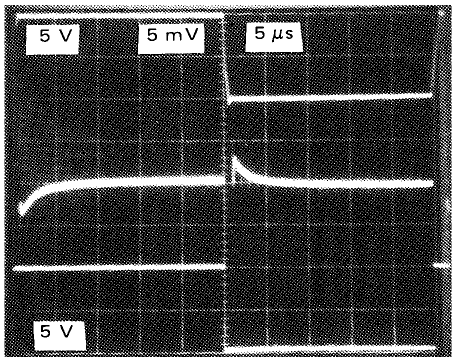



**FIGURE 28A. TEST CIRCUIT**




Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.

**FIGURE 28B. SMALL SIGNAL RESPONSE**




(Measurement made with Tektronix 7A13 differential amplifier.)

Top Trace: Output Signal; 5V/Div., 5μs/Div.
Center Trace: Difference Signal; 5mV/Div., 5μs/Div.
Bottom Trace: Input Signal; 5V/Div., 5μs/Div.

**FIGURE 28C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME**

**FIGURE 28. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS**

## *Typical Performance Curves*

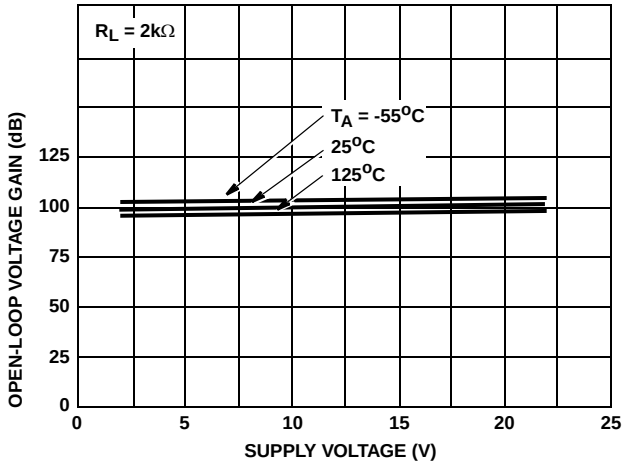



FIGURE 29. OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

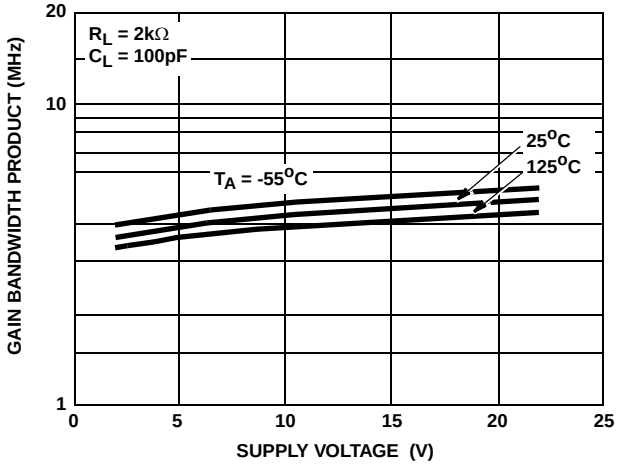



FIGURE 30. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

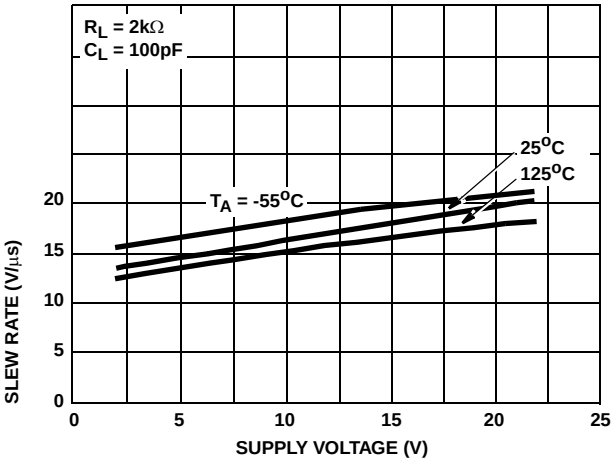



FIGURE 31. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

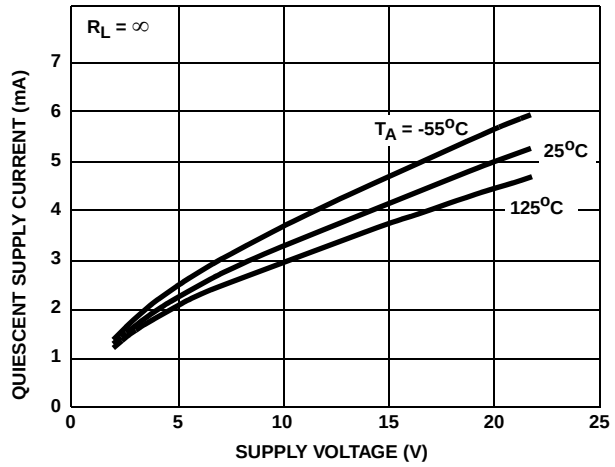



FIGURE 32. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

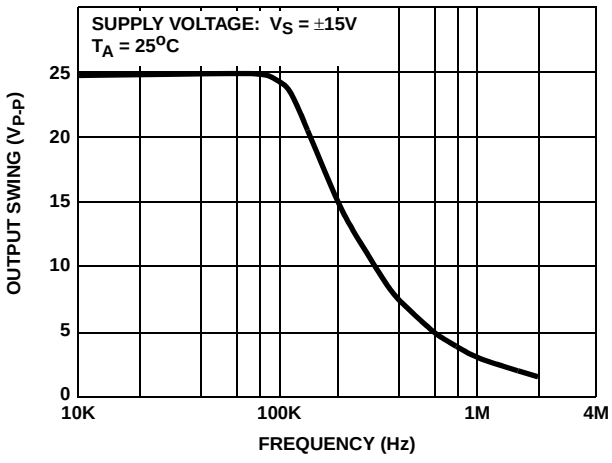



FIGURE 33. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

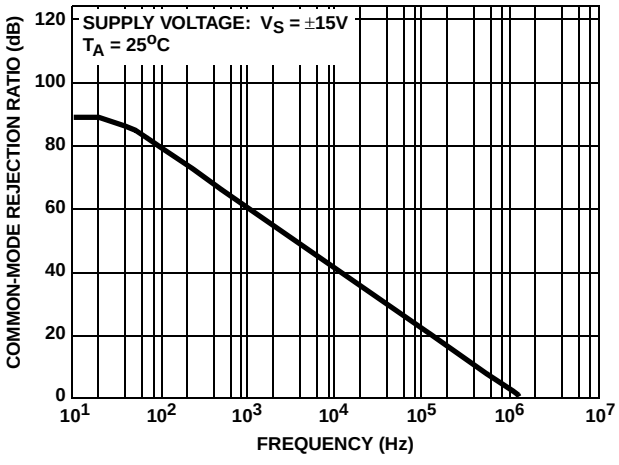



FIGURE 34. COMMON MODE REJECTION RATIO vs FREQUENCY

## *Typical Performance Curves* (Continued)

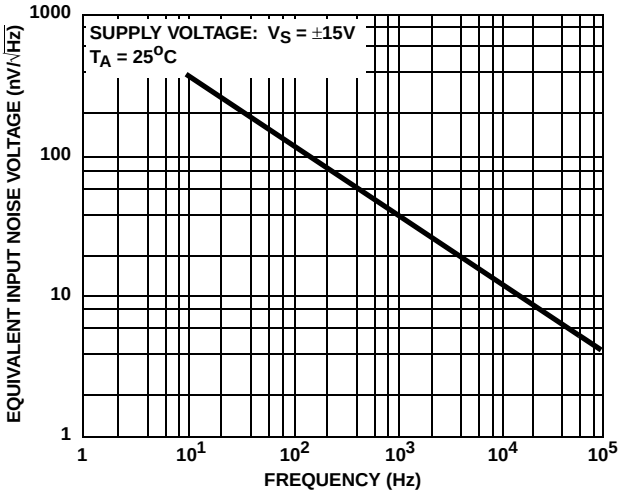



FIGURE 35. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

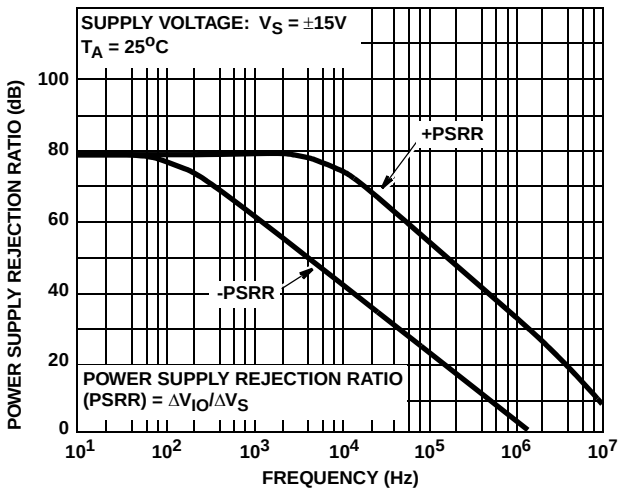



FIGURE 36. POWER SUPPLY REJECTION RATIO vs FREQUENCY

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