1. General description

The XD4069 is a general purpose hex unbuffered inverter. Each inverter has a single stage.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C and –40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Oscillator

4. Functional diagram

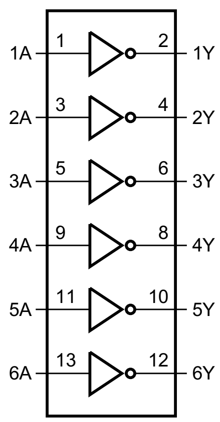


Fig 1. Functional diagram

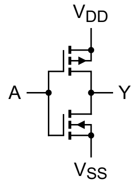


Fig 2. Schematic diagram (one inverter)

5. Pinning information

5.1 Pinning

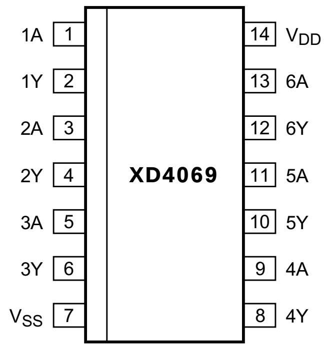


Fig 3. Pin configuration

5.2 Pin description

Table 1. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	input
1Y to 6Y	2, 4, 6, 8, 10, 12	output
V_{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

6. Limiting values

Table 2. Limiting values

In accordance with the Absolute Maximum Rating System .

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		–0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+125	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C			
		DIP-14 [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] DIP-14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

7. Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C

8. Static characteristics

Table 4. Static characteristics
V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4	-	4	-	4	-	4	-	V
			10 V	8	-	8	-	8	-	8	-	V
			15 V	12.5	-	12.5	-	12.5	-	12.5	-	V
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	1	-	1	-	1	-	1	V
			10 V	-	2	-	2	-	2	-	2	V
			15 V	-	2.5	-	2.5	-	2.5	-	2.5	V
V_{OH}	HIGH-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	–1.7	-	–1.4	-	–1.1	-	–1.1	mA
		V_O = 4.6 V	5 V	-	–0.64	-	–0.5	-	–0.36	-	–0.36	mA
		V_O = 9.5 V	10 V	-	–1.6	-	–1.3	-	–0.9	-	–0.9	mA
		V_O = 13.5 V	15 V	-	–4.2	-	–3.4	-	–2.4	-	–2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{DD}	supply current	all valid input combinations; I_O = 0 A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C_I	input capacitance	digital inputs		-	-	-	7.5	-	-	-	-	pF

9. Dynamic characteristics

Table 5. Dynamic characteristics

T_{amb} = 25 °C; for waveforms see Figure 4; for test circuit see Figure 5.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nA to nY;	5 V	18 ns + (0.55 ns/pF)C_L	-	45	90	ns
			10 V	9 ns + (0.23 ns/pF)C_L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C_L	-	15	25	ns
t_{PLH}	LOW to HIGH propagation delay	nA to nY	5 V	13 ns + (0.55 ns/pF)C_L	-	40	80	ns
			10 V	9 ns + (0.23 ns/pF)C_L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C_L	-	15	30	ns
t_{THL}	HIGH to LOW output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{TLH}	LOW to HIGH output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns

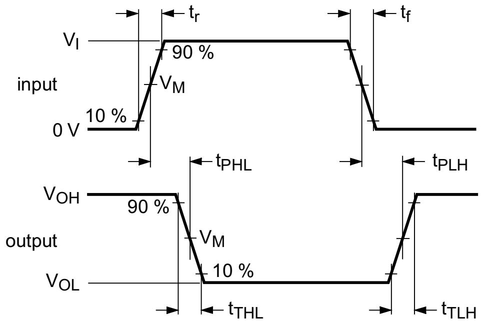
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 6. Dynamic power dissipation

V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_i = input frequency in MHz;
		10 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_o = output frequency in MHz;
		15 V	$P_D = 22000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	C_L = output load capacitance in pF;
				$\Sigma(f_o \times C_L)$ = sum of the outputs;
				V_{DD} = supply voltage in V.

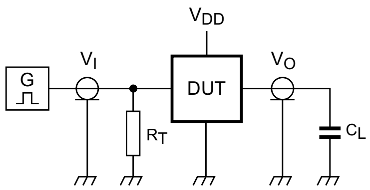
10. Waveforms



Measurement points: $V_M = 0.5V_{DD}$.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay and transition times



Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator;

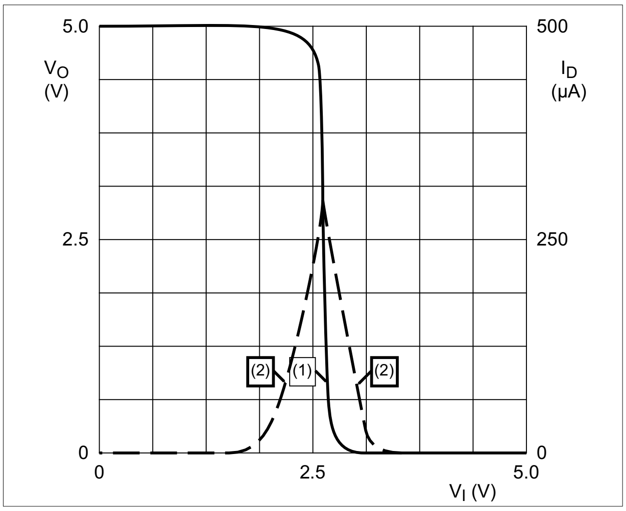
For test data refer to Table 7.

Fig 5. Test circuit for measuring switching times

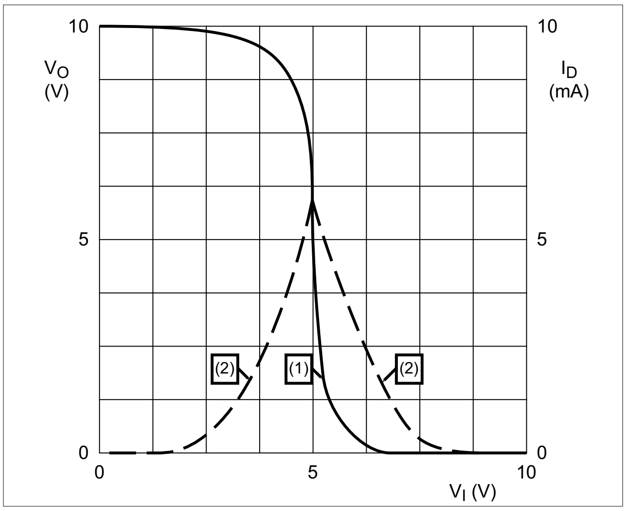
Table 7. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

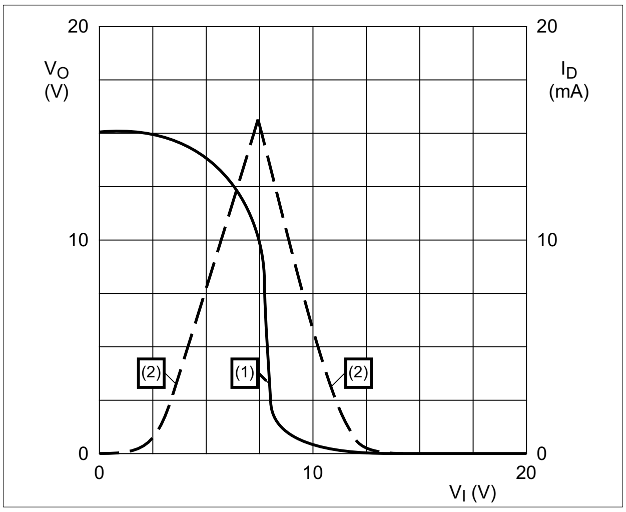
10.1 Transfer characteristics



a. V_{DD} = 5 V; I_O = 0 A



b. V_{DD} = 10 V; I_O = 0 A



c. V_{DD} = 15 V; I_O = 0 A

(1) V_O = output voltage.

(2) I_D = drain current.

Fig 6. Typical transfer characteristics

11. Application information

Some examples of applications for the XD4069.

Figure 7 shows an astable relaxation oscillator using two HEF4069UB inverters and 2 BAW62 diodes. The oscillation frequency is mainly determined by R1 × C1, provided R1 << R2 and R2 × C2 << R1 × C1.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance.

The period T_p is given by $T_p = T_1 + T_2$,

where:

$$T_1 = R1C1In\frac{V_{DD} + V_{ST}}{V_{ST}}$$

$$T_2 = R1C1In\frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}}$$

V_{ST} = the signal threshold level of the inverter.

The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.

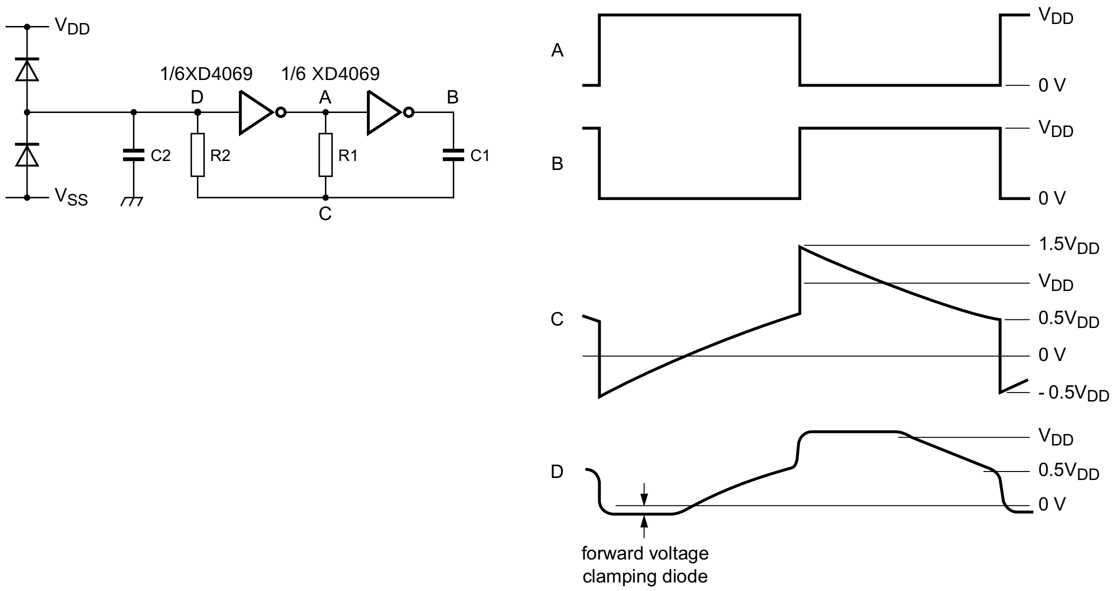
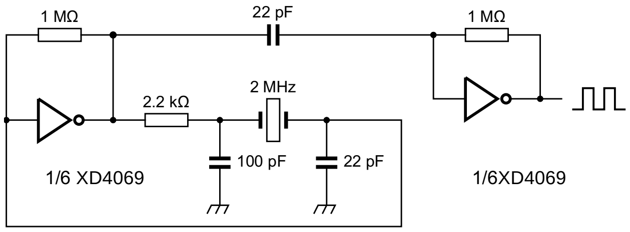


Fig 7. Astable relaxation oscillator

Figure 8 shows a crystal oscillator for frequencies up to 10 MHz using two HEF4069UB inverters. The second inverter amplifies the oscillator output voltage to a level sufficient to drive other Local Oxidation CMOS (LOCMOS) circuits.



The output inverter is used to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig 8. Crystal oscillator

Figure 9 and Figure 10 show voltage gain and supply current. Figure 11 shows the test set-up and an example of an analog amplifier using one XD4069.

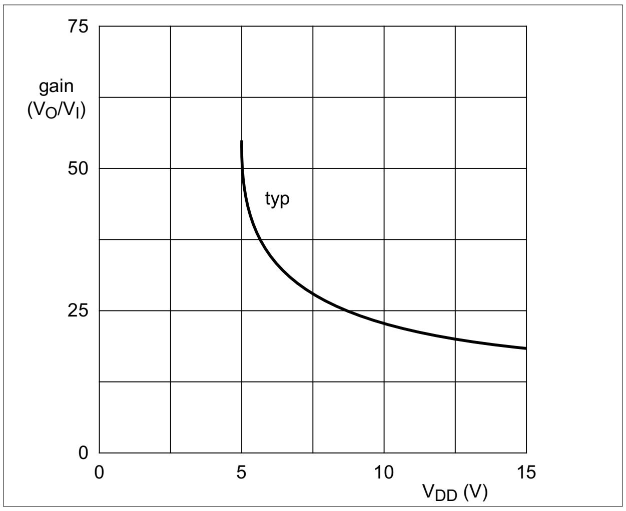


Fig 9. Typical voltage gain as a function of supply voltage

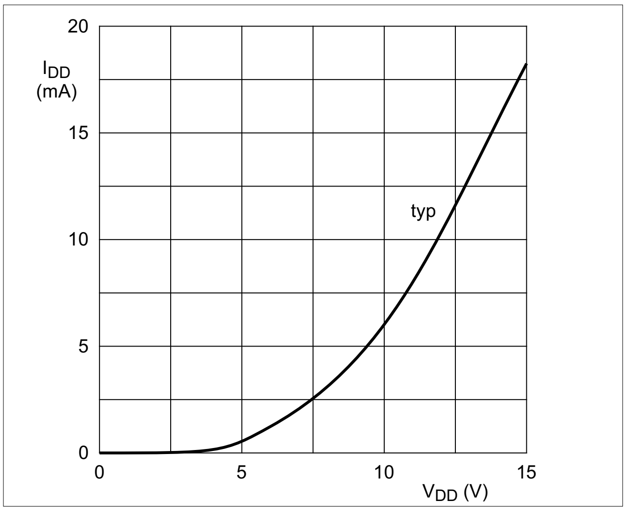


Fig 10. Typical supply current as a function of supply voltage

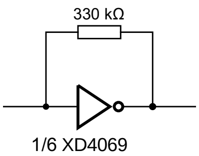
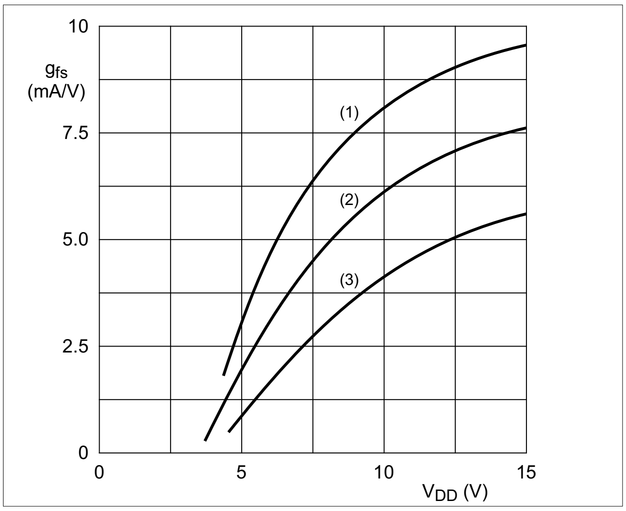


Fig 11. Test set-up

Figure 12 shows typical forward transconductance and Figure 13 shows the test set-up.

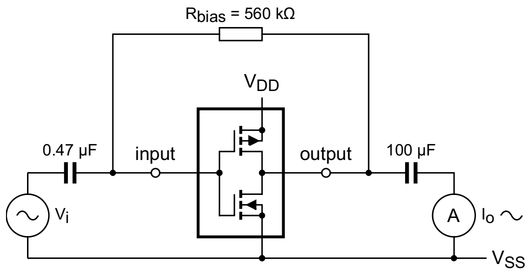


(1) Average +2σ; where: 'σ' is the standard deviation.

(2) Average.

(3) Average −2σ; where: 'σ' is the standard deviation.

Fig 12. Typical forward transconductance as a function of supply voltage at T_{amb} = 25 °C

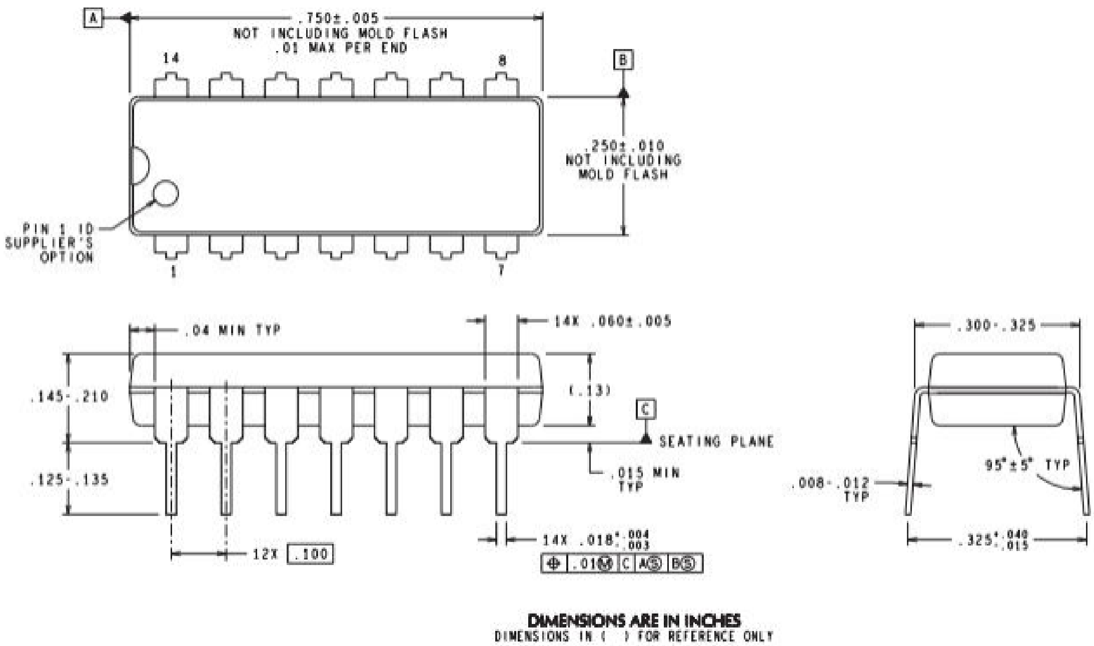


$$g_{fs} = \frac{dI_o}{dV_i}$$ at V_O is constant.

f_i = 1 kHz

Fig 13. Test set-up

DIP14



以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA