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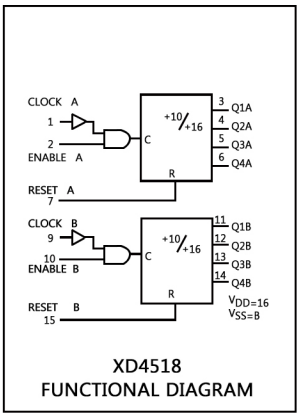
XD4518 DIP-16

High-Voltage Types(20-Volt Rating)
XD4518 Dual BCD UP-Counter

■ XD4518 Dual BCD Up-Counter nous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementingon either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive*going transition of the CLOCK. The counters are cleared by high levels on their RESET lines. The counter can be cascaded in the ripplemode by connecting Q4 to the enable input

Features:

- Medium speed operation- 6-MHz typical clock frequency at 10 V
- Positive- or negative-edge teiggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 20 V
- Maximum input current of 1μA at 18 V over full package-temperature range: 100 nA at 18V and 25°C
- Noise margin(over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10V; 2.5 V at V_{DD}= 15V
- 5-V,10-V,and 15-V perametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B,"Standard SPecifications fpr Description of 'b' Series CMOS Devices"



XD4518
FUNCTIONAL DIAGRAM

Applications:

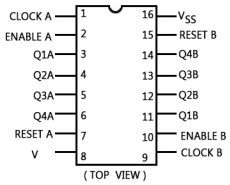
- Multistage synchronous counting
- Multistage ripple counting
- frequency dividers

MAXIMUM RATINGS, Absolute- Maximum Values:
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to Vss Terminal) . . . . . -0.5V to +20V
INPUTVOLTAGE RANGE, ALL INPUTS . . . . . -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
ForT_A = -55°C to +100°C 500mW
ForT_A = +100°C to +125°C . . . . . DerateLinearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FORT_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) . . . . . -55°C to +125°C
STORAGE TEMPERATURE RANGE (Tstg) . . . . . -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16±1/32 inch (1.59±0.79mm) from case for 10s max . . . . . +265°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐¯	1	0	Increment Counter
0	¯_	0	Increment Counter
¯_	X	0	No Change
X	⌐¯	0	No Change
⌐¯	0	0	No Change
1	¯_	0	No Change
X	X	0	Q1 thru Q4 = 0

X = Don't Care 1 = High State 0 = Low State



XD4518
TERMINAL ASSIGNMENT

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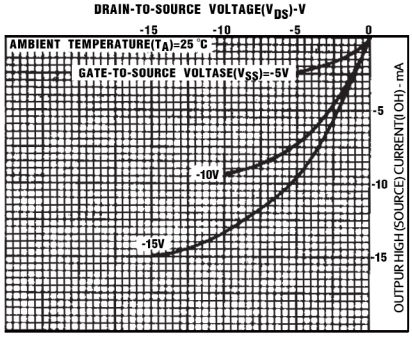
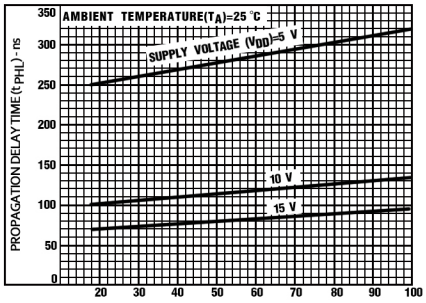
STATIC ELECTRLCAL CHARACTERISTICS

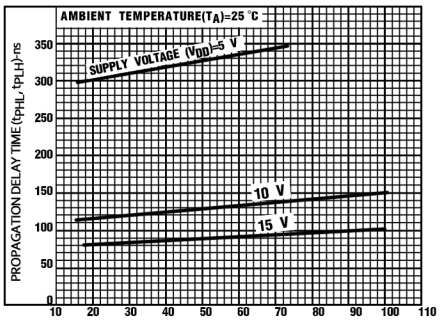
CHRACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES(°C)							UNITS
								+25			
	VO (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min	Typ	Max	
Quiescent Device Current I_{DD} Max.	–	0, 5	5	5	5	150	150	–	0. 04	5	μA
	–	0, 10	10	10	10	300	300	–	0. 04	10	
	–	0, 15	15	20	20	600	600	–	0. 04	20	
	–	0, 20	20	100	100	3000	3000	–	0. 08	100	
Qutput Low (Sink)Current I_{OL} Min.	0. 4	0, 5	5	0. 64	0. 61	0. 42	0. 36	0. 51	1	–	mA
	0. 5	0, 10	10	1. 6	1. 5	1. 1	0. 9	1. 3	2. 6	–	
	1. 5	0, 15	15	4. 2	4	2. 8	2. 4	3. 4	6. 8	–	
Qutput High (Source) Current, I_{OH} Min.	4. 6	0, 5	5	−0. 64	−0. 61	−0. 42	−0. 36	−0. 51	−1	–	
	2. 5	0, 5	5	−2	−1. 8	−1. 3	−1. 15	−1. 6	−3. 2	–	
	9. 5	0, 10	10	−1. 6	−1. 5	−1. 1	−0. 9	−1. 3	−2. 6	–	
	13. 5	0, 15	15	−4. 2	−4	−2. 8	−2. 4	−3. 4	−6. 8	–	
Output Voltage: Low-Level, V_{OL}Max.	–	0, 5	5	0. 05				–	0	0. 05	V
	–	0, 10	10	0. 05				–	0	0. 02	
	–	0, 15	15	0. 05				–	0	0. 02	
Output Voltage: High-Level, V_{OH}Min.	–	0, 5	5	4. 95				4. 95	5	–	
	–	0, 10	10	9. 95				9. 95	10	–	
	–	0, 15	15	14. 95				14. 95	15	–	
Lnput Low Voltage, V_{IL} Max.	0. 5, 4. 5	–	5	1. 5				–	–	1. 5	V
	1, 9	–	10	3				–	–	3	
	1. 5, 3. 5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0. 5, 4. 5	–	5	3. 5				3. 5	–	–	
	1, 9	–	10	7				7	–	–	
	1. 5, 13. 5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0, 18	18	±0 1	±0 1	±1	±1	–	$±10^{-5}$	±0 1	μA



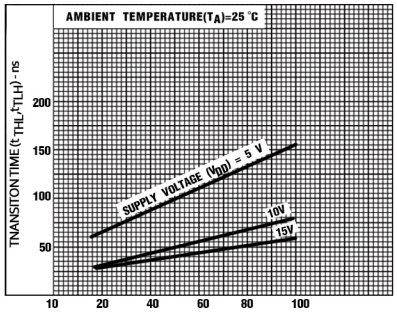
Minimum output high (source) current characterisitics.



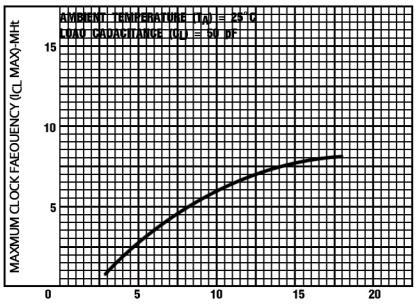
Typical propagation delay vs. load capacitance,clock or enable to output.



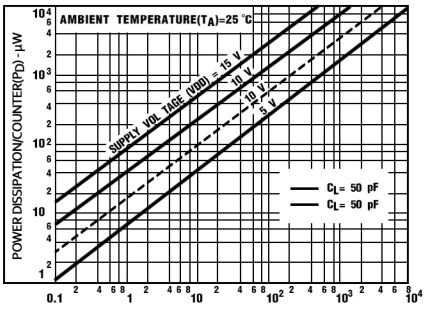
Typical propagation delay time vs. load capacitance,reset to output.



Typical transition time vs. load capacitance.



Typical maximum-clock-frequency vs. supply voltage.



Typical power dissipation characteristics.

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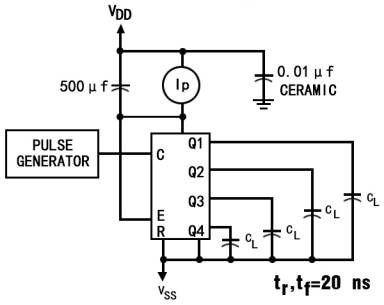
RECOMMENDED OPERATING CONDITIONS at TA = 25 °C,Except as Noted.
For maximum reliability,nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LINITS		UNITS
		Min	Max	
Supply-Voltage Range (For TA = Full Pack age Temperature Range)		3	18	V
Enable pulse Width ,tW 。	5	400	–	ns
	10	200	–	
	15	140	–	
Clock Pulse Width,tW	5	200	–	ns
	10	100	–	
	15	70	–	
Clock Input Frequency,fCL	5	dc	1.5	MHz
	10		3	
	15		4	
Clock Rise or Fall Time,t_rCL or t_fCL:	5	–	15	μs
	10		5	
	15		5	
Reset Pulse Width,tW	5	250	–	ns
	10	110		
	15	80		

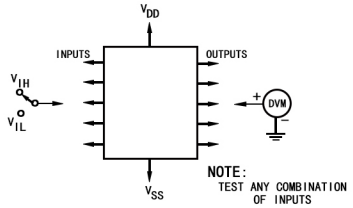
DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25 °C:
Input t_r,t_f=20 ns, C_L =50 pF, R_L =200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} V	Min	Typ	Max	
Propagation Delay Time, t_{PHL},t_{PLH}: Clock or Enable to Qutput		5	–	280	560	ns
		10		115	230	
		15		80	160	
Reset to Qutput		5	–	330	650	
		10		130	225	
		15		90	170	
Transition time,t_{THL} t_{TLH}		5	–	100	200	ns
		10		50	100	
		15		40	80	
Maximum Clock Input Frequency,fCL		5	1.5	3	–	MHz
		10	3	6		
		15	4	8		
Maximum Clock Pulse Width,tW		5		100	200	ns
		10		50	100	
		15		35	80	
Clock Rise or Fall Time t_r or t_f:		5	–	–	15	μs
		10, 15			5	
Minimum Reset Pulse Widtjh,tW		5	–	125	250	ns
		10		55	110	
		15		40	80	
Minimum Enable Pulse Widtjh,tW		5	–	200	400	ns
		10		100	200	
		15		70	140	
Input Capacitance,C_{IN}	Any Input			5	7.5	pF

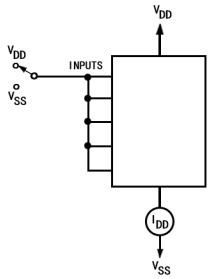
TEST CIRCUITS



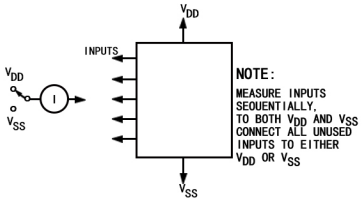
Dynamic power dissipartion



Input voltage.



Quiescent device current test circuit.



Input leakage-current test circuit

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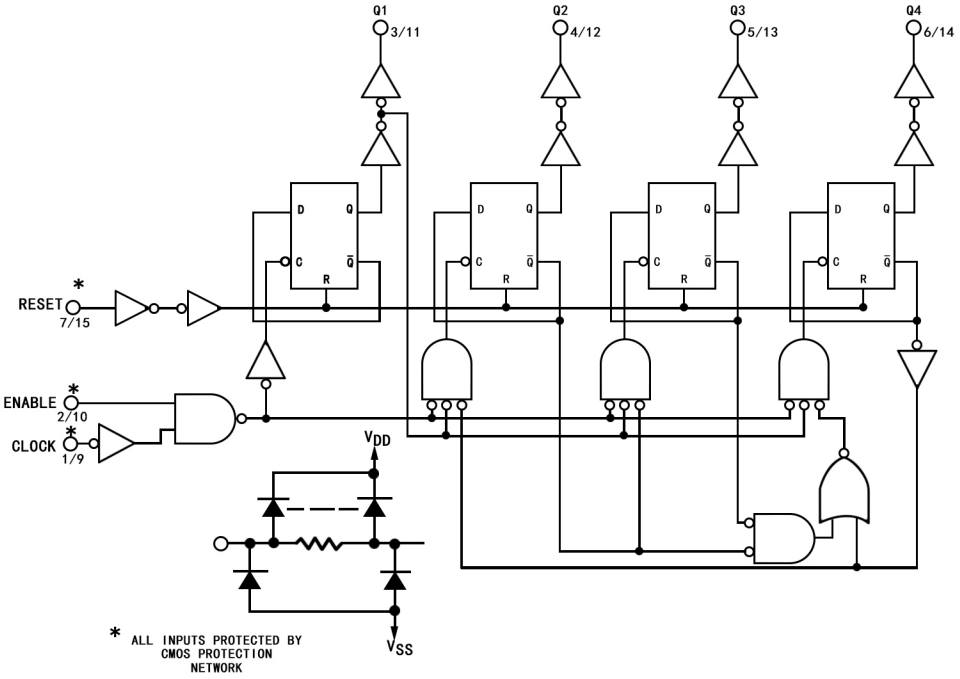
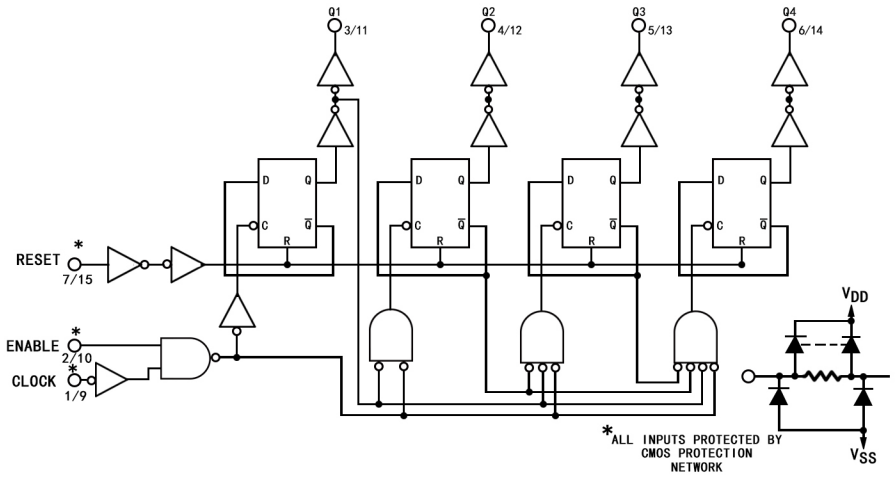
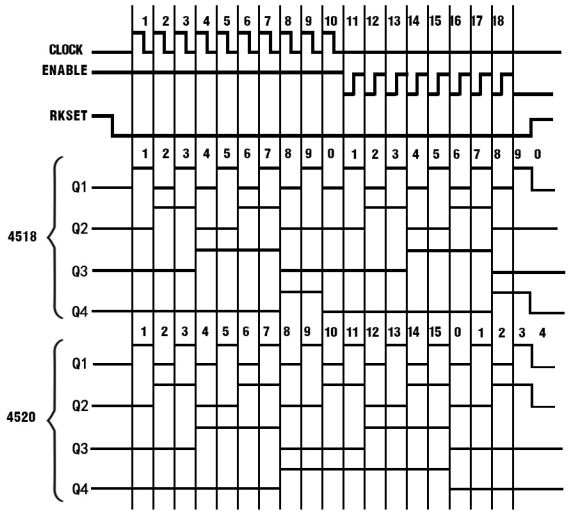


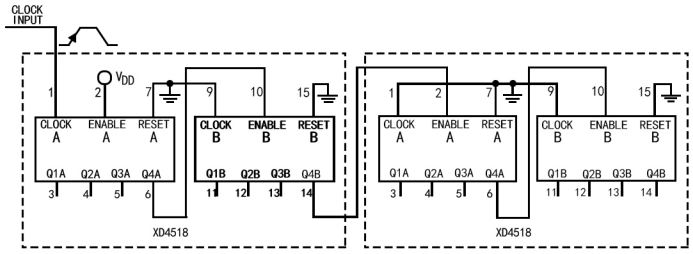
Decade counter (XD4518) logic diagram for one of two identical counters.



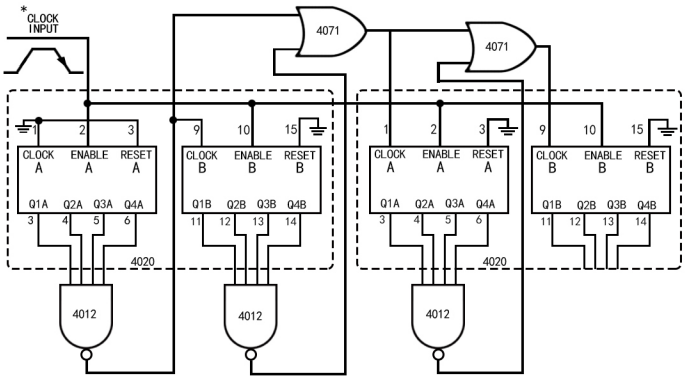
Binary counter (XD4518) logic diagram for one of two identical counters.



Timing diagrams for XD4518.



Ripple cascading of four counters with positive edge teiggering.



* NOTE:
FOR SYNCHRONUS CCASCADING. THE CLOCK TRANSITION TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE SUN OF THE FIXED PROPAGATION DELAY AT 15pF AND THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE FOR THE ESTIMATED CAPACITATIVE LOAD.

Synchronous cascading of four binary counters with negative edge teiggering.

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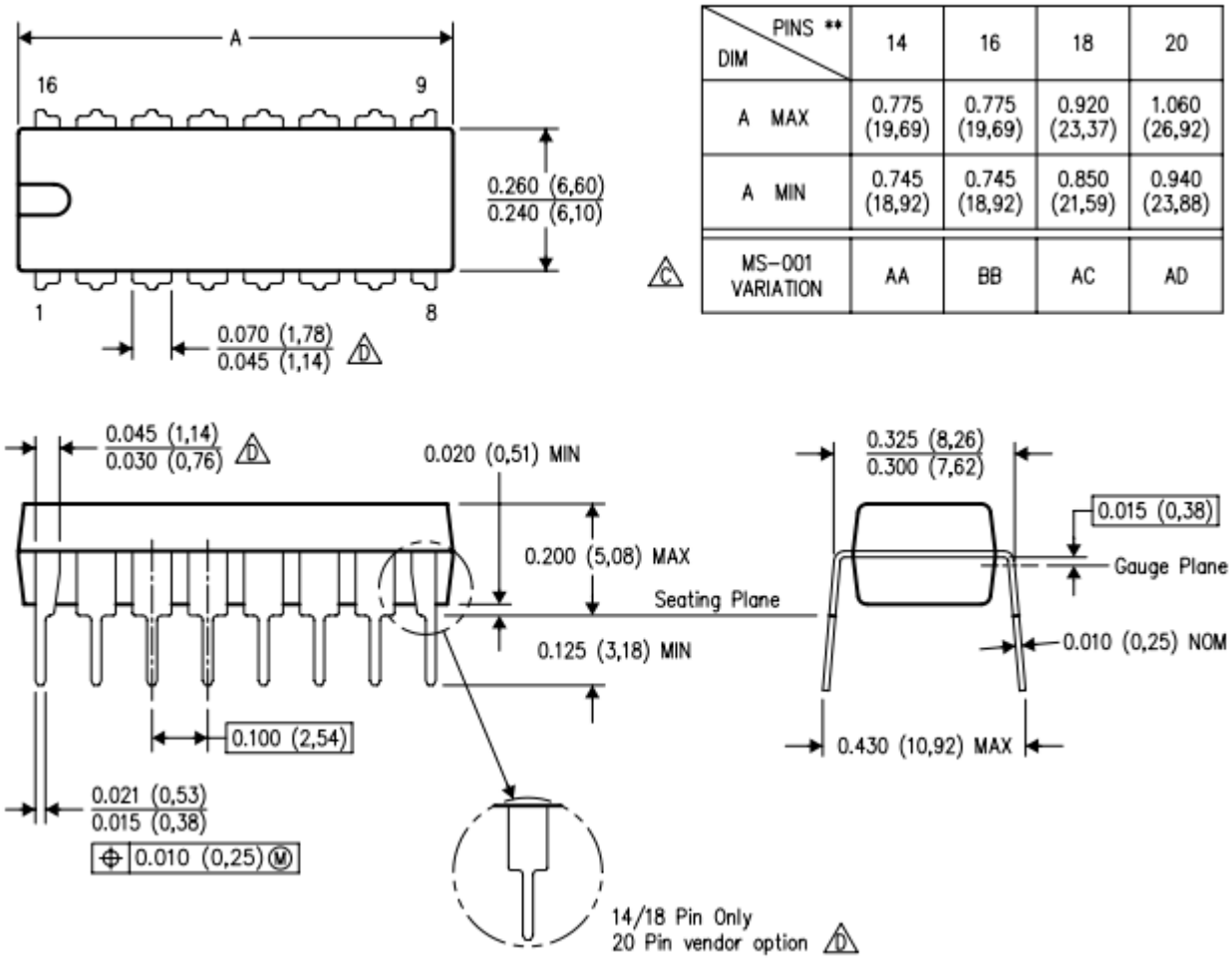
DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA

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