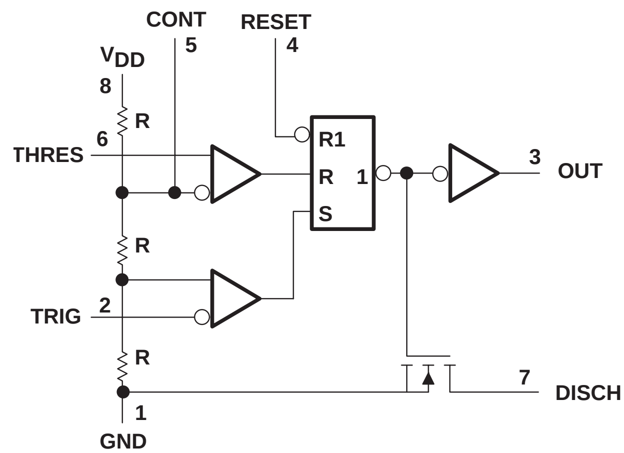
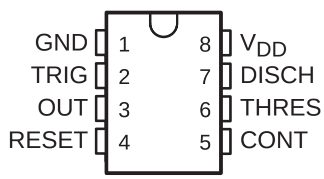
- **Very Low Power Consumption**
  1 mW Typ at V_{DD} = 5 V
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 1 V to 15 V**

functional block diagram



RESET can override TRIG, which can override THRES.



description

The XDXL551 is a monolithic timing circuit fabricated using LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Compared to the XL555 timer, this device uses smaller timing capacitors because of its high input impedance. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltage.

Like the XL555, the XDXL551 has a trigger level equal to approximately one-third of the supply voltage and athreshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use ofthe control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop isset and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above thethreshold level, the flip-flop is reset and the output is low. The reset input (RESET) can override all other inputsand can be used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low.Whenever the output is low, a low-impedance path is provided between DISCH and GND. All unused inputsshould be tied to an appropriate logic level to prevent false triggering.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the XDXL551 exhibits greatlyreduced supply-current spikes during output transitions. This minimizes the need for the large decouplingcapacitors required by the XL555.

The XDXL551C is characterized for operation from 0 °C to 70°C.

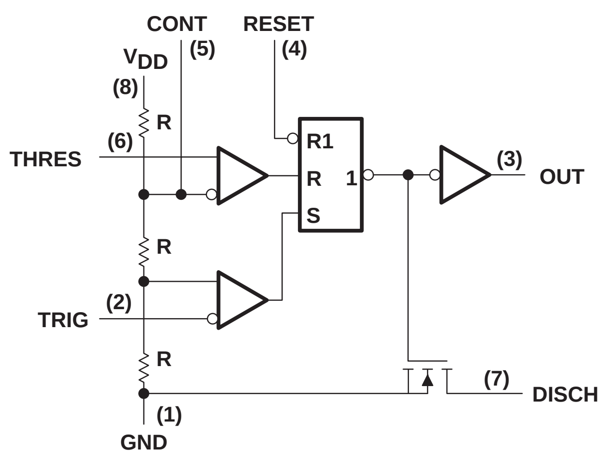
FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

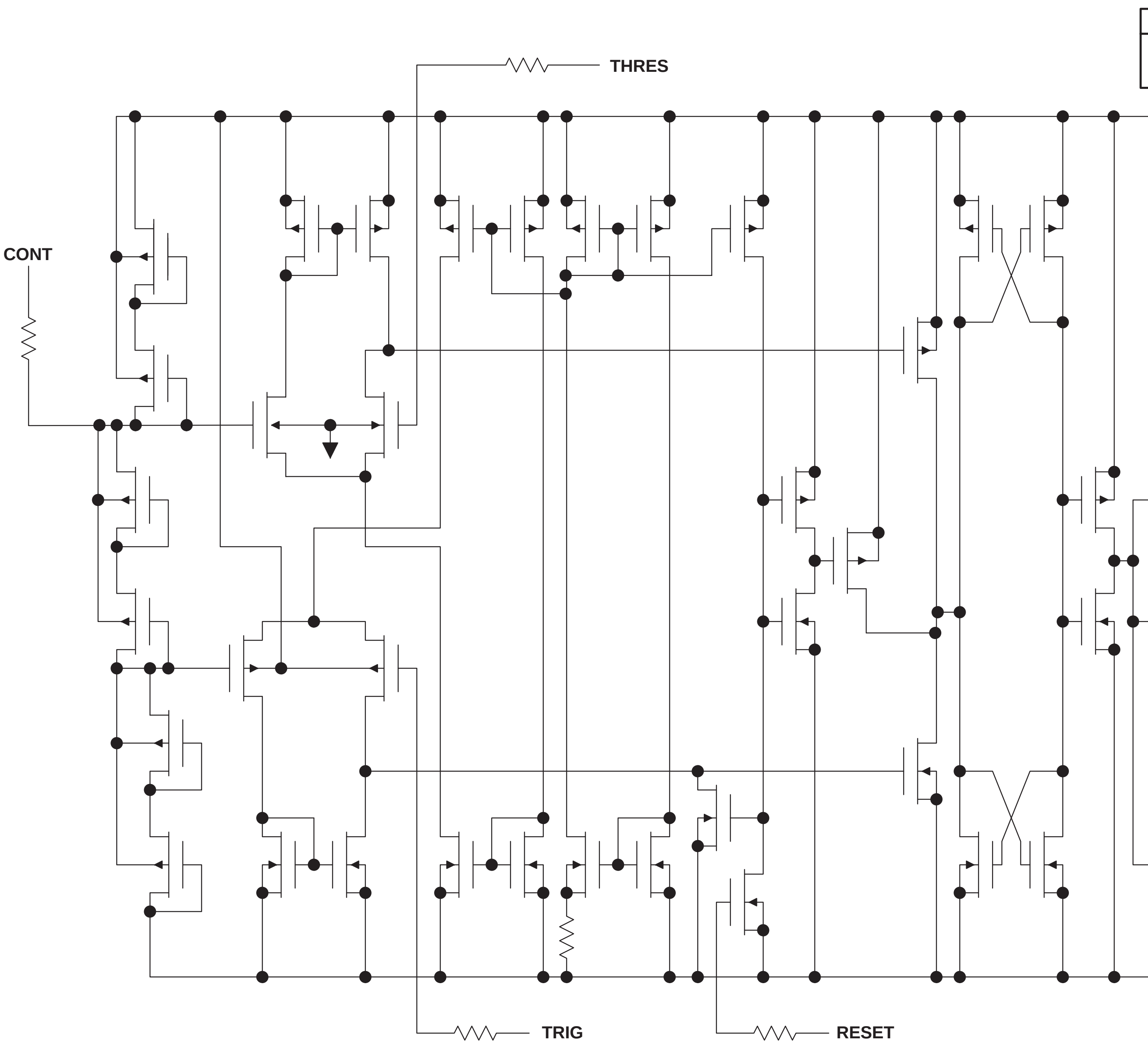
XL551 chip information

This chip, when properly assembled, displays characteristics similar to the XL551. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



RESET can override TRIG, which can override THRES.

equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Input voltage range, V_I (any input) . . . . –0.3 to V_{DD}
Sink current, discharge or output . . . . 150 mA
Source current, output, I_O . . . . 15 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	15	V
Operating free-air temperature range, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	0.475	0.67	0.85	V
			Full range	0.45		0.875	
I_{IT}	Threshold current		25°C		10		pA
			70°C		75		
$V_{I(TRIG)}$	Trigger voltage		25°C	0.15	0.33	0.425	V
			Full range	0.1		0.45	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			70°C		75		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	0.7	1	V
			Full range	0.3		1	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			70°C		75		
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 100 µA	25°C		0.02	0.15	V
			Full range			0.2	
	Discharge switch off-stage voltage		25°C		0.1		nA
			70°C		0.5		
V_{OH}	High-level output voltage	I_{OH} = –10 µA	25°C	0.6	0.98		V
			Full range	0.6			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA	25°C		0.03	0.2	V
			Full range			0.25	
I_{DD}	Supply current	See Note 2	25°C		15	100	µA
			Full range			150	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	0.95	1.33	1.65	V
			Full range	0.85		1.75	
I_{IT}	Threshold current		25°C		10		pA
			70°C		75		
$V_{I(TRIG)}$	Trigger voltage		25°C	0.4	0.67	0.95	V
			Full range	0.3		1.05	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			70°C		75		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			70°C		75		
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
			Full range			0.25	
	Discharge switch off-stage voltage		25°C		0.1		nA
			70°C		0.5		
V_{OH}	High-level output voltage	I_{OH} = –300 μA	25°C	1.5	1.9		V
			Full range	1.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
			Full range			0.35	
I_{DD}	Supply current	See Note 2	25°C		65	250	μA
			Full range			400	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A †	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	2.8	3.3	3.8	V
			Full range	2.7		3.9	
I_{IT}	Threshold current		25°C		10		pA
			70°C		75		
$V_{I(TRIG)}$	Trigger voltage		25°C	1.36	1.66	1.96	V
			Full range	1.26		2.06	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			70°C		75		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			70°C		75		
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
			Full range			0.6	
	Discharge switch off-stage voltage		25°C		0.1		nA
			70°C		0.5		
V_{OH}	High-level output voltage	I_{OH} = –1 mA	25°C	4.1	4.8		V
			Full range	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
			Full range			0.5	
		I_{OL} = 5 mA	25°C		0.13	0.3	
			Full range			0.4	
		I_{OL} = 3.2 mA	25°C		0.08	0.3	
			Full range			0.35	
I_{DD}	Supply current	See Note 2	25°C		170	350	µA
			Full range			500	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	9.45		10.55	V
			Full range	9.35		10.65	
I_{IT}	Threshold current		25°C		10		pA
			70°C		75		
$V_{I(TRIG)}$	Trigger voltage		25°C	4.65	5	5.35	V
			Full range	4.55		5.45	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			70°C		75		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			70°C		75		
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
			Full range			1.8	
	Discharge switch off-stage voltage		25°C		0.1		nA
			70°C		0.5		
V_{OH}	High-level output voltage	I_{OH} = –10 mA	25°C	12.5	14.2		V
			Full range	12.5			
		I_{OH} = –5 mA	25°C	13.5	14.6		
			Full range	13.5			
		I_{OH} = –1 mA	25°C	14.2	14.9		
			Full range	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
			Full range			3.6	
		I_{OL} = 50 mA	25°C		0.63	1	
			Full range			1.3	
		I_{OL} = 10 mA	25°C		0.12	0.3	
			Full range			0.4	
I_{DD}	Supply current	See Note 2	25°C		360	600	μA
			Full range			800	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Initial error of timing interval‡	V_{DD} = 5 V to 15 V, C_T = 0.1 μF,	$R_A = R_B$ = 1 kΩ to 100 kΩ, See Note 3		1%	3%	
	Supply voltage sensitivity of timing interval				0.1	0.5	%/V
t_r	Rise time, output pulse	R_L = 10 MΩ,	C_L = 10 pF		20	75	ns
t_f	Fall time, output pulse				15	60	
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF	R_B = 200 Ω, See Note 3	1.2	1.8		MHz

‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 3.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		2.8	3.3	3.8	V
I_{IT}	Threshold current			10		pA
$V_{I(TRIG)}$	Trigger voltage		1.36	1.66	1.96	V
$I_{I(TRIG)}$	Trigger current			10		pA
$V_{I(RESET)}$	Reset voltage		0.4	1.1	1.5	V
$I_{I(RESET)}$	Reset current			10		pA
	Control voltage (open circuit) as a percentage of supply voltage			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA		0.14	0.5	V
	Discharge switch off-state current			0.1		nA
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	4.1	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.21	0.4	V
		I_{OL} = 5 mA		0.13	0.3	
		I_{OL} = 3.2 mA		0.08	0.3	
I_{DD}	Supply current	See Note 2		170	350	μA

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

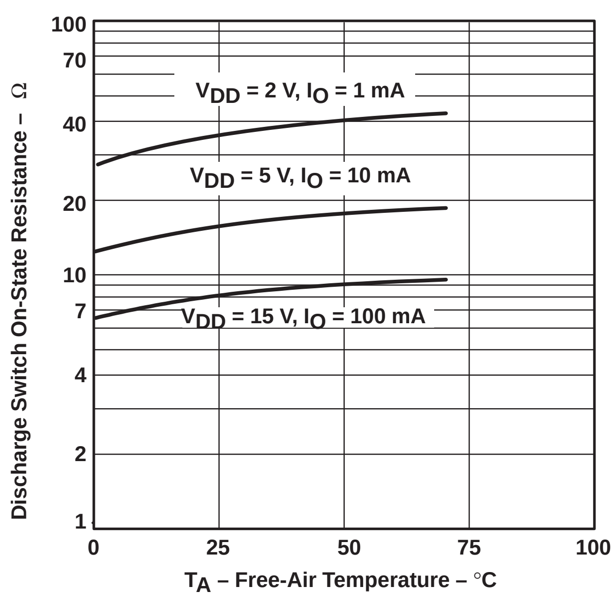
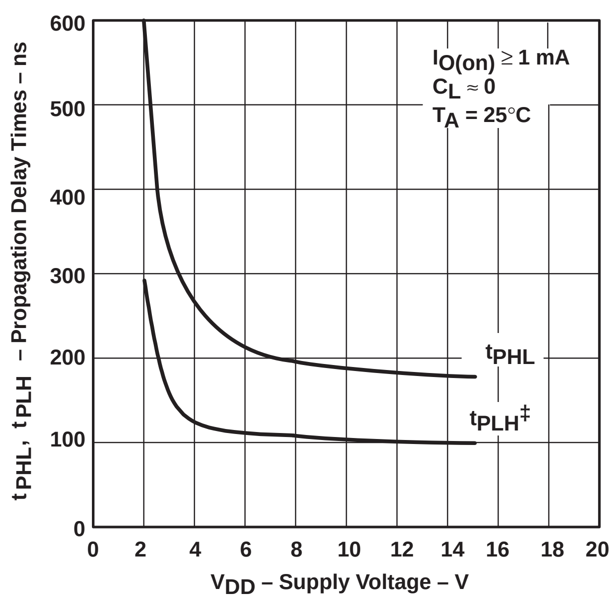


Figure 1

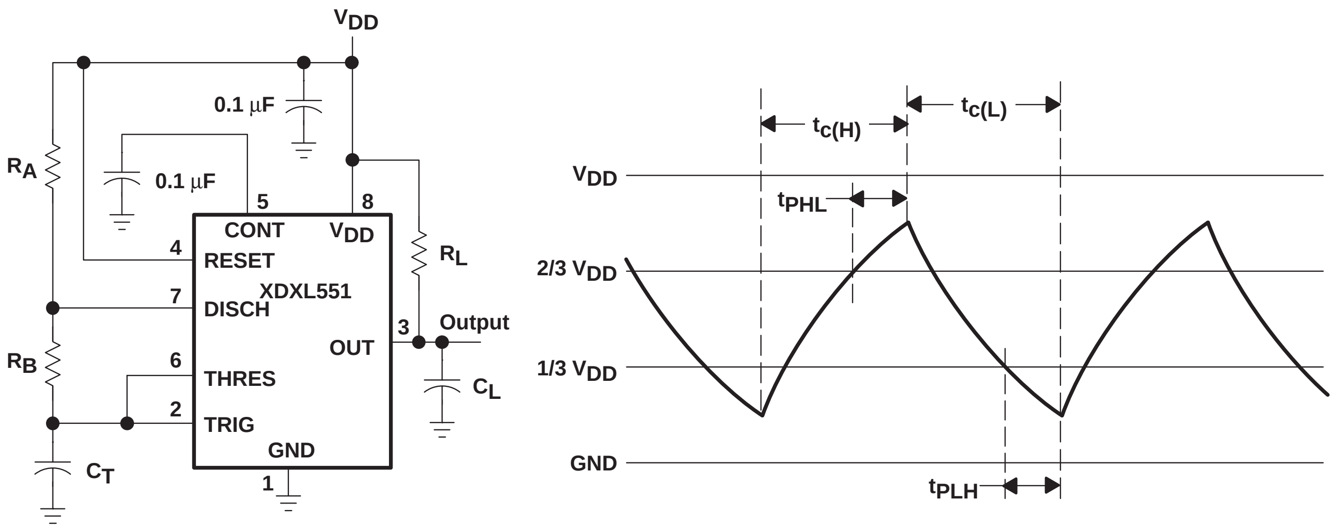
PROPAGATION DELAY TIMES (TO DISCHARGE OUTPUT FROM TRIGGER AND THRESHOLD SHORTED TOGETHER) vs SUPPLY VOLTAGE



‡ The effects of the load resistance on these values must be taken into account separately.

Figure 2

APPLICATION INFORMATION



CIRCUIT TRIGGER AND THRESHOLD VOLTAGE WAVEFORM

Figure 3. Astable Operation

Connecting TRIG to THRES, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the threshold voltage level (approximately 0.67 V_{DD}) and then discharges through R_B only to the value of the trigger voltage level (approximately 0.33 V_{DD}). The output is high during the charging cycle ($t_{c(H)}$) and low during the discharge cycle ($t_{c(L)}$). The duty cycle is controlled by the values of R_A, and R_B, and C_T, as shown in the equations below.

$$t_{c(H)} \approx C_T\,(R_A + R_B)\ \ln 2 \quad (\ln 2 = 0.693)$$

$$t_{c(L)} \approx C_T\,R_B\ \ln 2$$

$$\text{Period} = t_{c(H)} + t_{c(L)} \approx C_T\,(R_A + 2R_B)\ \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_{c(L)}}{t_{c(H)} + t_{c(L)}} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-µF capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay times from TRIG and THRES to DISCH. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low or r_{on} is very high.

APPLICATION INFORMATION

The equations below provide better agreement with measured values.

$$t_{c(H)} = C_T (R_A + R_B) \ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})}\right)\right] + t_{PHL}$$

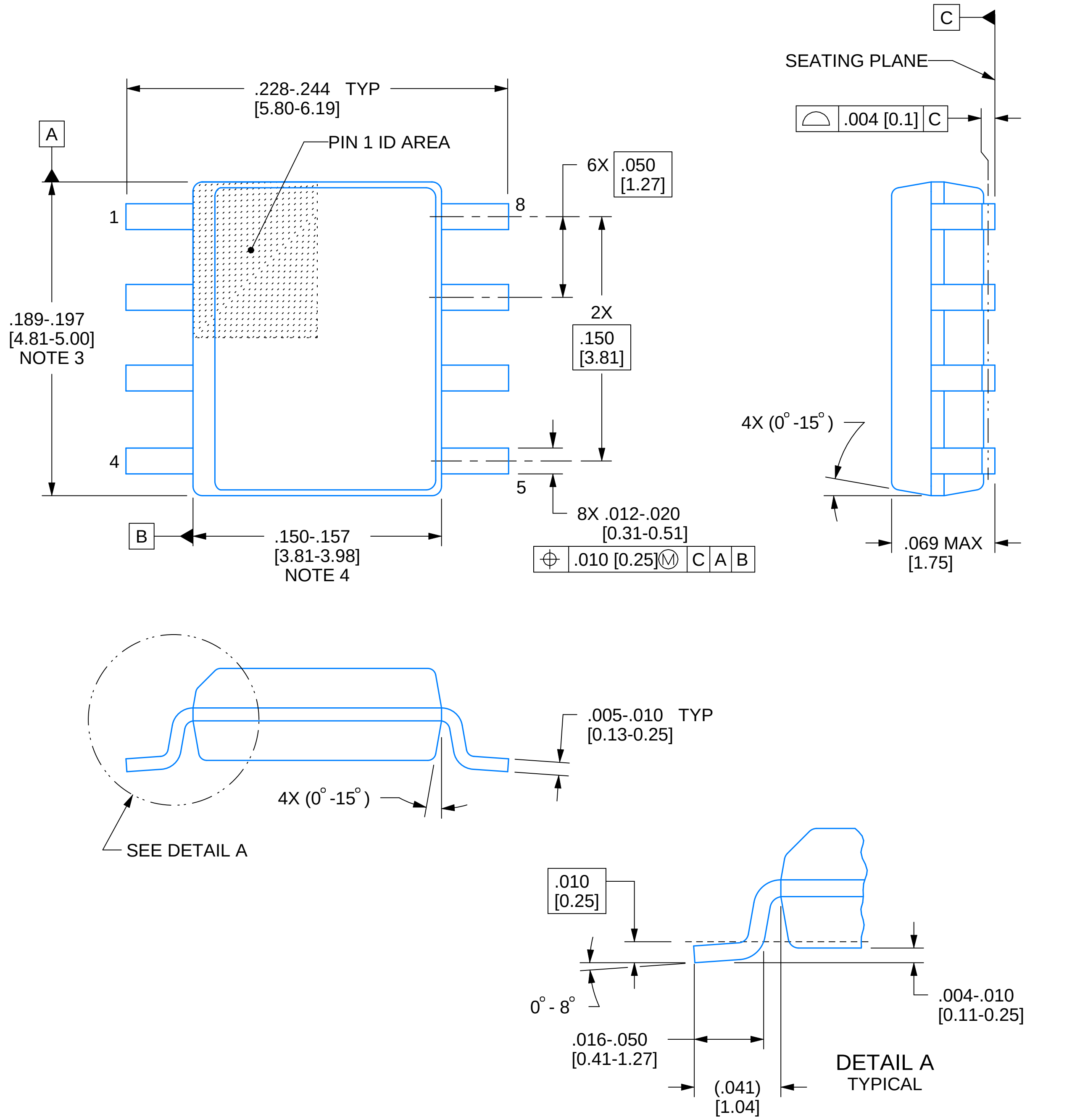
$$t_{c(L)} = C_T (R_B + r_{on}) \ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)}\right)\right] + t_{PLH}$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between In 2 at low frequencies and In 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}}$ require that $\frac{t_{c(H)}}{t_{c(L)}} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500-µA bias provides good results.

SMALL OUTLINE INTEGRATED CIRCUIT

SOP

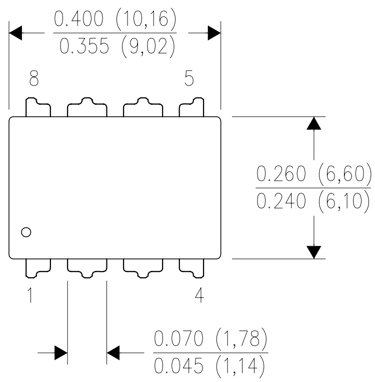


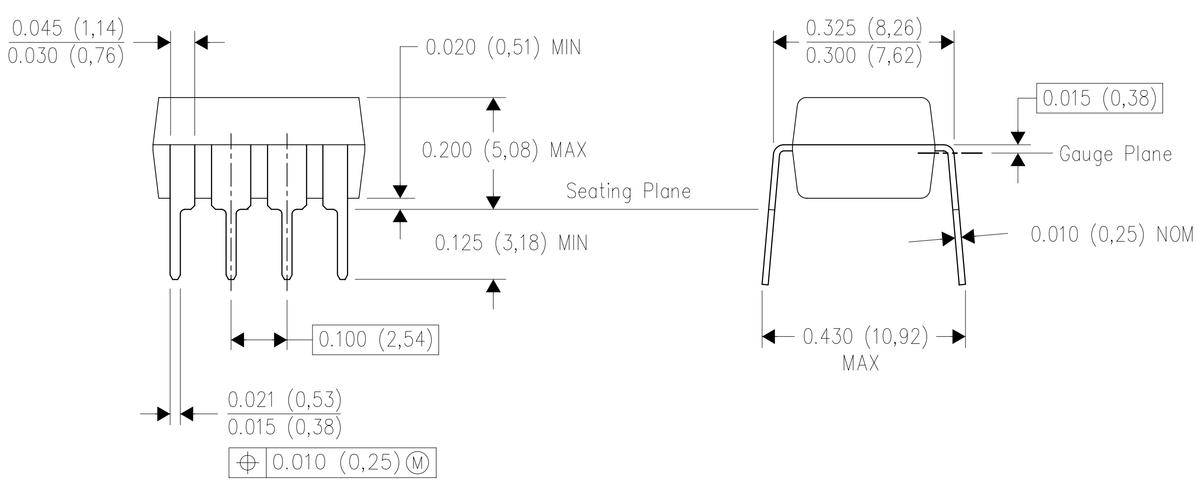
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

DIP





NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA