1 Features

- Wide Operating Voltage Range from 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly up to 15 LSTTL Loads
- Low Power Consumption: 80-µA Maximum I_{CC}
- Typical t_{pd} = 21 ns
- ±6-mA Output Drive at 5 V
- Low Input Current: 1 µA (Maximum)
- Bus-Structured Pinout

2 Applications

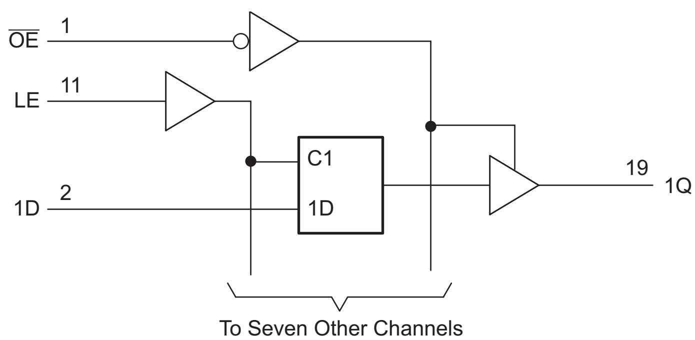
- Buffer Registers
- Bidirectional Bus Drivers
- Working Registers

3 Description

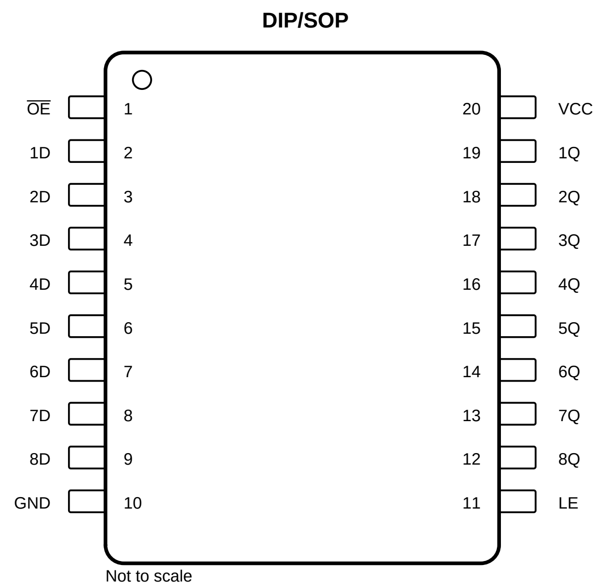
The 74HC573 devices are octal transparent D-type latches that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

4 Logic Diagram (Positive Logic)



5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output enable
2	1D	I	1D input
3	2D	I	2D input
4	3D	I	3D input
5	4D	I	4D input
6	5D	I	5D input
7	6D	I	6D input
8	7D	I	7D input
9	8D	I	8D input
10	GND	—	Ground
11	LE	I	Latch enable input
12	8Q	O	8Q output
13	7Q	O	7Q output
14	6Q	O	6Q output
15	5Q	O	5Q output
16	4Q	O	4Q output
17	3Q	O	3Q output
18	2Q	O	2Q output
19	1Q	O	1Q output
20	V_{CC}	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current[2]	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	74HC573	–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		74HC573 DW (SOIC) 20 PINS	74HC573 N (PDIP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.3	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.8	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.2	30	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18	22.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.7	29.9	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = –20\ \mu A$	$V_{CC} = 2\ V$	1.9	1.998		V
			$V_{CC} = 4.5\ V$	4.4	4.499		
			$V_{CC} = 6\ V$	5.9	5.999		
		$I_{OH} = –6\ mA$, $V_{CC} = 4.5\ V$	$T_A = 25°C$	3.98	4.3		
			74HC573	3.84			
		$I_{OH} = –7.8\ mA$, $V_{CC} = 6\ V$	$T_A = 25°C$	5.48	5.8		
			74HC573	5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	$V_{CC} = 2\ V$		0.002	0.1	V
			$V_{CC} = 4.5\ V$		0.001	0.1	
			$V_{CC} = 6\ V$		0.001	0.1	
		$I_{OL} = 6\ mA$, $V_{CC} = 4.5\ V$	$T_A = 25°C$		0.17	0.26	
			74HC573			0.33	
		$I_{OL} = 7.8\ mA$, $V_{CC} = 6\ V$	$T_A = 25°C$		0.15	0.26	
			74HC573			0.33	
I_I	$V_I = V_{CC}$ or 0, $V_{CC} = 6\ V$		$T_A = 25°C$		±0.1	±100	nA
			74HC573			±1000	
I_{OZ}	$V_O = V_{CC}$ or 0, $V_{CC} = 6\ V$		$T_A = 25°C$		±0.01	±0.5	µA
			74HC573			±5	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$, $V_{CC} = 6\ V$		$T_A = 25°C$			8	µA
			74HC573			80	
C_i	$V_{CC} = 2\ V$ to $6\ V$				3	10	pF
C_{pd} Power dissipation capacitance per latch	$T_A = 25°C$, no load				50		pF

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
t_w	Pulse duration, LE high	V_{CC} = 2 V	T_A = 25°C	80			ns
			74HC573	100			
		V_{CC} = 4.5 V	T_A = 25°C	16			
			74HC573	20			
		V_{CC} = 6 V	T_A = 25°C	14			
			74HC573	17			
t_{su}	Setup time, data before LE↓	V_{CC} = 2 V	T_A = 25°C	50			ns
			74HC573	63			
		V_{CC} = 4.5 V	T_A = 25°C	10			
			74HC573	13			
		V_{CC} = 6 V	T_A = 25°C	9			
			74HC573	11			
t_h	Hold time, data after LE↓	V_{CC} = 2 V	T_A = 25°C	20			ns
			74HC573	24			
		V_{CC} = 4.5 V		5			
		V_{CC} = 6 V		5			

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted; see Figure 2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	C_L = 50 pF, from D (input) to Q (output)	V_{CC} = 2 V	T_A = 25°C		77	175	ns
			74HC573			220	
		V_{CC} = 4.5 V	T_A = 25°C		26	35	
			74HC573			44	
		V_{CC} = 6 V	T_A = 25°C		23	30	
			74HC573			38	
	C_L = 50 pF, from LE (input) to any Q (output)	V_{CC} = 2 V	T_A = 25°C		87	175	
			74HC573			220	
		V_{CC} = 4.5 V	T_A = 25°C		27	35	
			74HC573			44	
		V_{CC} = 6 V	T_A = 25°C		23	30	
			74HC573			38	

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{en}	C_L = 50 pF, from $\overline{OE}$ (input) to any Q (output)	V_{CC} = 2 V	T_A = 25°C		68	150	ns
			74HC573			190	
		V_{CC} = 4.5 V	T_A = 25°C		24	30	
			74HC573			38	
		V_{CC} = 6 V	T_A = 25°C		21	26	
			74HC573			32	
t_{dis}	C_L = 50 pF, from $\overline{OE}$ (input) to any Q (output)	V_{CC} = 2 V	T_A = 25°C		47	150	ns
			74HC573			190	
		V_{CC} = 4.5 V	T_A = 25°C		23	30	
			74HC573			38	
		V_{CC} = 6 V	T_A = 25°C		21	26	
			74HC573			32	
t_t	C_L = 50 pF to any Q (output)	V_{CC} = 2 V	T_A = 25°C		28	60	ns
			74HC573			75	
		V_{CC} = 4.5 V	T_A = 25°C		8	12	
			74HC573			15	
		V_{CC} = 6 V	T_A = 25°C		6	10	
			74HC573			13	
t_{pd}	C_L = 150 pF, from D (input) to Q (output)	V_{CC} = 2 V	T_A = 25°C		95	200	ns
			74HC573			250	
		V_{CC} = 4.5 V	T_A = 25°C		33	40	
			74HC573			50	
		V_{CC} = 6 V	T_A = 25°C		21	34	
			74HC573			43	
	C_L = 150 pF, from LE (input) to any Q (output)	V_{CC} = 2 V	T_A = 25°C		103	225	
			74HC573			285	
		V_{CC} = 4.5 V	T_A = 25°C		33	45	
			74HC573			57	
		V_{CC} = 6 V	T_A = 25°C		29	40	
			74HC573			50	

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{en}	C_L = 150 pF, from $\overline{OE}$ (input) to any Q (output)	V_{CC} = 2 V	T_A = 25°C		85	200	ns
			74HC573			250	
		V_{CC} = 4.5 V	T_A = 25°C		29	40	
			74HC573			50	
		V_{CC} = 6 V	T_A = 25°C		26	34	
			74HC573			43	
t_t	C_L = 150 pF to any Q (output)	V_{CC} = 2 V	T_A = 25°C		60	210	ns
			74HC573			265	
		V_{CC} = 4.5 V	T_A = 25°C		17	42	
			74HC573			53	
		V_{CC} = 6 V	T_A = 25°C		14	36	
			74HC573			45	

6.8 Typical Characteristics

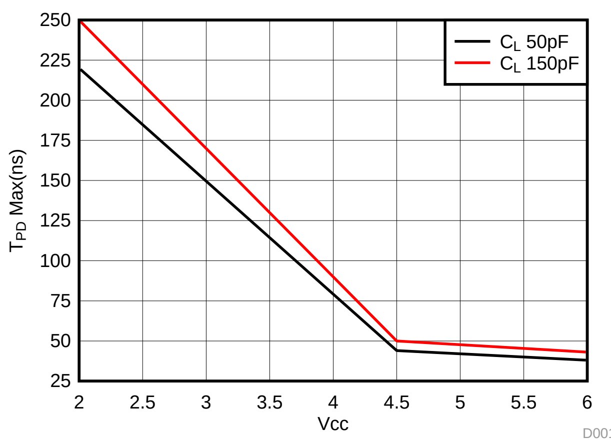
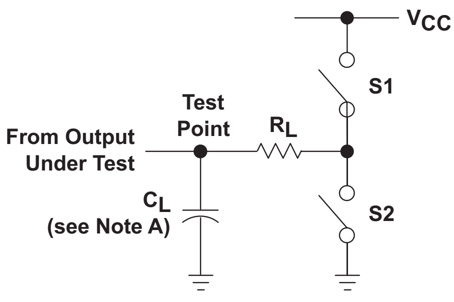


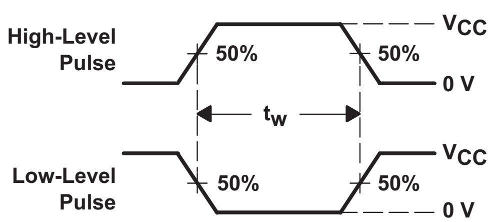
Figure 1. Maximum Propagation Delay Curves

7 Parameter Measurement Information

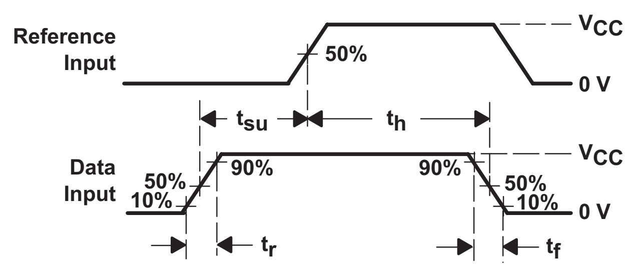


LOAD CIRCUIT

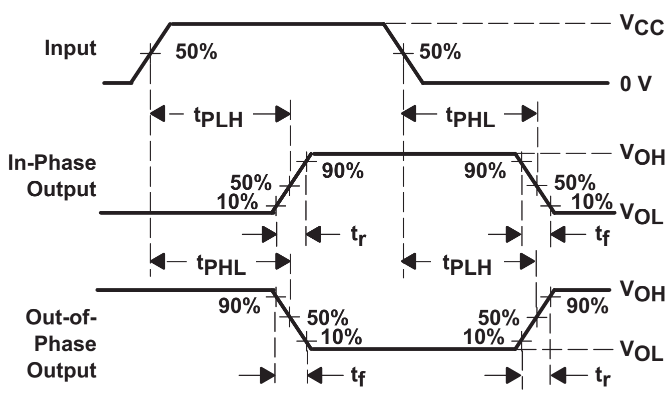
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



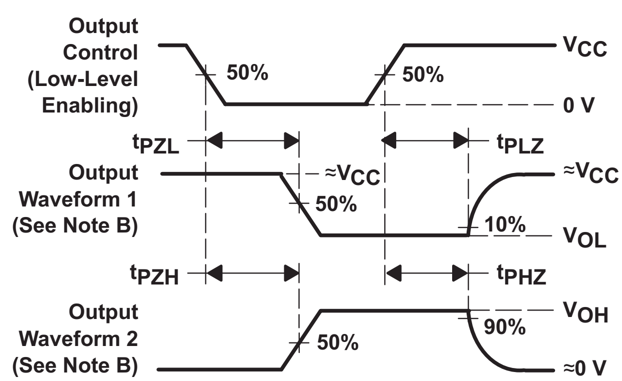
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The 74HC573 devices are octal transparent D-type latches that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

8.2 Functional Block Diagram

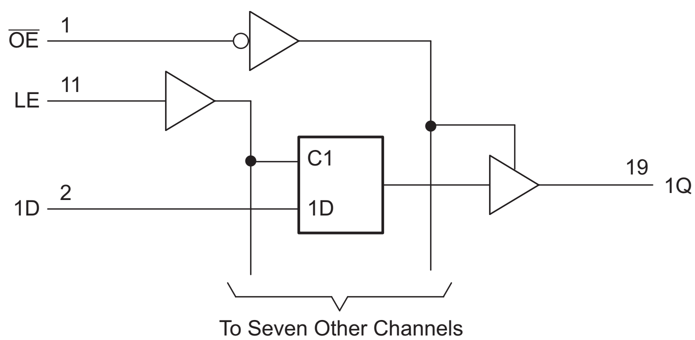


Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The 74HC573 is a high current 3-state output device which can drive bus lines directly or up to 15 LSTTL loads. It has low power consumption up to 80-µA maximum I_{CC}. The high speed CMOS family has typical propagation delay of 21 ns with ±6-mA output drive at 5 V. The input leakage current is a very low 1-µA (maximum).

8.4 Device Functional Modes

Table 1 lists the functional modes of the 74HC573

Table 1. Function Table (Each Latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Hi-Z