XD74LS06 DIP14
XL74LS06 SOP14

1 Features

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Factory Automation
- Building Automation
- Line Drivers
- Electronic Point of Sale
- Desktop or Notebook PCs

3 Description

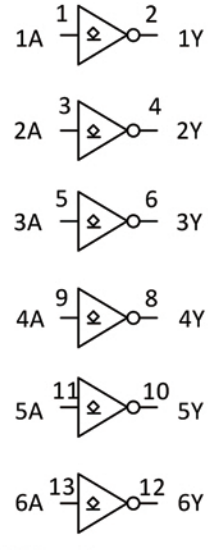
The XD74LS06 devices feature high-voltage, open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The XD74LS06 devices have a rated output voltage of 30 V.

4 Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
54LS06	CDIP (14)	19.50 mm × 6.92 mm
	LCCC (20)	8.89 mm × 8.89 mm
XL746S06	SOIC (14)	8.65 mm × 3.91 mm
XL74LS06-SS	SSOP (14)	5.30 mm × 6.20 mm
XD74LS06	PDIP (14)	19.30 mm × 6.35 mm
XD74LS06S	SOP (14)	5.30 mm × 10.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

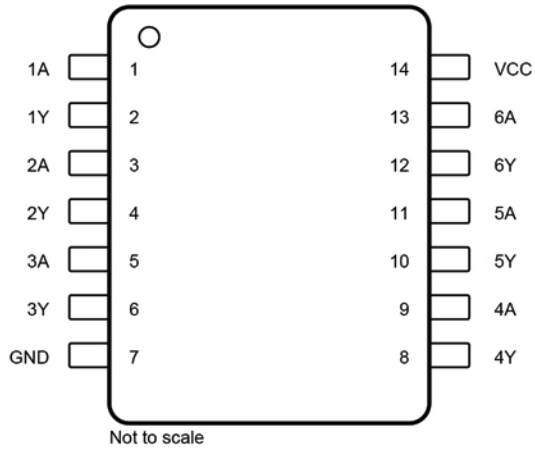
Logic Diagram (Positive Logic)



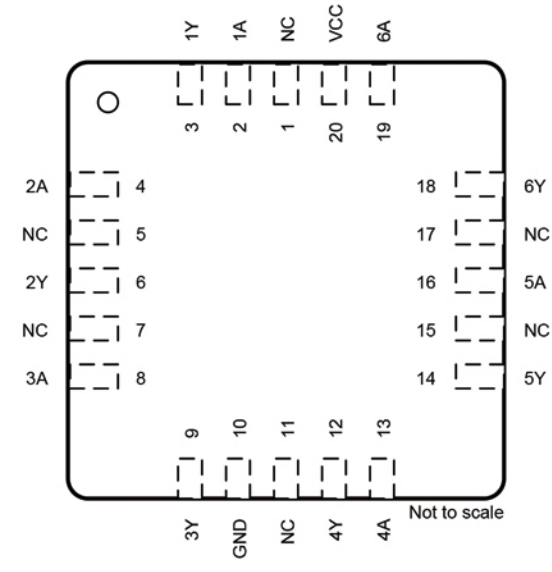
Pin numbers shown are for the D, DB, J, N, and NS packages.

5 Pin Configuration and Functions

D, DB, J, N, and NS Package
14-Pin SOIC, SSOP, CDIP, PDIP, and SOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, CDIP, PDIP, SOP	LCCC		
1A	1	2	I	1A Input
1Y	2	3	O	1Y Output
2A	3	4	I	2A Input
2Y	4	6	O	2Y Output
3A	5	8	I	3A Input
3Y	6	9	O	3Y Output
4A	9	13	I	4A Input
4Y	8	12	O	4Y Output
5A	11	16	I	5A Input
5Y	10	14	O	5Y Output
6A	13	19	I	6A Input
6Y	12	18	O	6Y Output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V_{CC}	14	20	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}		7	V
Input voltage, V_I(2)		7	V
Output voltage, V_O (XD74LS06)(2)(3)		30	V
Absolute maximum junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) This is the maximum voltage that must be applied to any output when it is in the off state.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Tested on N package

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage (XD74LS06)				30	V
I_{OL}	Low-level output current	XD74LS06			30	mA
		XL74LS06			40	
T_A	Operating free-air temperature	XD74LS06	–55		125	°C
		XL74LS06	0		70	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC[1]		XD74LS06				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.8	97.4	50.2	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44	49.8	37.5	40.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.3	44.5	30	41.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	16.5	22.3	12.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.1	44	29.9	41.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –12 mA				–1.5	V
I_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V, XD74LS06 XL74LS06				0.25	mA
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 16 mA		0.25	0.4	V
		I_{OL} = 30 mA			0.7	
		I_{OL} = 40 mA, SN74LS06			0.7	
I_I	V_{CC} = MAX, V_I = 7 V				1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				–0.2	mA
I_{CCH}	V_{CC}= MAX				18	mA
I_{CCL}	V_{CC}= MAX				60	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Recommended Operating Conditions*.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.6 Switching Characteristics

V_{CC} = 5 V and T_A = 25°C (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to Y (output), R_L= 110 Ω, C_L = 15 pF	7		15	ns
t_{PHL}	From A (input) to Y (output), R_L= 110 Ω, C_L = 15 pF	10		20	

6.7 Typical Characteristics

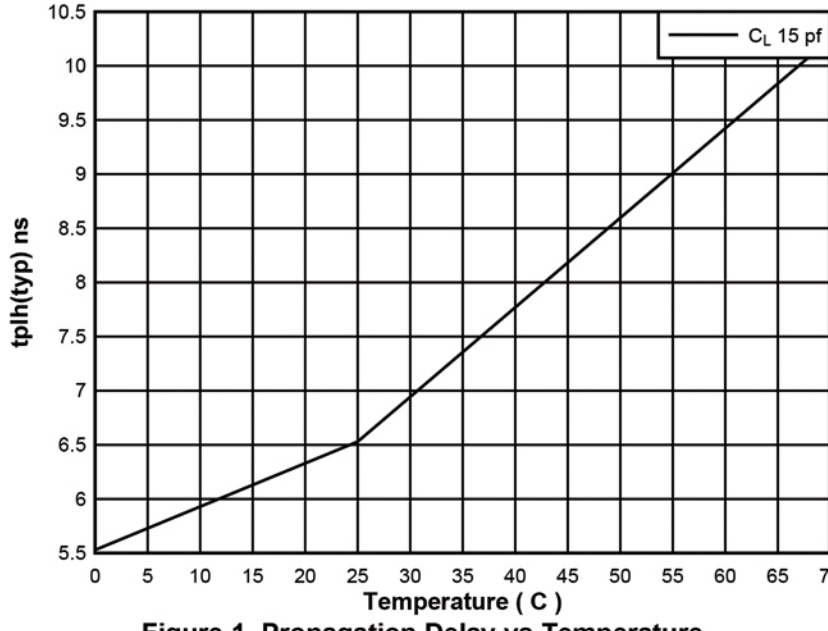
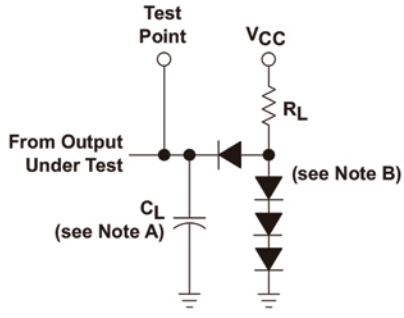
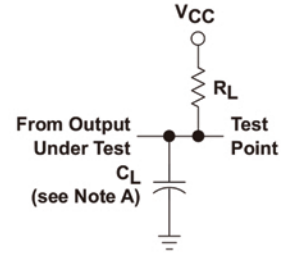


Figure 1. Propagation Delay vs Temperature

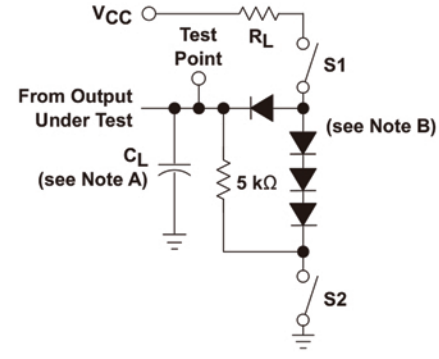
7 Parameter Measurement Information



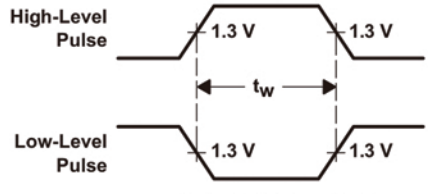
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



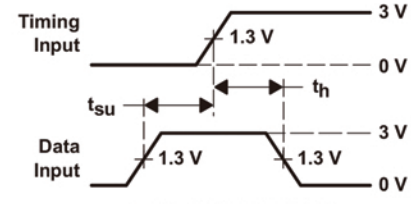
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



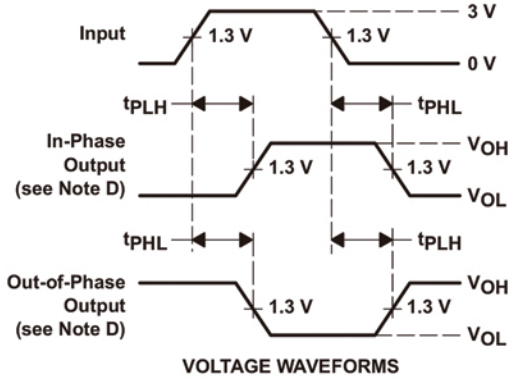
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



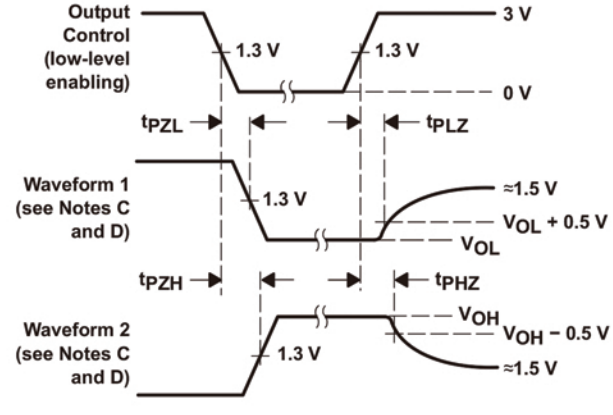
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r≤ 1.5 ns, t_f≤ 2.6 ns.

G. The outputs are measured one at a time, with one input transition per measurement.

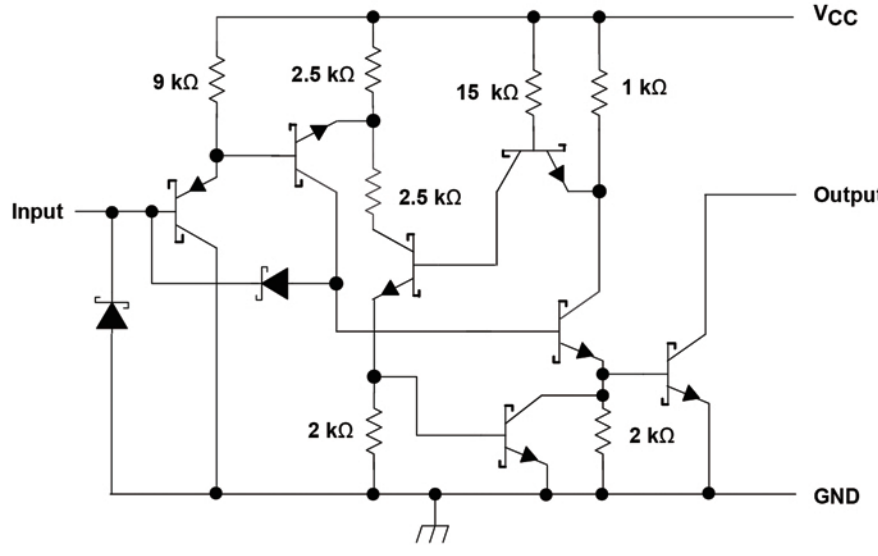
Figure 2. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The XD74LS06 devices are open-collector output inverters. The maximum sink current for the XD74LS06 device is 30 mA, and for the XD74LS06 device it is 40 mA. These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

8.2 Functional Block Diagram



8.3 Feature Description

The XD74LS06 devices can convert most TTL voltage circuit voltage level to MOS levels. The devices have high sink-current capability of up to 40 mA. The open-collector driver can be used for typical applications including Indicator lamps and relays.

8.4 Device Functional Modes

Table 1 lists the functional modes of the XD74LS06 devices.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	Hi-Z

9 Application and Implementation

9.1 Application Information

The open-collector device is suitable for high-drive and high-voltage translation applications.

9.2 Typical Application

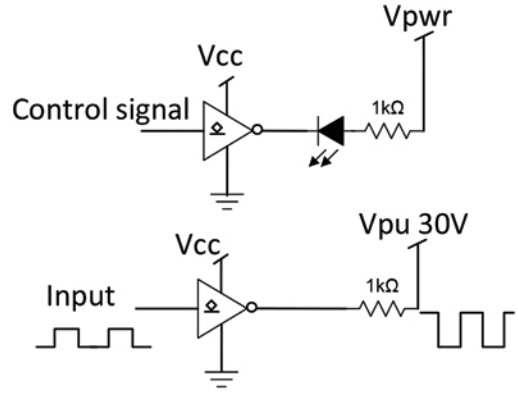


Figure 3. Application Schematic

9.2.1 Design Requirements

The XD74LS06 are open-collector devices which can sink current(up to 40 mA on XD74LS06) The devices can be used in applications such as LED drivers and voltage translation using pullup resistors.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents must not exceed (I_O max) per output.
   - Outputs can be pulled up to 30 V.

Typical Application (continued)

9.2.3 Application Curve

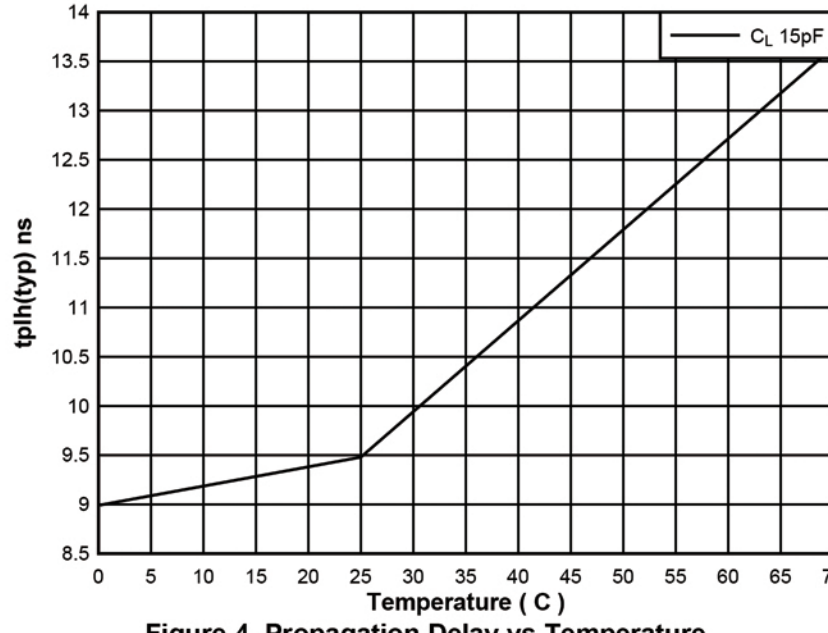


Figure 4. Propagation Delay vs Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor, and if there are multiple V_{CC} pins, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input and gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following rules must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} whichever make more sense or is more convenient. TI recommends keeping the signal lines as short and as straight as possible (see Figure 6). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1" long. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω as required by the application.

11.2 Layout Examples

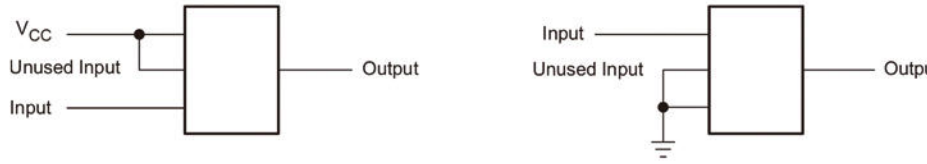


Figure 5. Layout Schematic

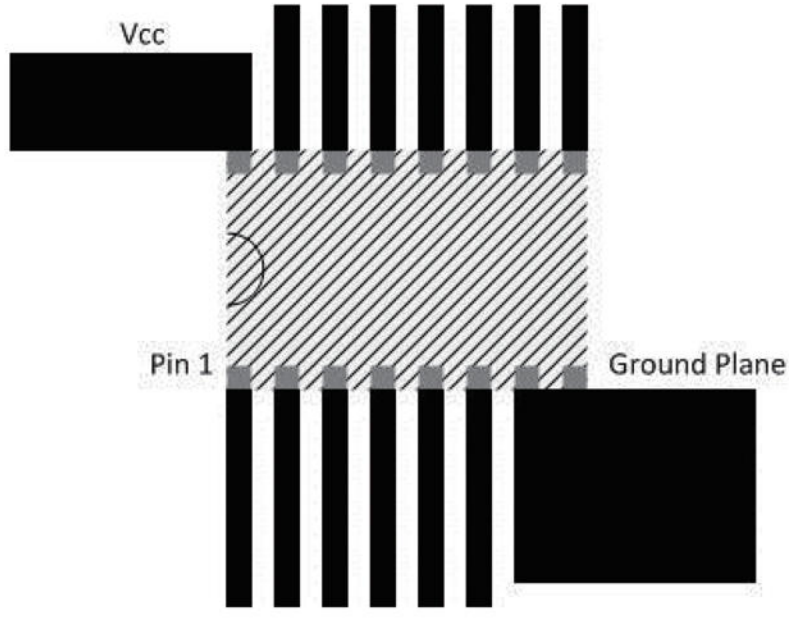
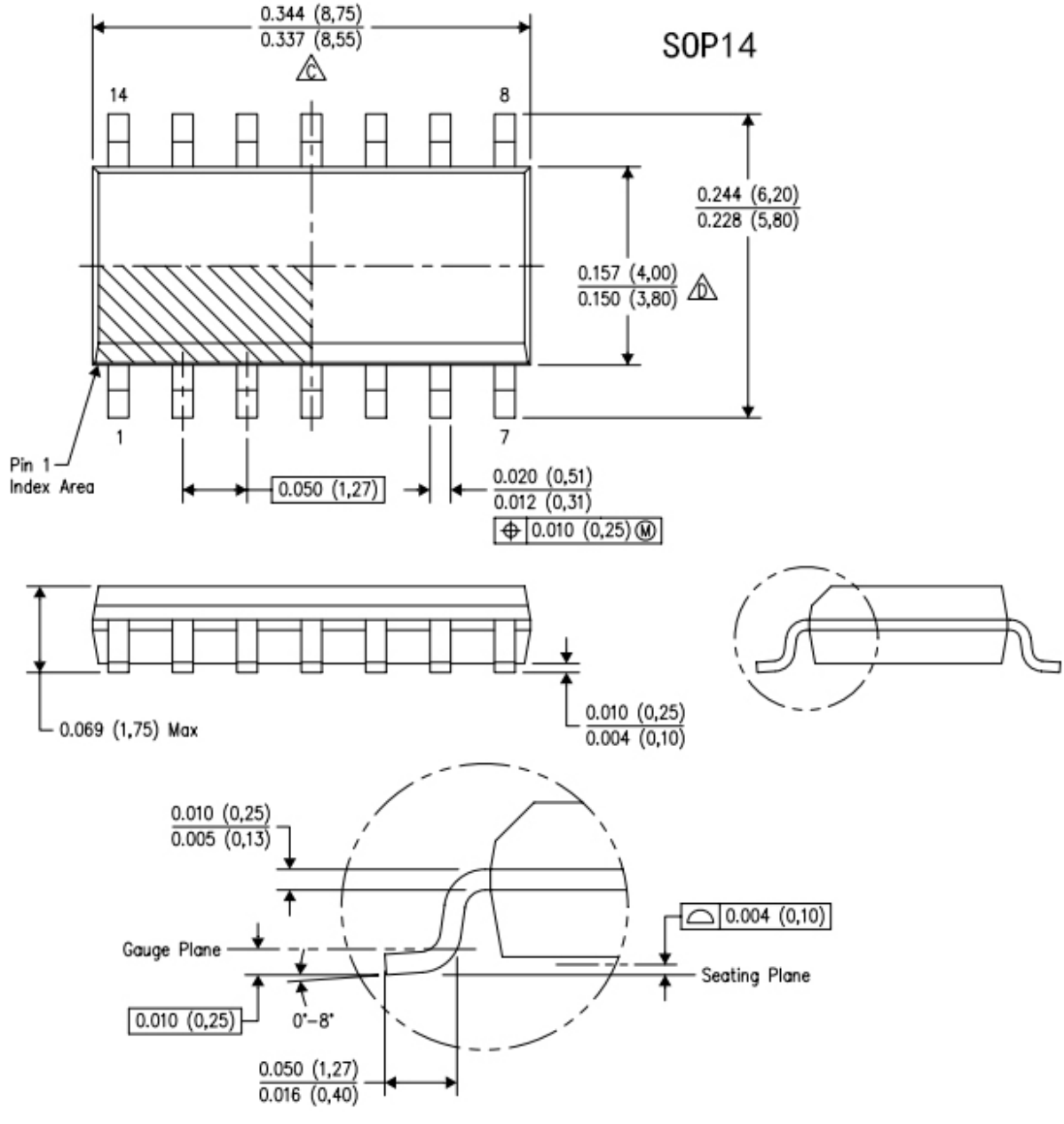
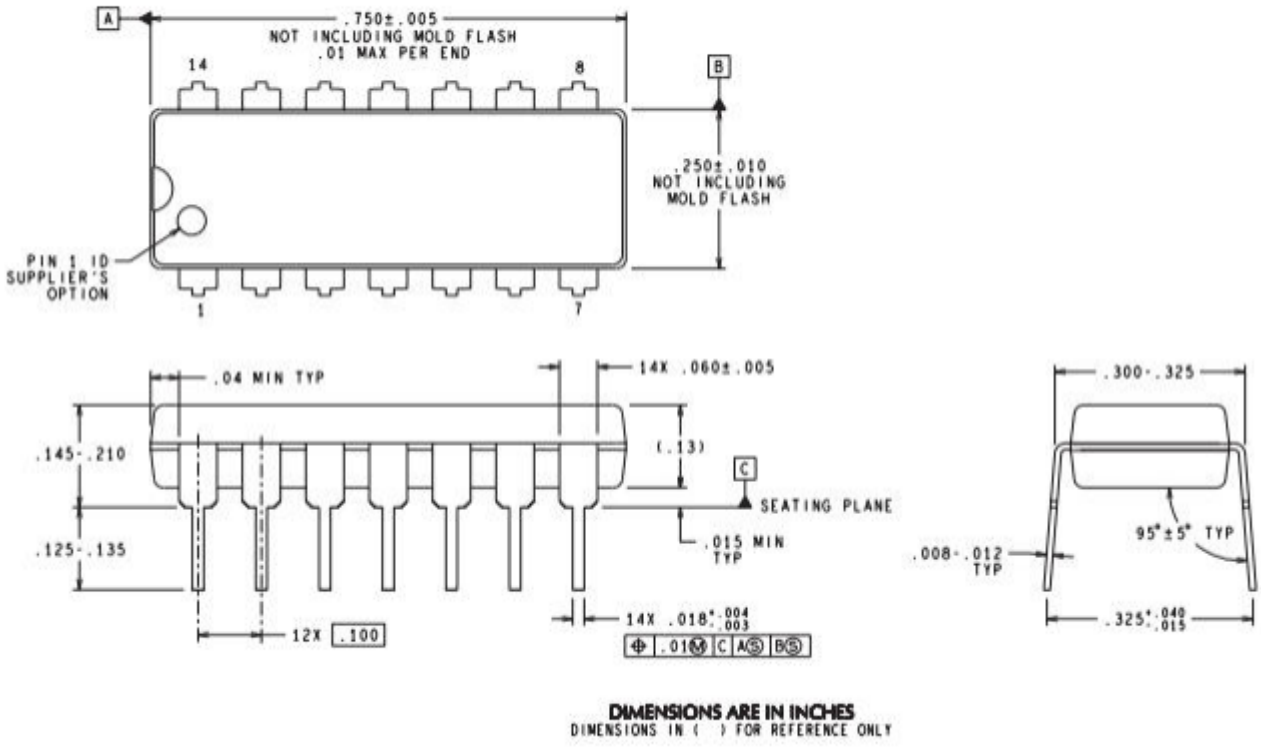


Figure 6. Signal Line Layout


SOP14
0.344 (8,75)
0.337 (8,55)
C
14
8
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
1
7
Pin 1
Index Area
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
0.004 (0,10)
Gauge Plane
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

DIP14



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