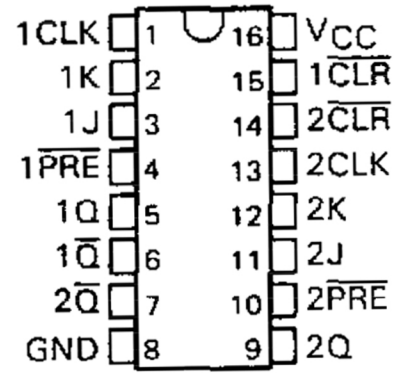
description

Thww dvvicw contain two indepMXJent j-k neQattve~fldue∗trigverBd flip-flops. A luw levet at the preset and clear inputs sots or resets the outputs regsrdlesB of the tevsis of the other Inputs. When preset and dear are Inacrive (high), data at the J and K inputs meeting the setup time rcquiremonts are traneferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a vdtago tsvef and is not directly related to the rise time of the dock pulse. Following tha hold time intevval, data at the J end K inputs rnay be nhangHri wifhmit affpering the I»vel3 at the outputs. These vetsatile flip-flops Mn perform aa toggle fllp-tiops by tying J and K h»gh.

74LS112

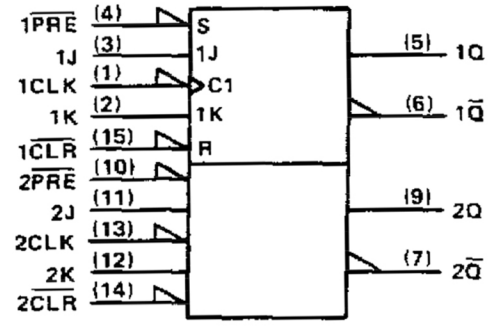


FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

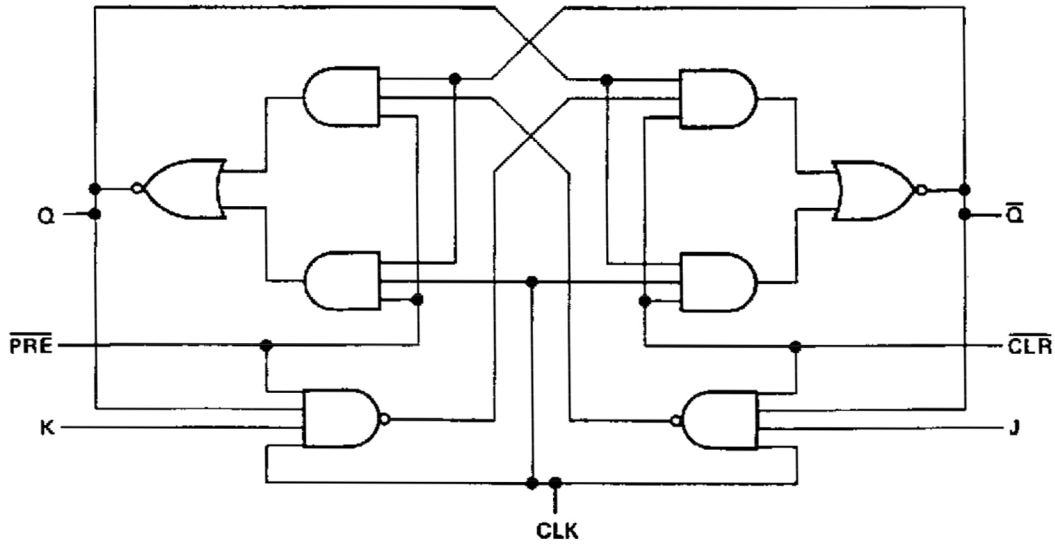
r TTw output in eonfigura^on orv not guar∗Att∗d to moM tX minimum kivela for V°h If the lows ∗t pro&et a(id Uvm are neer V|I minimum. FunhBfnionir this comigurttian » ncratwiQ； that 畑 ft WIN not perdflt wh«n either pc— or olmt rgg to its in active (high} level.

logic symbol‡



logic diagrams (positive logic)

74LS112



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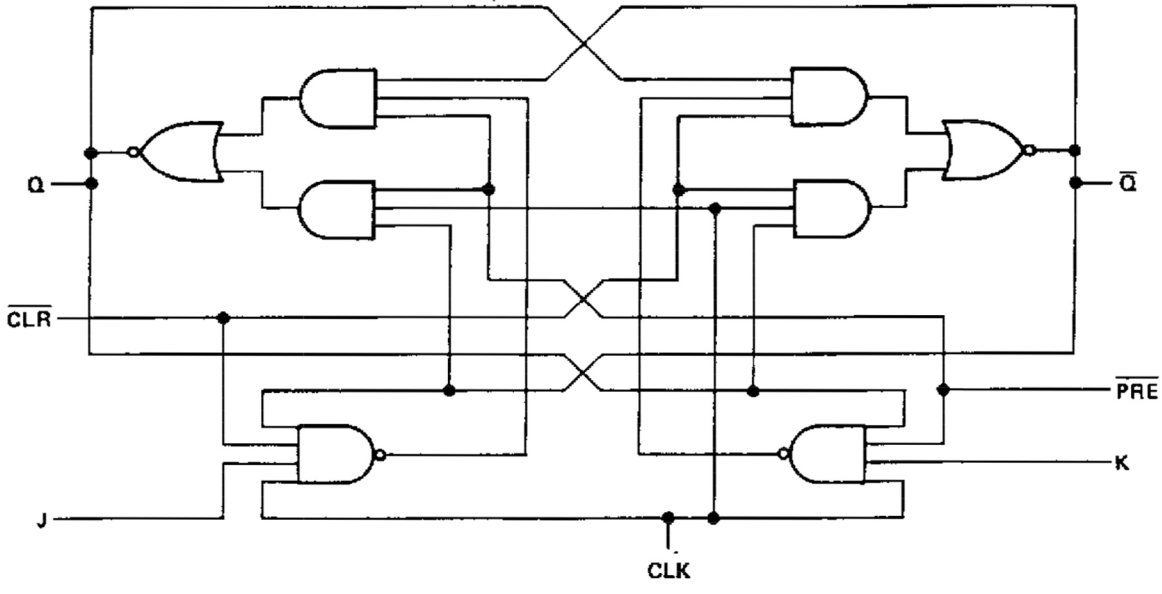
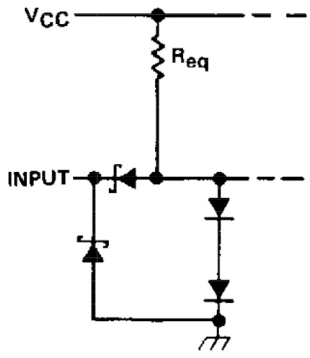


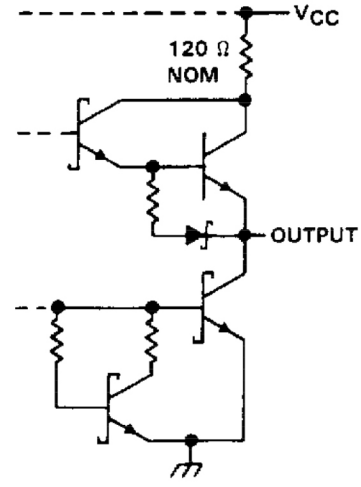
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

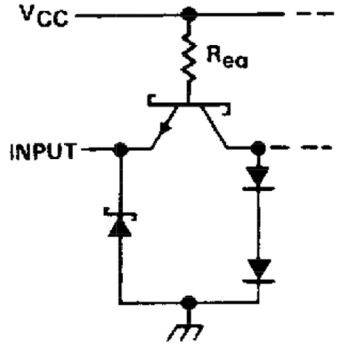


I_{IL} MAX	R_{eq} NOM
−0.4 mA	30 kΩ
−0.8 mA	8.25 kΩ

TYPICAL OF ALL OUTPUTS

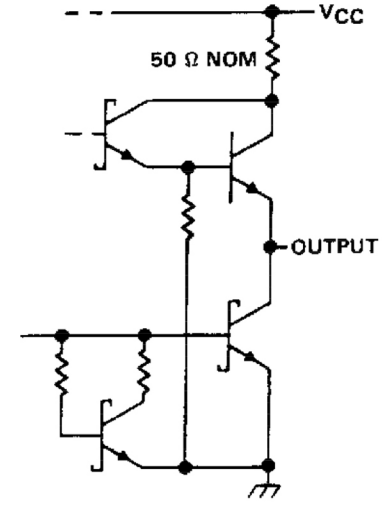


EQUIVALENT OF EACH INPUT



I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−4 mA	1.4 kΩ
−7 mA	900 Ω

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: 74LS112 . . . . . 7 V
74LS112 . . . . . 5.5 V
Operating free-air temperature range: 74LS112 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			XD74LS112			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency		0		30	MHz
t_w	Pulse duration	CLK high	20			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			
t_{su}	Set up time-before CLK↓	Data high or low	20			ns
		$\overline{CLR}$ inactive	25			
		$\overline{PRE}$ inactive	20			
t_h	Hold time-data after CLK↓		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			XD74LS112			UNIT
					MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.7	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.35	0.5	
I_I	J or K	V_{CC} = MAX,	V_I = 7 V				0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$						0.3	
	CLK						0.4	
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.7 V				20	μA
	$\overline{CLR}$ or $\overline{PRE}$						60	
	CLK						80	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−0.4	mA
	All other						−0.8	
I_{OS}§		V_{CC} = MAX,	see Note 2		−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX,	see Note 3			4	6	mA

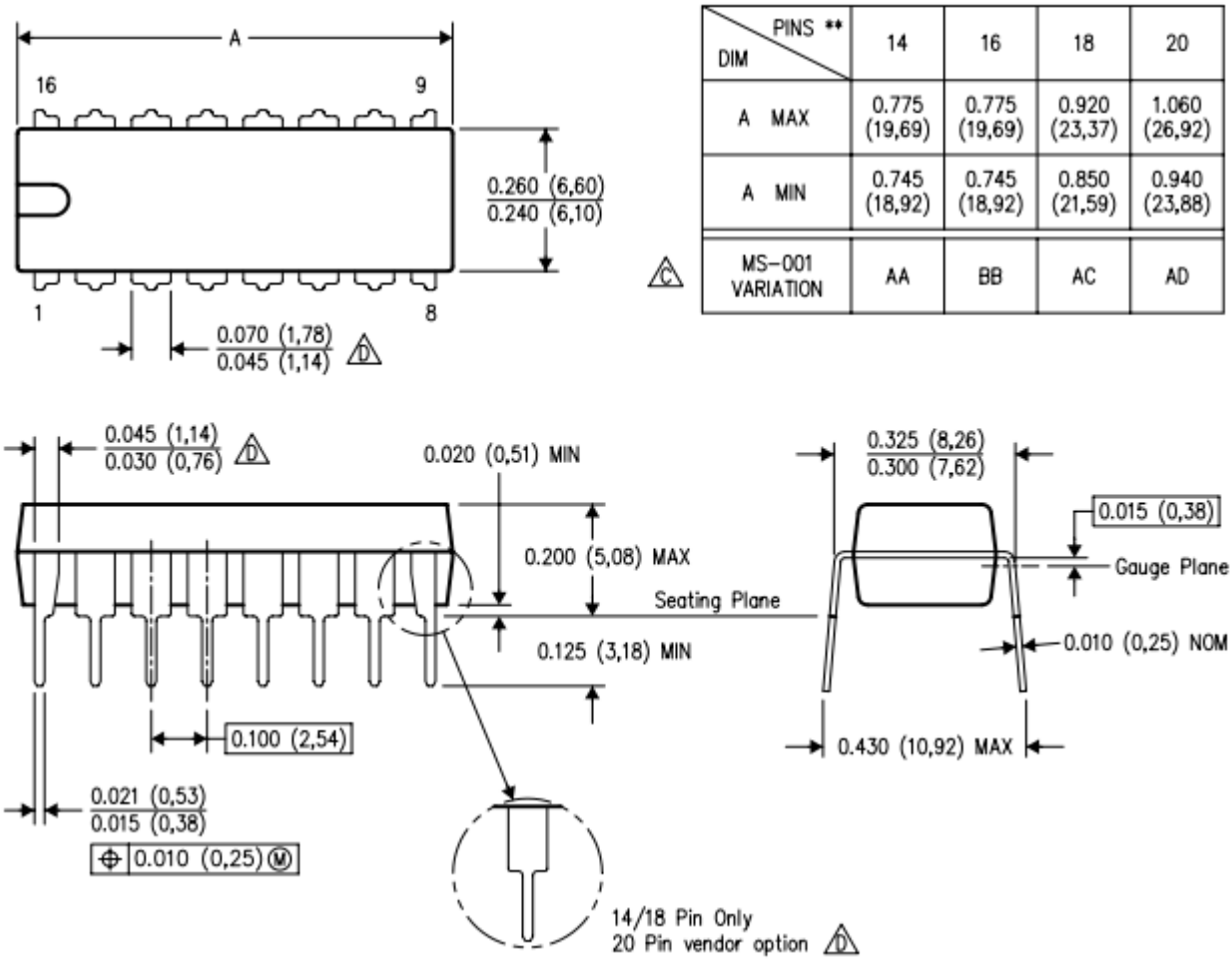
For ^nditiona abown at MIN or MAX. s the sppropritti vdut specified urtder rweoiwhtddtd o^wattng conditions.
*All typical vbIuob m st *cc ■ 5 V, Ta - 25flC.
Not more thee one ouWE X RfwvrM ar x He. am rM durMmn of uhrur^ircitiT AhntUd net Exceed cne secerxt
NOTES:
2. Por certain device whor» cUtacommotatifin con bo 8uaad by «ho«tihg ai output to ground, s teei may ba pvformea with Vq — 2.25 V Md 2.12SV for tfio *M family ond the '7, family, roepMtivefy. with tt» minimum and maximum Hmit® reduced to ww hdr uf the, maied valuoe,
3. with all cinpim open, is masured wim itift a and B ntirptm high in nim. at The time of m*Mr^ent, g dock input le ggr»d

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	30	45		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA

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