

XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

**Designed Specifically for High-Speed:
Memory Decoders
Data Transmission Systems**

**3 Enable Inputs to Simplify Cascading
and/or Data Reception**

Schottky-Clamped for High Performance

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

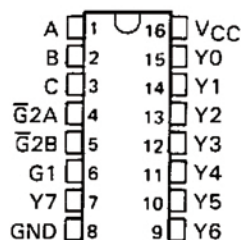
The XD74LS138, XL74LS138 and XD54LS138 decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The XD74LS138 and XL74LS138 are characterized for operation over the full military temperature range of -55°C to 125°C . The XD74LS138 and XL74LS138 are characterized for operation from 0°C to 70°C .

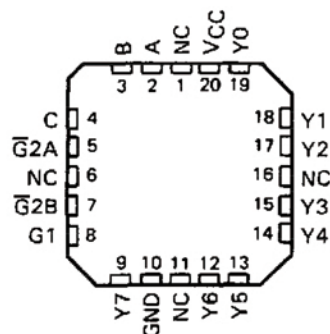
XD74LS138/XL74LS138/XD54LS138

(TOP VIEW)



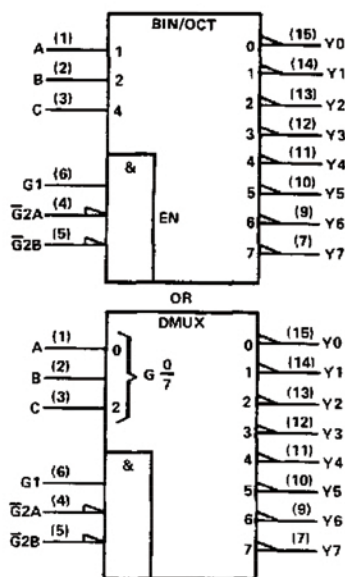
XD74LS138/XL74LS138

(TOP VIEW)



NC—No internal connection

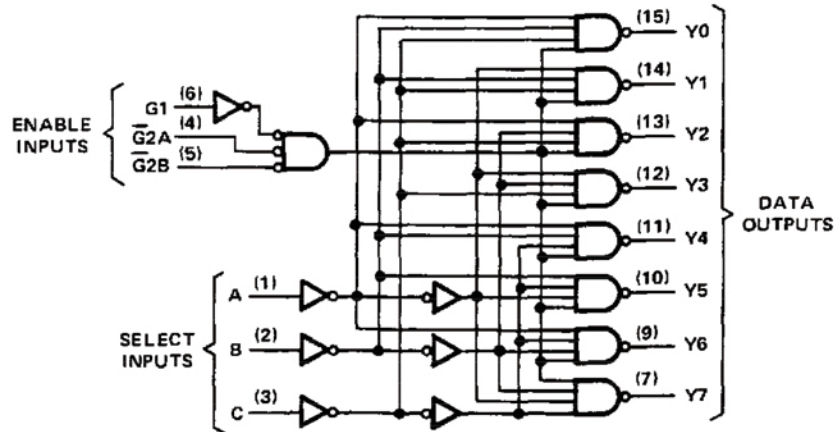
logic symbols †



XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

logic diagram and function table

XD74LS138/XL74LS138/XD54LS138



Pin numbers shown are for D, J, N, and W packages.

XD74LS138/XL74LS138/XD54LS138

FUNCTION TABLE

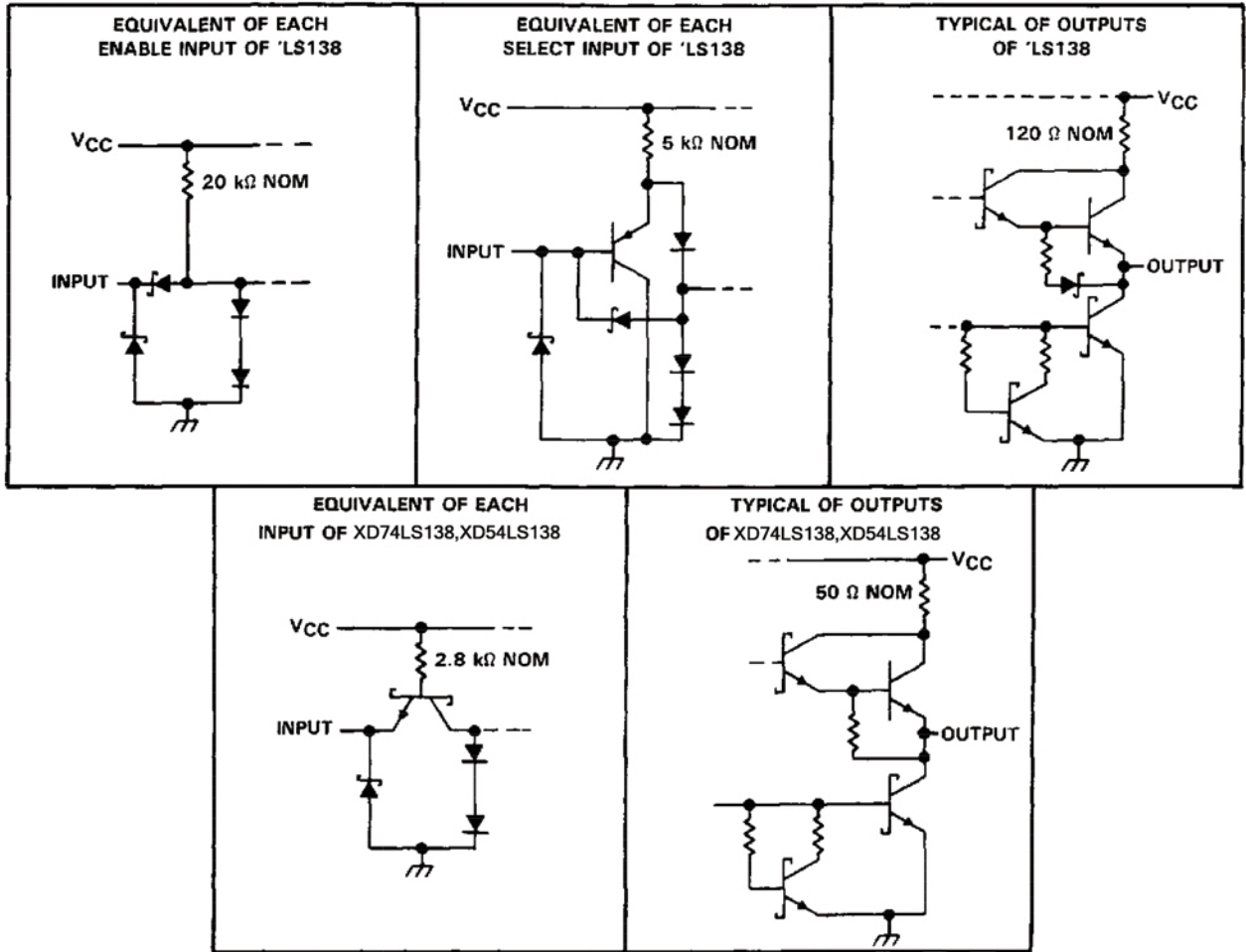
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\overline{G2}^*$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = \overline{G2A} + \overline{G2B}$

H = high level, L = low level, X = irrelevant

XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: XD54LS138	-55 °C to 125 °C
XD74LS138 XL74LS138	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

recommended operating conditions

		XD54LS138			XD74LS138			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage	0.7			0.8			V		
I _{OH}	High-level output current	-0.4			-0.4			mA		
I _{OL}	Low-level output current	4			8			mA		
T _A	Operating free-air temperature	-55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	XD54LS138			XD74LS138			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V	
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA		0.25	0.4	0.25	0.4	V	
		I _{OL} = 8 mA				0.35	0.5		
I _I	V _{CC} = MAX, V _I = 7 V	0.1			0.1			mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7 V	20			20			μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	Enable		-0.4		-0.4		mA	
		A, B, C		-0.2		-0.2			
I _{OS} [§]	V _{CC} = MAX	-20	-100	-20	-100			mA	
I _{CC}	V _{CC} = MAX, Outputs enabled and open	6.3		10		6.3		10	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	XD54LS138 XD74LS138			UNIT
					MIN	TYP	MAX	
t _{PLH}	Binary Select	Any	2	R _L = 2 kΩ, C _L = 15 pF, See Note 2	11	20	20	ns
t _{PHL}					18	41	41	ns
t _{PLH}			3		21	27	27	ns
t _{PHL}					20	39	39	ns
t _{PLH}	Enable	Any	2		12	18	18	ns
t _{PHL}					20	32	32	ns
t _{PLH}			3		14	26	26	ns
t _{PHL}					13	38	38	ns

[†]t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: XD54LS138	-55°C to 125°C
XD74LS138	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		XD54LS138			XD74LS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
I_{OH}	High-level output current	-1			-1			mA
I_{OL}	Low-level output current	20			20			mA
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	XD54LS138 XD74LS138			UNIT		
		MIN	TYP [‡]	MAX			
		V_{IK}	$V_{CC} = \text{MIN.}$	$I_I = -18 \text{ mA}$		-1.2	V
V_{OH}	$V_{CC} = \text{MIN.}$	$V_{IH} = 2 \text{ V.}$	$V_{IL} = 0.8 \text{ V.}$	$I_{OH} = -1 \text{ mA}$		V	
				SN54S'	2.5	3.4	
				SN74S'	2.7	3.4	
V_{OL}	$V_{CC} = \text{MIN.}$	$V_{IH} = 2 \text{ V.}$	$V_{IL} = 0.8 \text{ V.}$	$I_{OL} = 20 \text{ mA}$	0.5		V
I_I	$V_{CC} = \text{MAX.}$	$V_I = 5.5 \text{ V}$			1		mA
I_{IH}	$V_{CC} = \text{MAX.}$	$V_I = 2.7 \text{ V}$			50		μA
I_{IL}	$V_{CC} = \text{MAX.}$	$V_I = 0.5 \text{ V}$			-2		mA
I_{OS}^{\S}	$V_{CC} = \text{MAX.}$				-40	-100	mA
I_{CC}	$V_{CC} = \text{MAX.}$	Outputs enabled and open			49	74	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

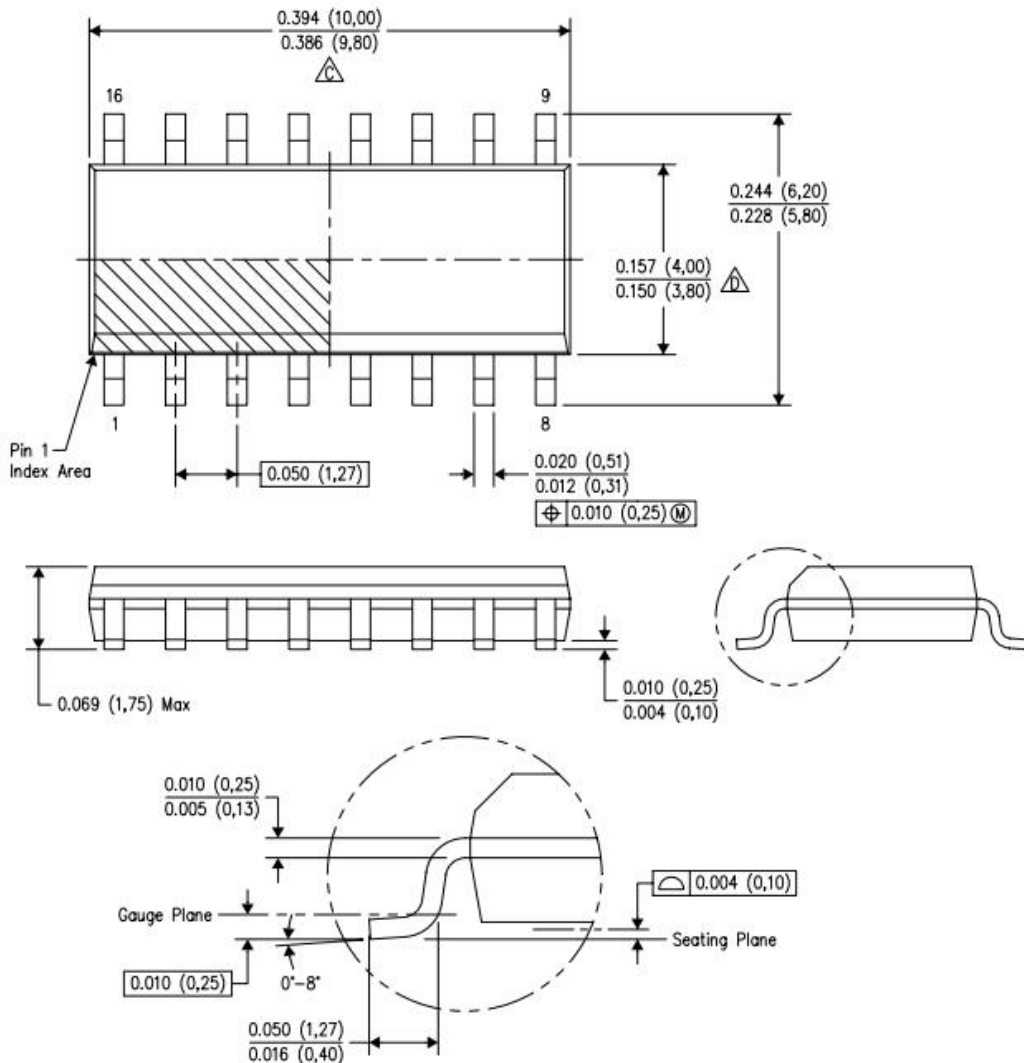
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	XD54LS138 XD74LS138			UNIT
					MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	$R_L = 280\ \Omega$, $C_L = 15\ \text{pF}$. See Note 2		4.5	7	ns
t_{PHL}						7	10.5	ns
t_{PLH}			3			7.5	12	ns
t_{PHL}						8	12	ns
t_{PLH}	Enable	Any	2			5	8	ns
t_{PHL}						7	11	ns
t_{PLH}			3			7	11	ns
t_{PHL}						7	11	ns

† t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

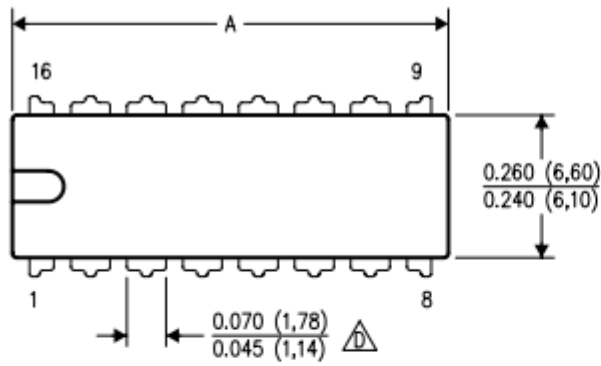
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SOP

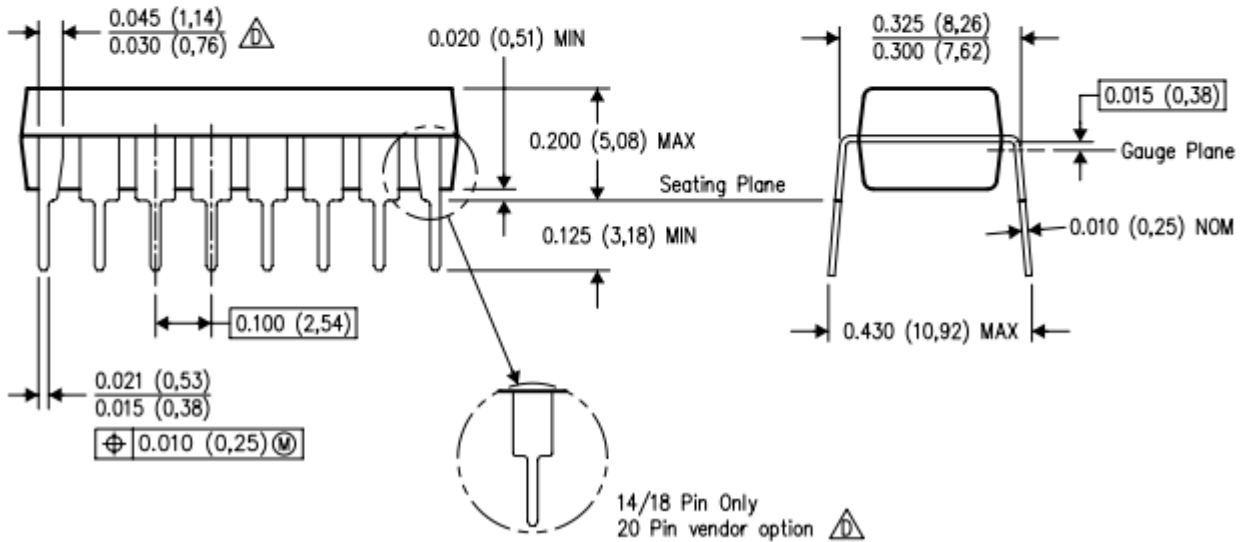


XD74LS138 DIP16/XL74LS138 SOP16/XD54LS138 DIP16

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



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