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XD74LS14 DIP-14
XL74LS14 SOP-14

1 Features

- Operation From Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

2 Applications

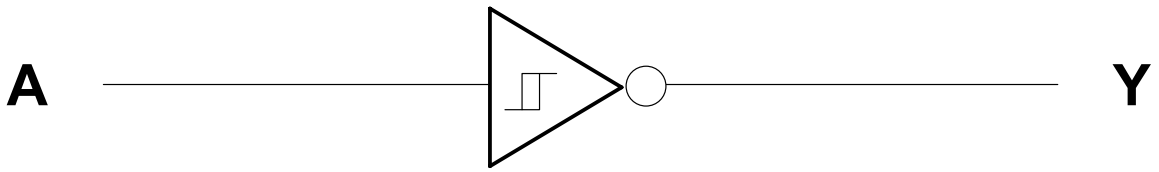
- HVAC Gateways
- Residential Ductless Air Conditioning Outdoor Units
- Robotic Controls
- Industrial Stepper Motors
- Power Meter and Power Analyzers
- Digital Input Modules for Factory Automation

3 Description

Each circuit in XD/XL74LS14 functions asan inverter. However, because of the Schmitt-Triggeraction, they have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

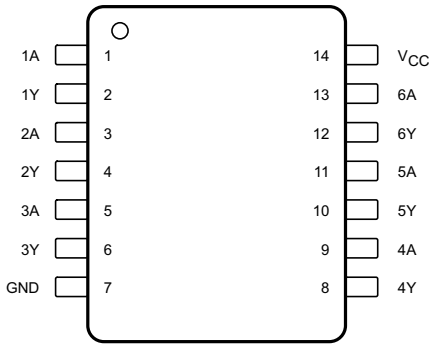
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

4 Logic Diagram (Positive Logic)



5 Pin Configuration and Functions

DIP/SOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DIP/SOP		
1A	1	I	Channel 1 input
1Y	2	O	Channel 1 output
2A	3	I	Channel 2 input
2Y	4	O	Channel 2 output
3A	5	I	Channel 3 input
3Y	6	O	Channel 3 output
4A	9	I	Channel 4 input
4Y	8	O	Channel 4 output
5A	11	I	Channel 5 input
5Y	10	O	Channel 5 output
6A	13	I	Channel 6 input
6Y	12	O	Channel 6 output
GND	7	—	Ground
NC	—	—	No internal connection
V_{CC}	14	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage	XD/XL74LS14		5.5	V
			7	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	XD/XL74LS14	4.5	5	5.5	V
			4.75	5	5.25	
I_{OH}	High-level output current	XD/XL74LS14			–0.8	mA
					–0.4	
I_{OL}	Low-level output current	XD/XL74LS14			16	mA
					4	
					8	
T_A	Operating free-air temperature	XD/XL74LS14	–55		125	°C
			0		70	

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{T+}	V_{CC} = 5 V	74LS14	1.5	1.7	2	V
			1.4	1.6	1.9	
V_{T-}	V_{CC} = 5 V		0.6	0.9	1.1	V
			0.5	0.8	1	
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V		0.4	0.8		V
V_{IK}	V_{CC} = MIN, I_I = –12 mA, XD/XL74LS14				–1.5	V
	V_{CC} = MIN, I_I = –18 mA, XD/XL74LS14				–1.5	
V_{OH}	V_{CC} = MIN, V_I = 0.6 V, I_{OH} = –0.8 mA, XD/XL74LS14		2.4	3.4		V
	V_{CC} = MIN, V_I = 0.5 V, I_{OH} = –0.4 mA, XD/XL74LS14		2.4	3.4		
V_{OL}	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA, XD/XL74LS14			0.2	0.4	V
	V_{CC} = MIN, V_I = 1.9 V	I_{OL} = 4 mA, XD/XL74LS14		0.25	0.4	
		I_{OL} = 8 mA, XD/XL74LS14		0.35	0.5	
I_{T+}	V_{CC} = 5 V, V_I = V_{T+}	XD/XL74LS14		–0.43		mA
				–0.14		
I_{T-}	V_{CC} = 5 V, V_I = V_{T-}	XD/XL74LS14		–0.56		mA
				–0.18		
I_I	V_{CC} = MAX, V_I = 5.5 V, XD/XL74LS14				1	mA
	V_{CC} = MAX, V_I = 7 V, XD/XL74LS14				0.1	
I_{IH}	V_{CC} = MAX, V_{IH} = 2.4 V, XD/XL74LS1414				40	μA
	V_{CC} = MAX, V_{IH} = 2.7 V, XD/XL74LS14				20	
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V	XD/XL74LS14		–0.8	–1.2	mA
					–0.4	
I_{OS}[3]	V_{CC} = MAX	XD/XL74LS14	–18		–55	mA
			–20		–100	
I_{CCH}	V_{CC} = MAX	XD/XL74LS14		22	36	mA
				8.6	16	
I_{CCL}	V_{CC} = MAX	XD/XL74LS14		39	60	mA
				12	21	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) Not more than one output should be shorted at a time.

6.5 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted; see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω and C_L = 15 pF, or R_L = 2 kΩ and C_L = 15 pF		15	22	ns
t_{PHL}	A	Y	R_L = 400 Ω and C_L = 15 pF, or R_L = 2 kΩ and C_L = 15 pF		15	22	ns

6.5.1 XD/XL74LS14 Circuits

Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for XD/XL74LS14 only.

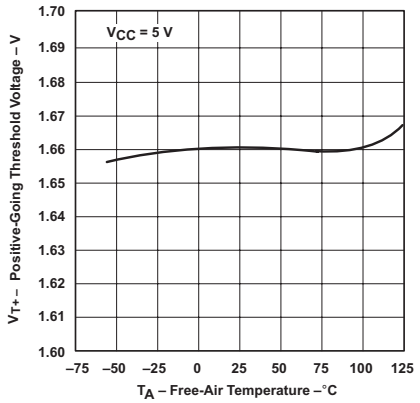


Figure 1. Positive-Going Threshold Voltage vs Free-Air Temperature

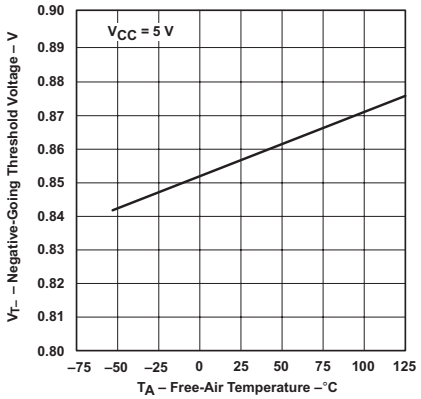


Figure 2. Negative-Going Threshold Voltage vs Free-Air Temperature

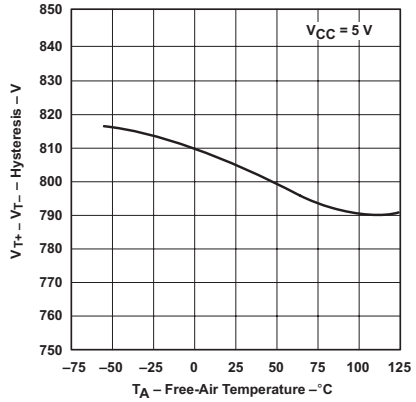


Figure 3 Hysteresis vs Free-Air Temperature

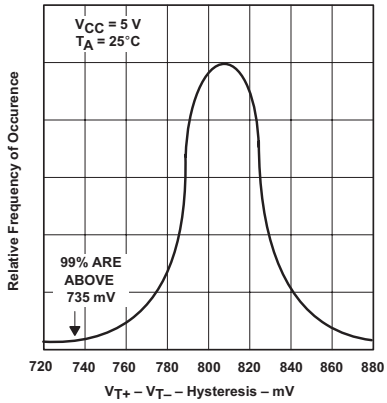


Figure 4 Distribution of Units for Hysteresis

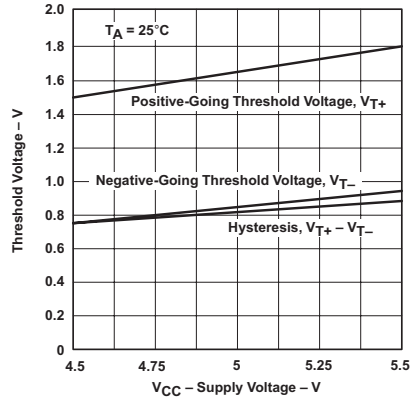


Figure 5 Threshold Voltages and Hysteresis vs Supply Voltage

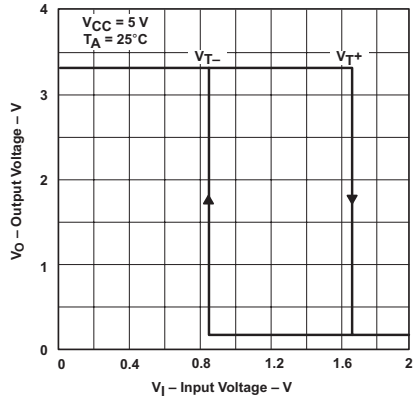


Figure 6 Output Voltage vs Input Voltage

7 Parameter Measurement Information

7.1 Series XD/XL74LS14 Devices

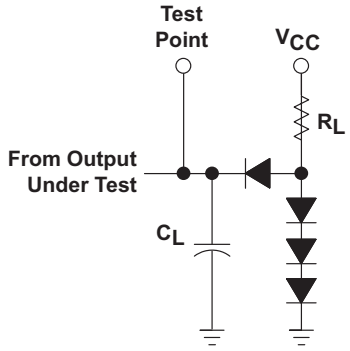


Figure 7 Load Circuit For 2-State Totem-Pole Outputs

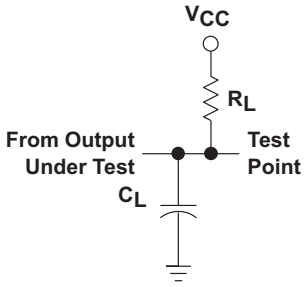


Figure 8 Load Circuit For Open-Collector Outputs

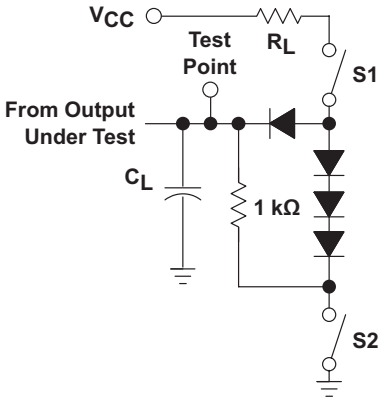


Figure 9 Load Circuit For 3-State Outputs

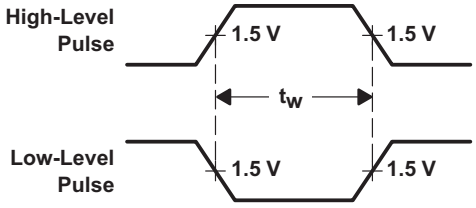


Figure 10 Voltage Waveforms Pulse Durations

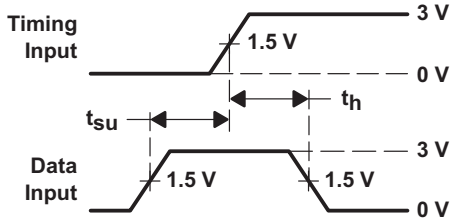


Figure 11 Voltage Waveforms Setup and Hold Times

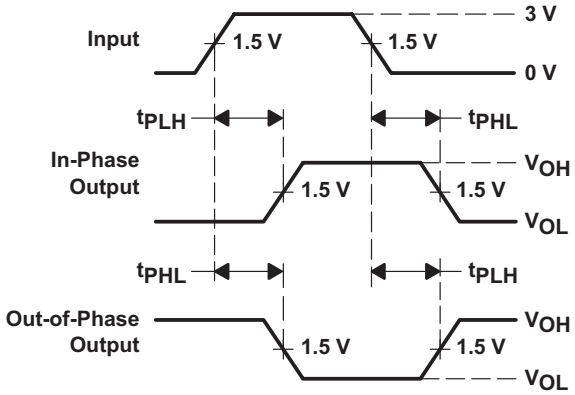
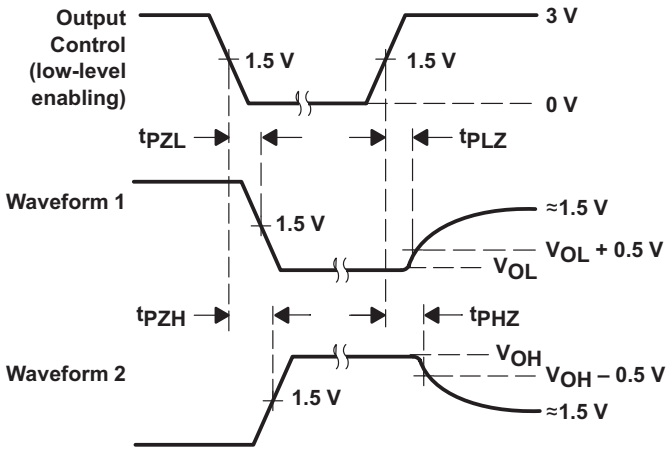


Figure 12 Voltage Waveforms Propagation Delay Times

Series XD/XL74LS14 Devices (continued)



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. The outputs are measured one at a time with one input transition per measurement.

Figure 13 Voltage Waveforms Enable and Disable Times, 3-State Outputs

7.2 Series XD/XL74LS14 Devices

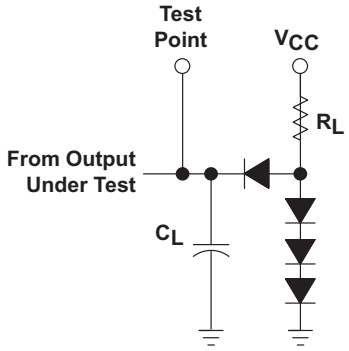


Figure 14 Load Circuit For 2-State Totem-Pole Outputs

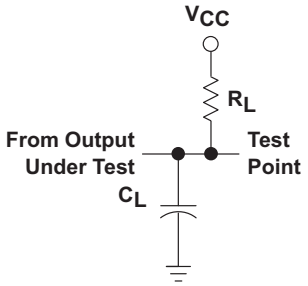


Figure 15 Load Circuit For Open-Collector Outputs

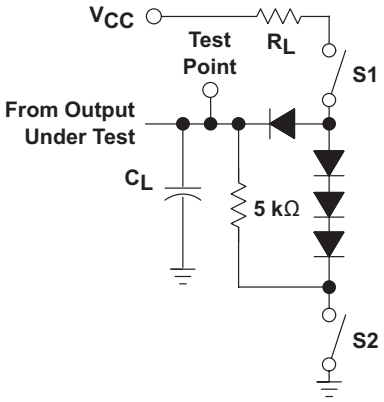


Figure 16 Load Circuit For 3-State Outputs

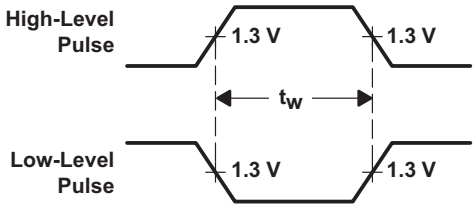


Figure 17 Voltage Waveforms Pulse Durations

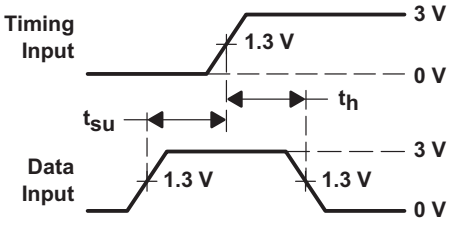


Figure 18 Voltage Waveforms Setup and Hold Times

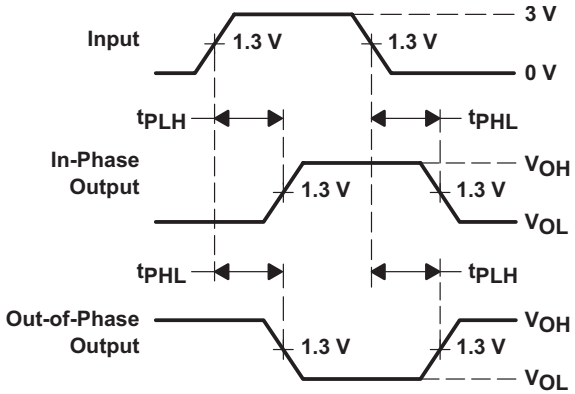
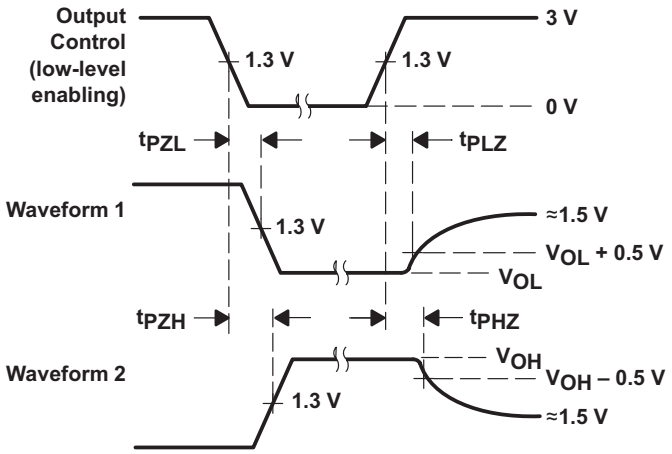


Figure 19 Voltage Waveforms Propagation Delay Times

Series XD/XL74LS14 Devices (continued)



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.

G. The outputs are measured one at a time with one input transition per measurement.

Figure 20 Voltage Waveforms Enable and Disable Times, 3-State Outputs

Typical Application (continued)

8 Application Curve

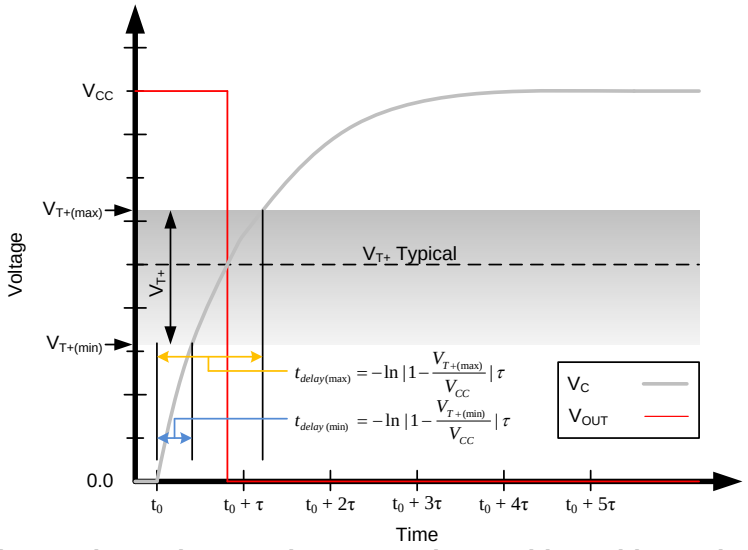


Figure 21 Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold

8.1 System Examples

Here are some examples of various applications using the XD/XL74LS14 device.

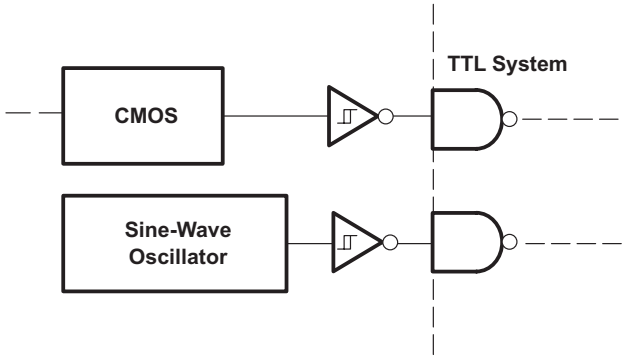


Figure 22 TTL System Interface For Slow Input Waveforms

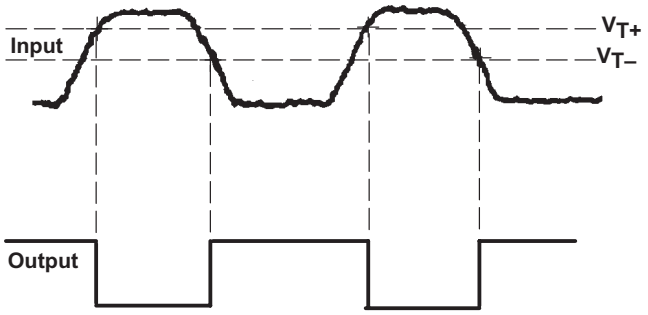


Figure 23 Pulse Shaper

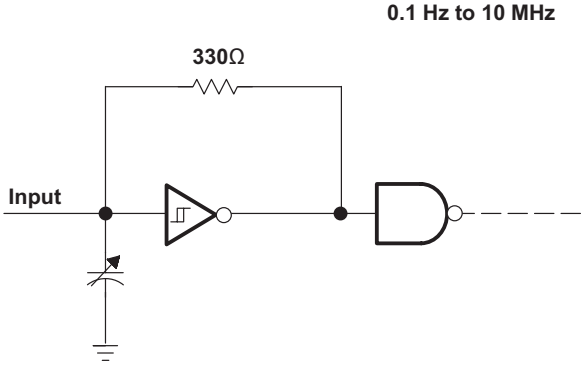


Figure 24 Multivibrator

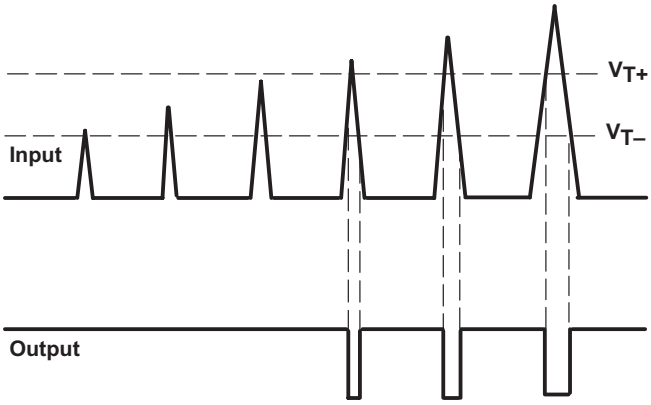
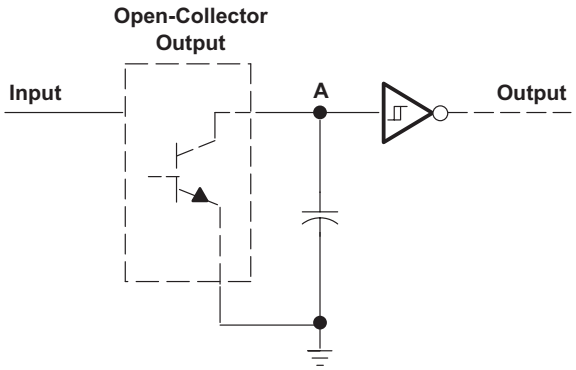


Figure 25 Threshold Detector



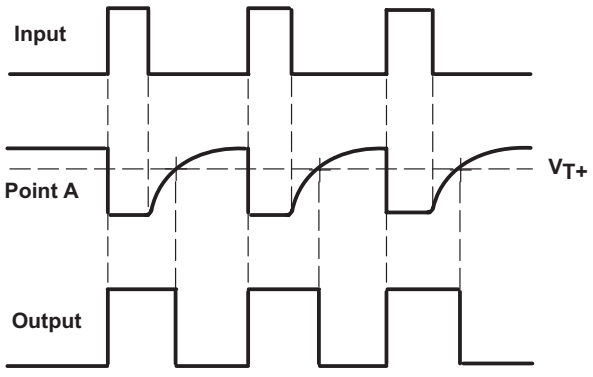


Figure 26 Pulse Stretcher

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. The V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends using a 0.1-µF capacitor on the V_{CC} terminal, and must be placed as close as possible to the pin for best results.

10 Layout

10.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

10.2 Layout Example

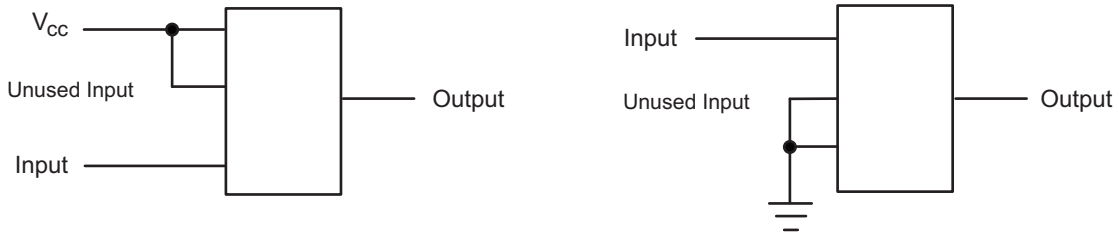
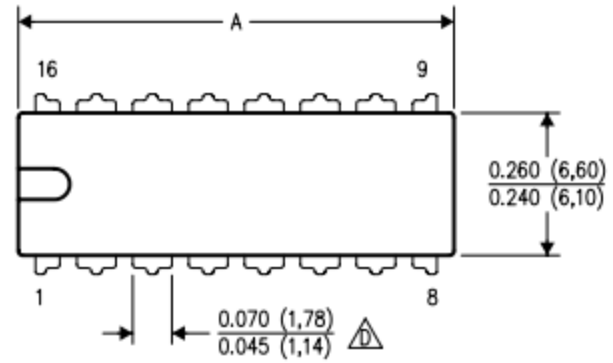


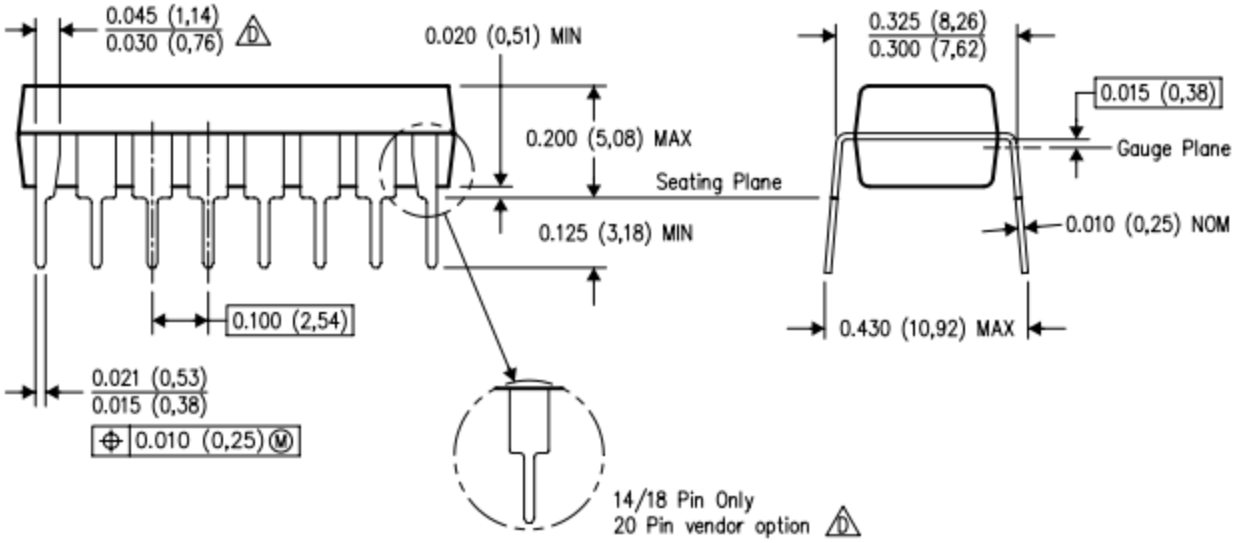
Figure 27 Layout Diagram

DIP

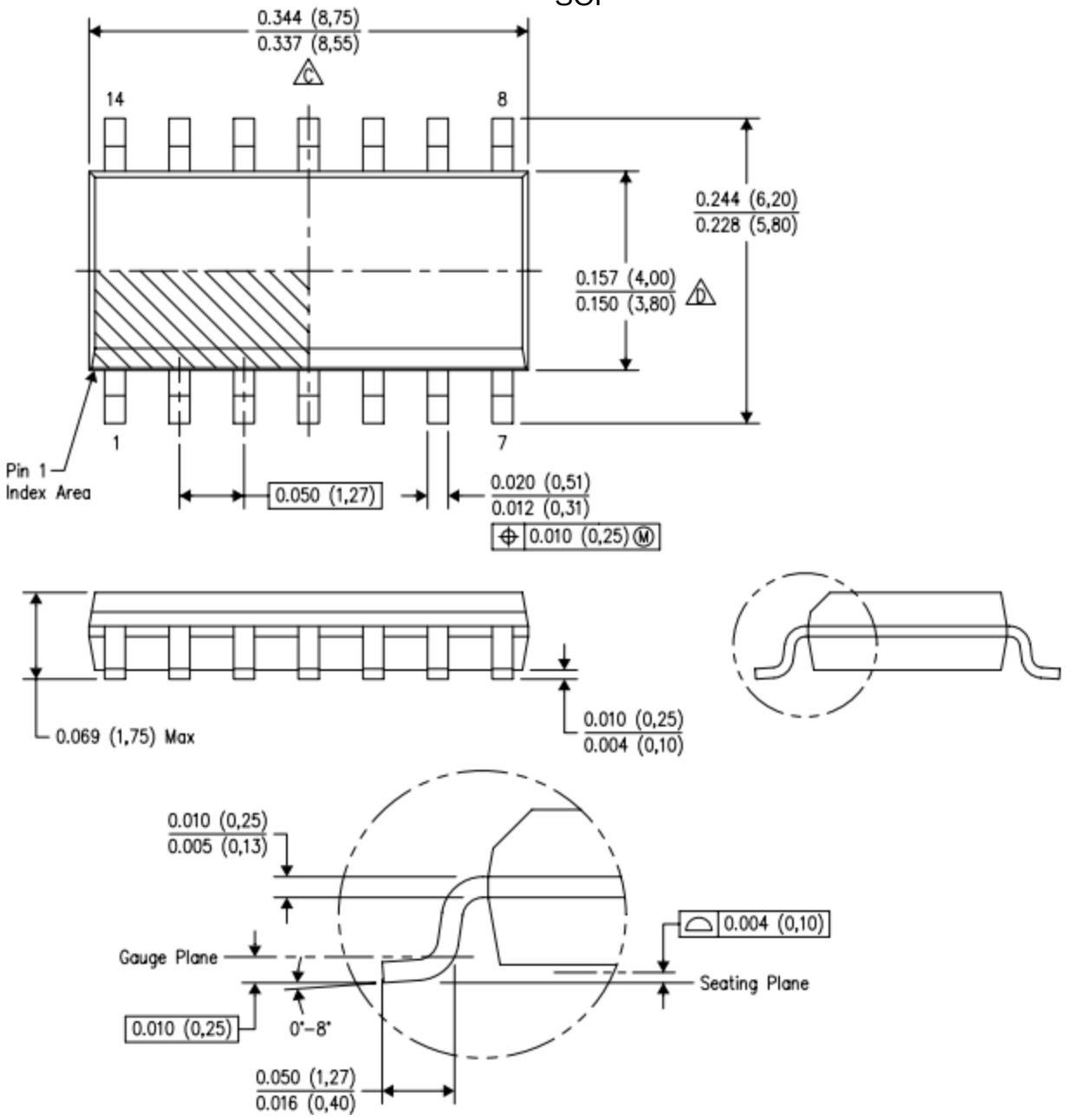


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

C



SOP



以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA

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