- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
74LS165	35 MHz	90 mW

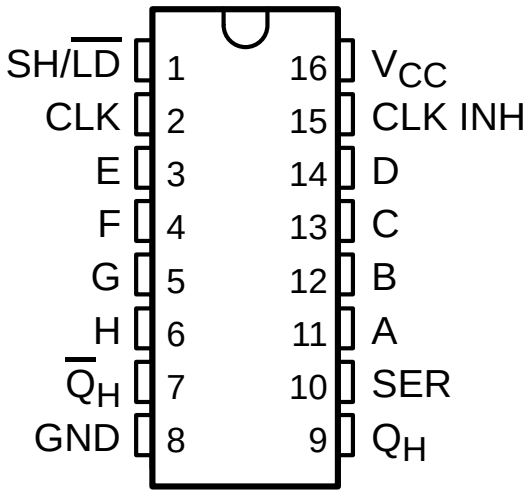
description

74LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual, direct data inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. These registers also feature gated clock (CLK) inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a two-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with SH/$\overline{LD}$ high enables the other clock input. Clock inhibit (CLK INH) should be changed to the high level only while CLK is high. Parallel loading is inhibited as long as SH/$\overline{LD}$ is high. Data at the parallel inputs are loaded directly into the register while SH/$\overline{LD}$ is low, independently of the levels of CLK, CLK INH, or serial (SER) inputs.

74LS165

(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	DIP	Tube	XD74LS165	XD74LS165
	SOP	Tube	XL74LS165	XL74LS165
		Tape and reel	XL74LS165	

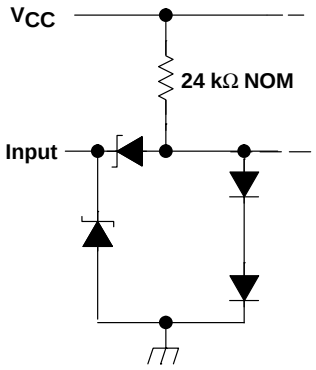
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A . . . H	$\overline{Q}_A$	$\overline{Q}_B$	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

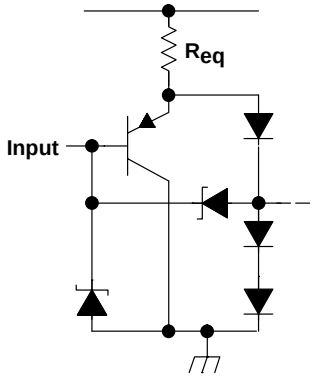
schematics of inputs and outputs

74LS165

EQUIVALENT OF PARALLEL INPUTS AND SERIAL INPUT

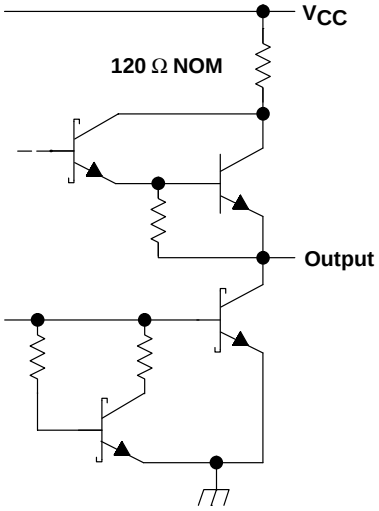


EQUIVALENT OF ALL OTHER INPUTS

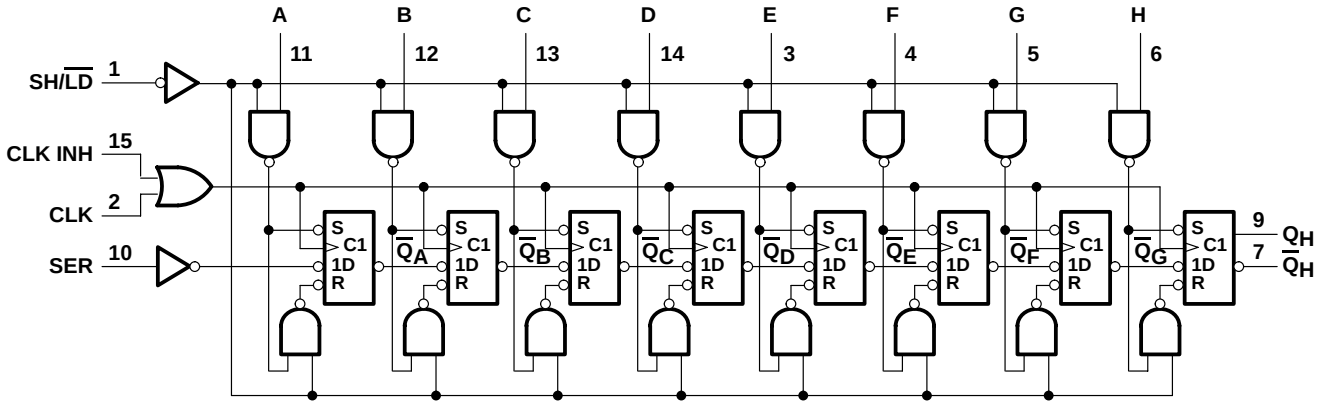


CLK, CLK INH: R_{eq} = 10 kΩ NOM
SH/$\overline{LD}$: R_{eq} = 13 kΩ NOM

TYPICAL OF BOTH OUTPUTS

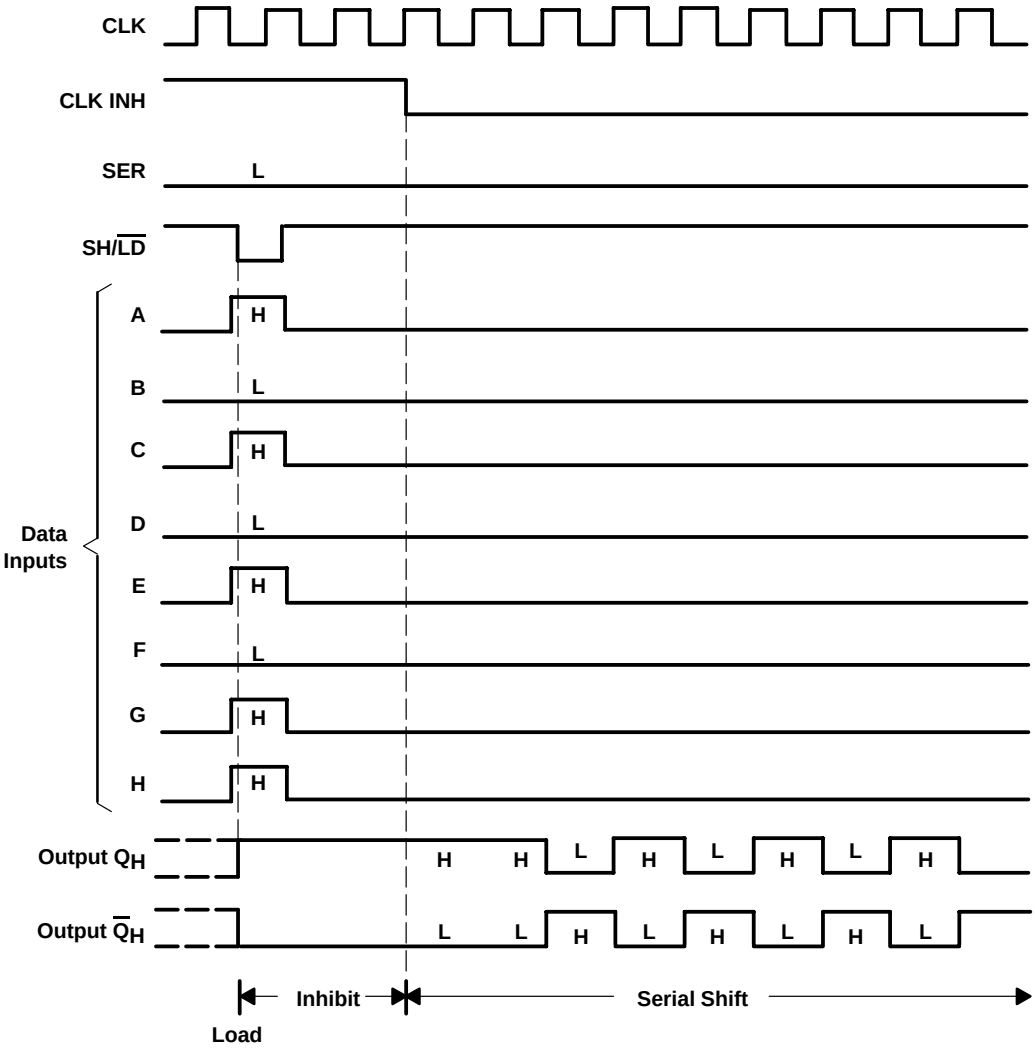


logic diagram (positive logic)



Pin numbers shown are for D, J, N, NS, and W packages.

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I: 74LS165	7 V
Interemitter voltage (see Note 2)	5.5 V
Package thermal impedance θ_{JA} (see Note 3): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the SH/$\overline{LD}$ input in conjunction with the CLK INH input.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			74LS165			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency		0		25	MHz
$t_{w(clock)}$	Width of clock input pulse	Clock high	15			ns
		Clock low	25			
$t_{w(load)}$	Width of load input pulse	Clock high	25			ns
		Clock low	17			
t_{su}	Clock-enable setup time		30			ns
t_{su}	Parallel input setup time		10			ns
t_{su}	Serial input setup time		20			ns
t_{su}	Shift setup time		45			ns
t_h	Hold time at any input		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†				74LS165			UNIT
					MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –18 mA					–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = MAX,	I_{OH} = –0.4 mA	2.7	3.5		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4	V
				I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V					0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V					20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V					–0.4	mA
I_{OS}§	V_{CC} = MAX				–20		–100	mA
I_{CC}	V_{CC} = MAX,					18	30	mA

NOTE 4. With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/$\overline{LD}$, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

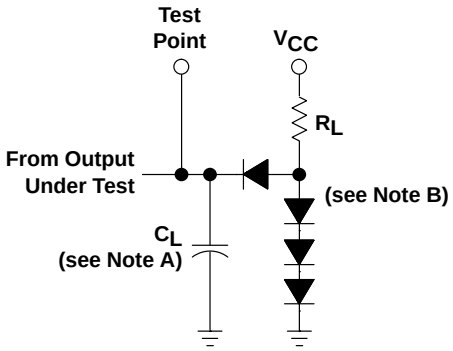
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

74LS165 switching characteristics, V_{CC} = 5 V, T_A = 25°C

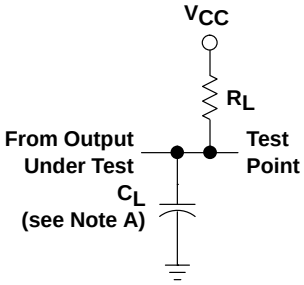
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	35		MHz
t_{PLH}	$\overline{LD}$	Any	R_L = 2 kΩ, C_L = 15 pF		21	35	ns
t_{PHL}					26	35	
t_{PLH}	CLK	Any	R_L = 2 kΩ, C_L = 15 pF		14	25	ns
t_{PHL}					16	25	
t_{PLH}	H	Q_H	R_L = 2 kΩ, C_L = 15 pF		13	25	ns
t_{PHL}					24	30	
t_{PLH}	H	$\overline{Q}_H$	R_L = 2 kΩ, C_L = 15 pF		19	30	ns
t_{PHL}					17	25	

† f_{max} = maximum clock frequency, t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output

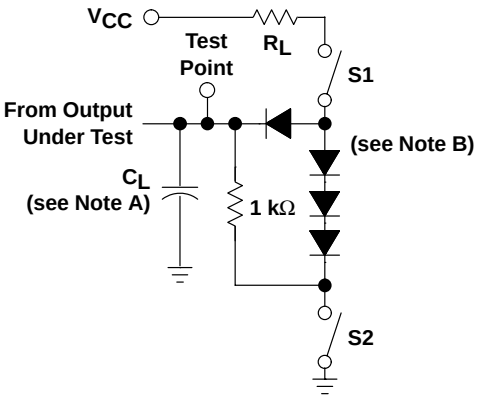
PARAMETER MEASUREMENT INFORMATION



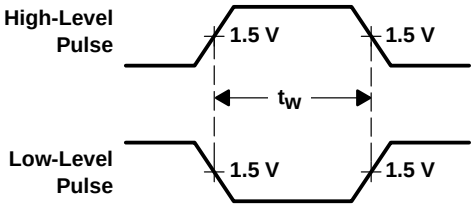
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



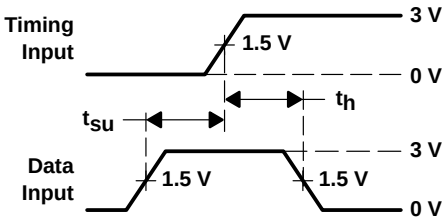
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



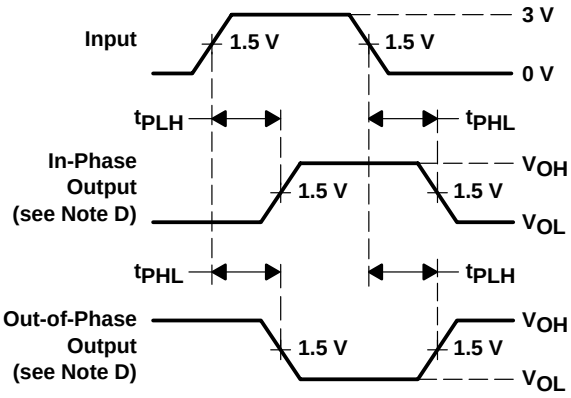
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



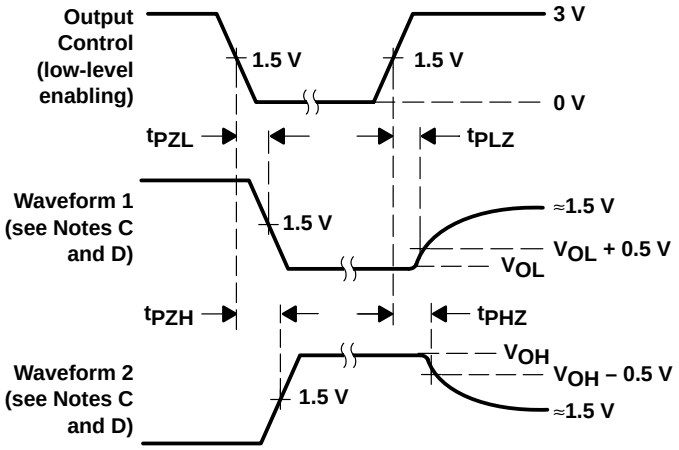
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

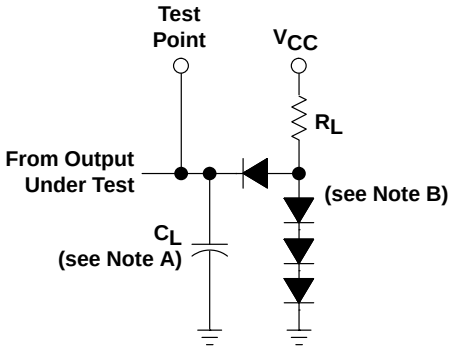


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

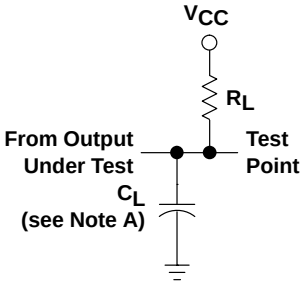
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 74LS165 devices and t_r and $t_f \leq 2.5$ ns for Series 74LS165 devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

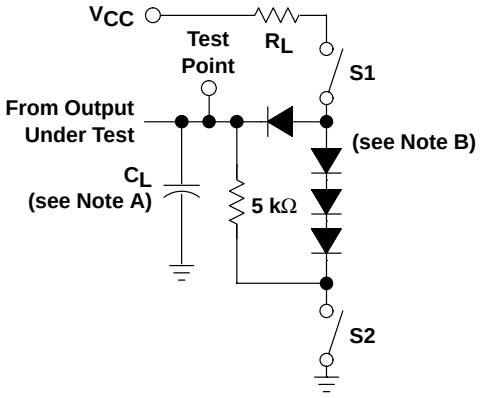
PARAMETER MEASUREMENT INFORMATION



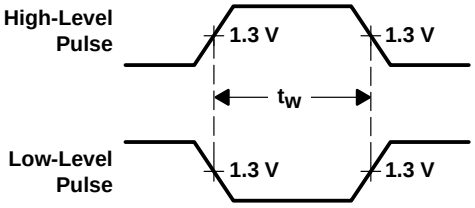
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



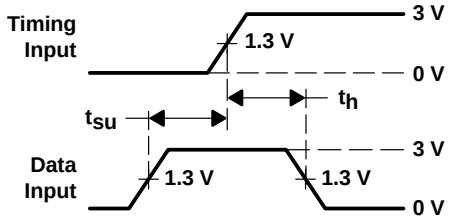
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



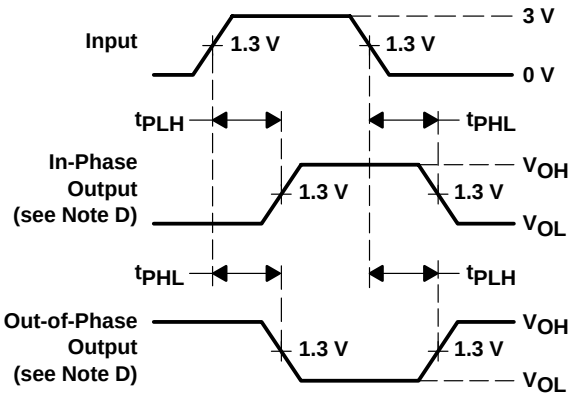
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



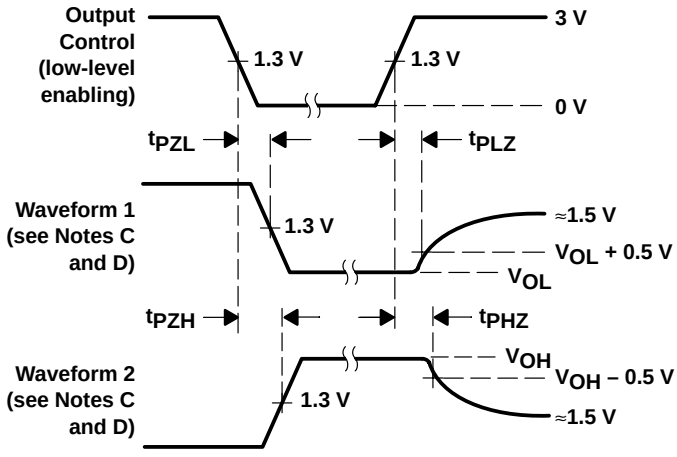
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

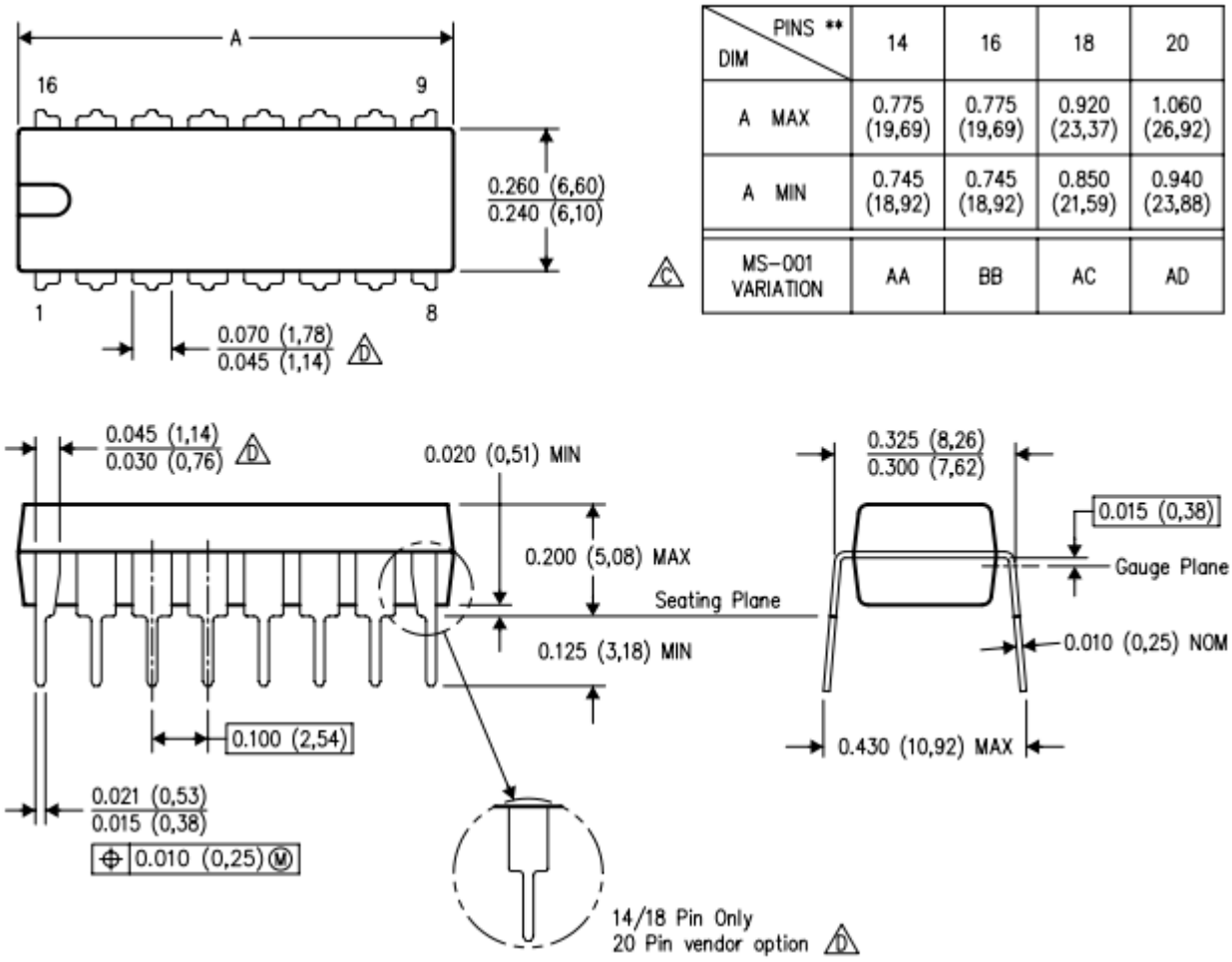


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

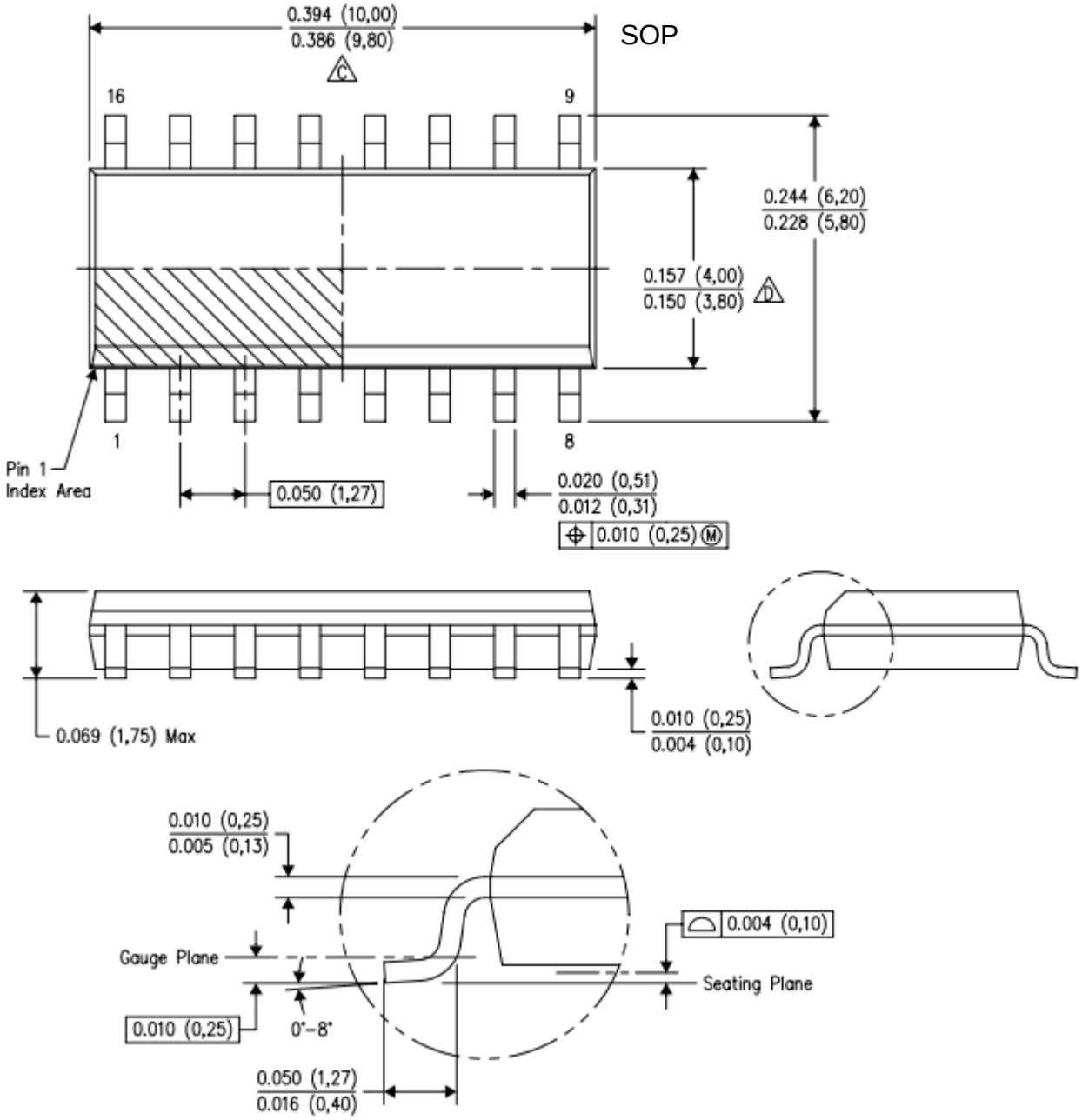
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD


SOP
0.394 (10,00)
0.386 (9,80)
C
16
9
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
1
8
Pin 1
Index Area
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
0.004 (0,10)
Gauge Plane
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

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