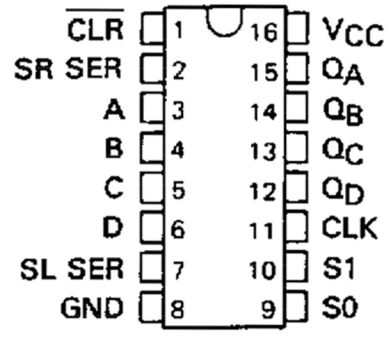
- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
74LS194	36 MHz	75 mW

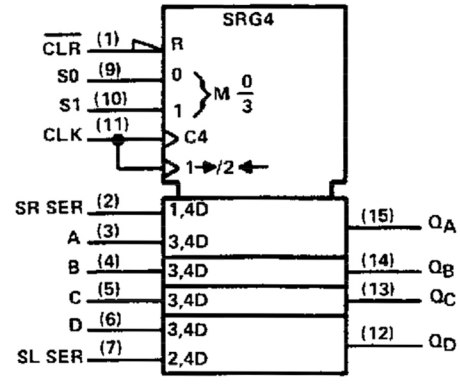
XD74LS194
(TOP VIEW)



description

Thasa bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want ina shift register. TM circuit contain* 46 equivalent gates and features paraMI inputs, parallel outputs, right-shift and left-shift serial inputs, operMino-mode-control inputs, and a direct overriding clear line. The rtgister has four distinct modes of operation, namely:
Inhibit clock (do nothing)
Shift right (in the direction Qa toward Qd)
Shift left On the direction Qq toward Qa)
Parallol (broadside) load
Synchronoua parallel loading Is accomplished by applying the four bits of data and taking both mode control inputs, SO and SI, high. The 4ata are loaded into the associated fnp*flops and appear at the outputs after ttw positivn transition of the clock input. During loading, sorial data flow is inhibited.
Shift right is accomplished synchronouBly with the rising edge of th® clock pulse when SO is high and S1 Is low. Serial data for this modB is entered at the shift-right data input. When SO la low and $1 is high, data shifts left synchronously and now data ic entered at the shift-left serial input. Clocking of the shift register 询 inhibited when both mode control inputs are low. The mode controls of the XD74LS194 should be changed only whHe the clock input le high.

logic symbol†



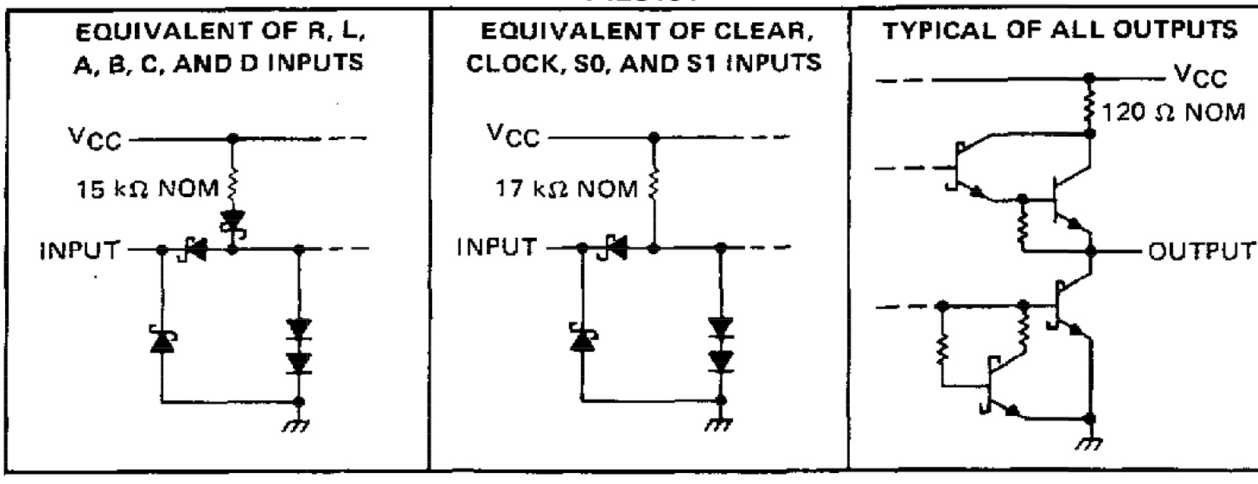
FUNCTION TABLE

INPUTS									OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL						
	S1	S0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

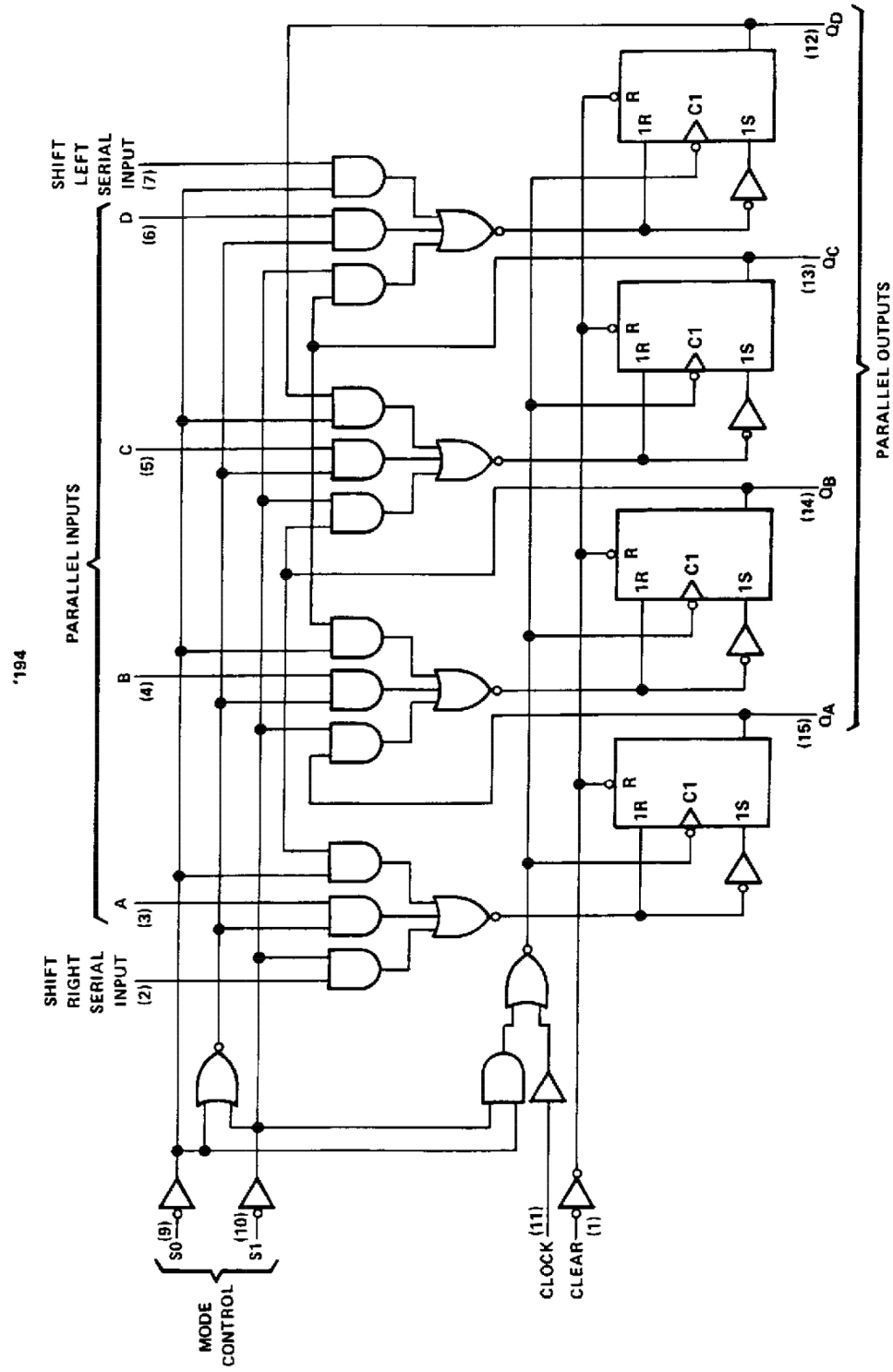
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, incuding tean-sitions)
↑ = transition from low to high level
a,b,c,d = the level of steady-state input at input A,B,C,orD,respectively.
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = the level of Q_A, Q_B, Q_C,or Q_D,respectively,before the indicated steady-state input conditions were established.
An, Bn, Cn, Dn = the level of A,, B, C, respectively, before the most-recent ↑ teansition of the clock.

schematics of inputs and outputs

74LS194

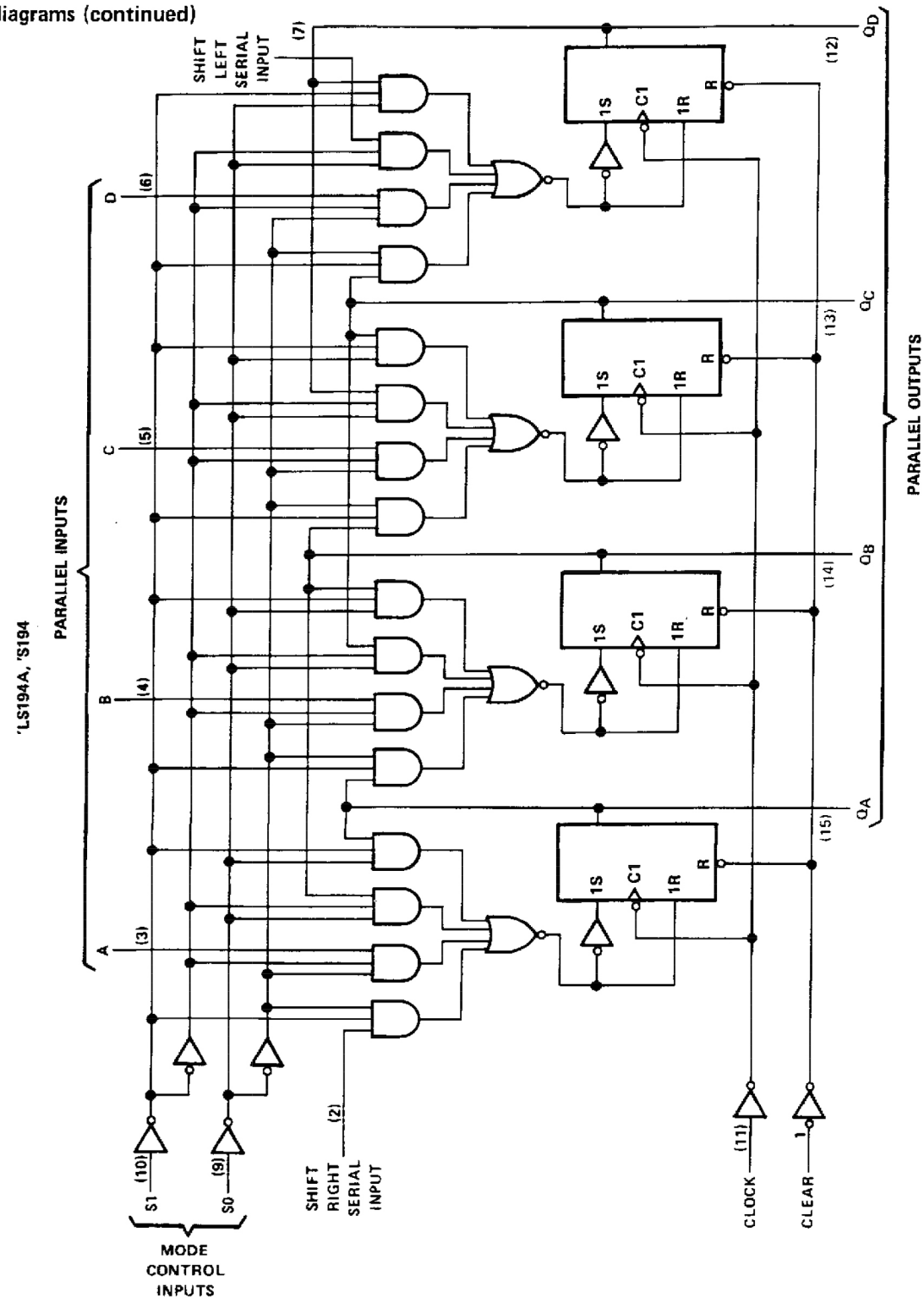


logic diagrams (positive logic)



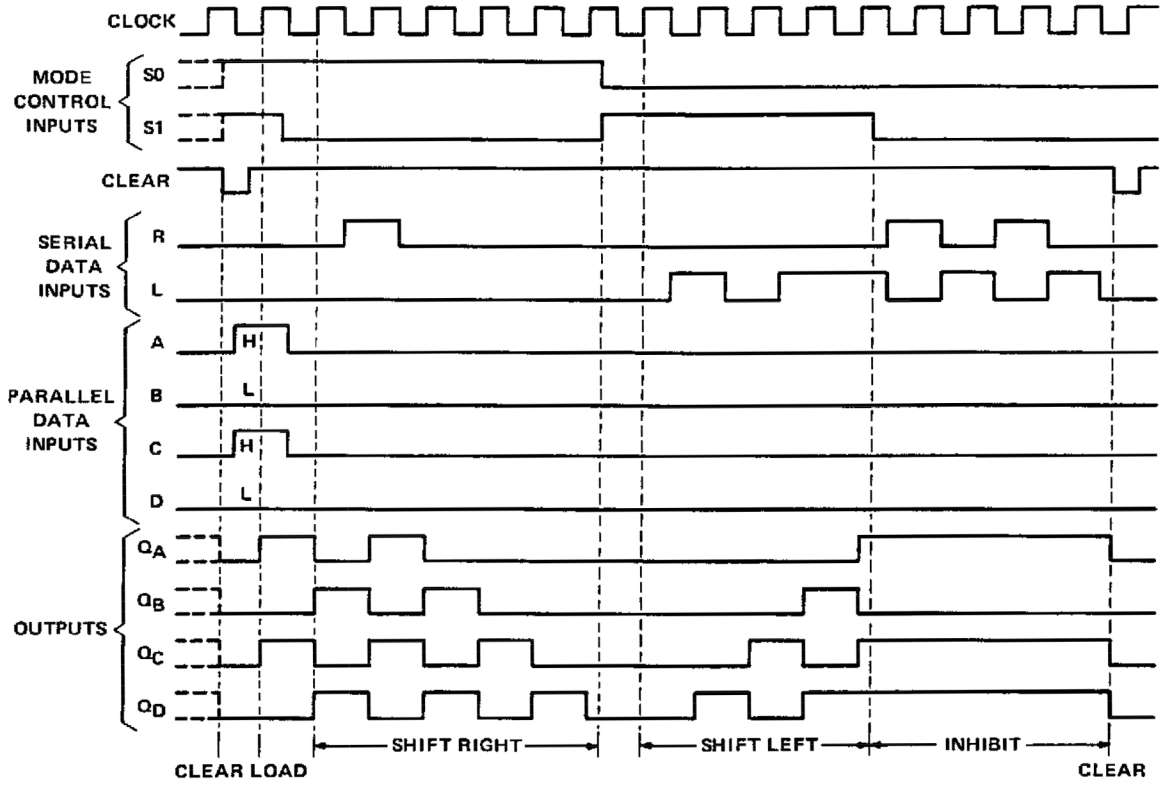
Pin numbers shown are for D, J, N, and W packages.

logic diagrams (continued)



Pin numbers shown on logic notation are for D, J or N, and W packages.

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: XD74LS194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		XD74LS164			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				8	mA
Clock frequency, f_{clock}		0		25	MHz
Width of clock or clear pulse, t_w		20			ns
Setup time, t_{su}	Mode control	30			ns
	Serial and parallel data	20			ns
	Clear inactive-state	25			ns
Hold time at any input, t_h		0			ns
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

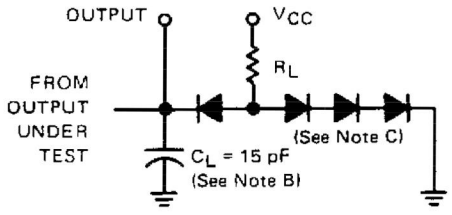
PARAMETER		TEST CONDITIONS†		XD74LS164			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4	V
			I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			15	23	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high level output from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low level output from clock			17	26	ns

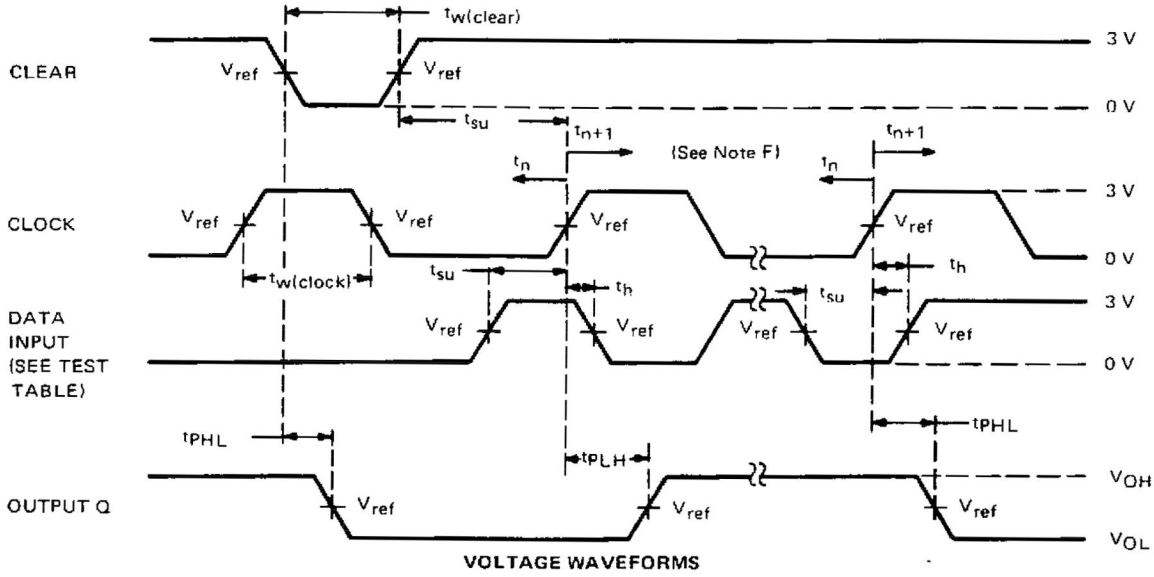
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

. TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}

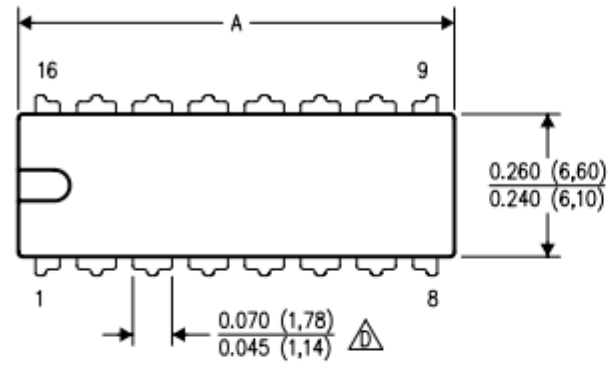


VOLTAGE WAVEFORMS

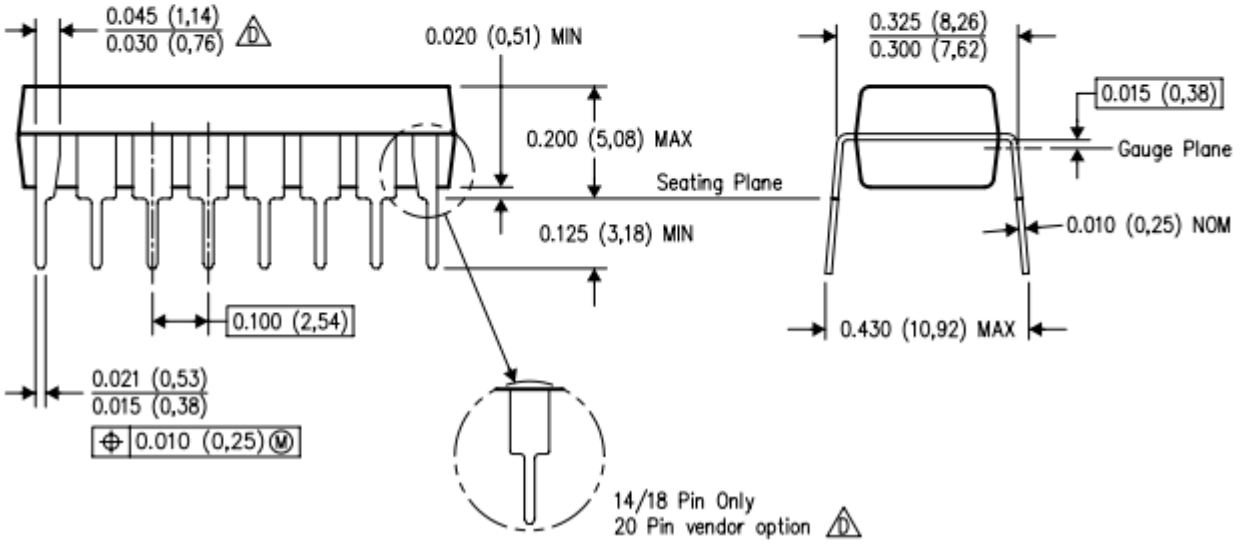
NOTES: A. The clock pulse generator has the following characteristics: Zout≈50Ω and PRR≤ 1 MHz. For 'XD74LS194. tp≤7ns and tp≤7 ns. For XD74LS194, < 15ns andtf≤6ns. For'XD74LS194. Ip≤2.5 ns and tf≤2.5 ns. When testing fmax. vary PRR.
B. CL includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916. .
D. A clear pulse is appied prior to each test.
E. For XD74LS194, Vref= 1.5 V:for XD74LS194. Vref- 1.3 V.
F. Propagation delay times (tPLH and tPHL are measured at in+1. Proper shiting of data s vernfied at tn+a wit a tunctional tost.
G. tn = bit time before clocking tr ansition.
tn+1 = bit time attor ono clock ing transition.
tn+4 = bit time atter four clocking transitions.

FIGURE 1–SWITCHING TIMES

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



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