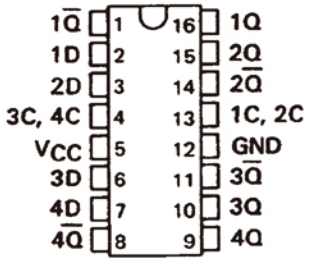
XD74LS75 0° C to 70° C.

FUNCTION TABLE
(each latch)

INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G



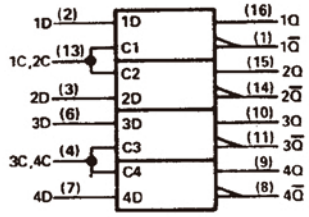
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

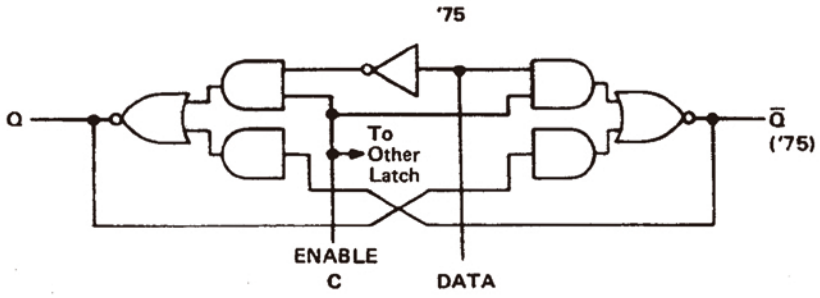
The '75 and 'LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications.

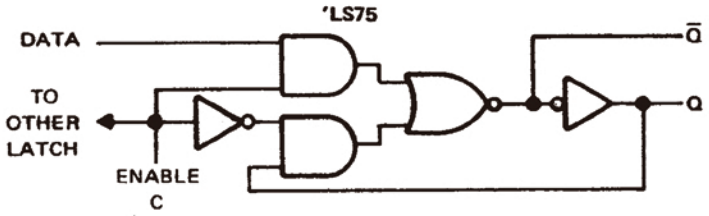
logic symbols†

'75, 'LS75



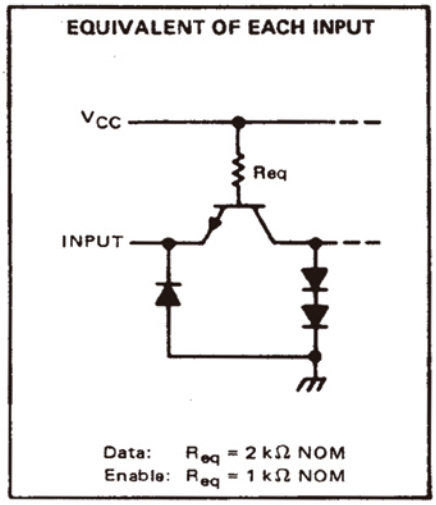
logic diagrams (each latch) (positive logic)



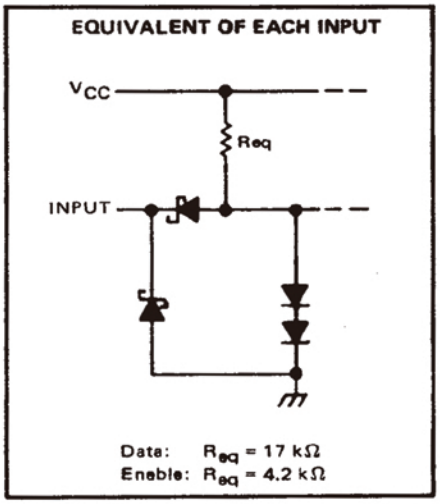


schematics of inputs and outputs

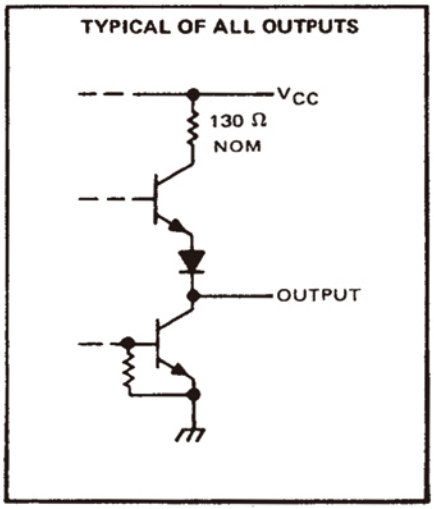
'75



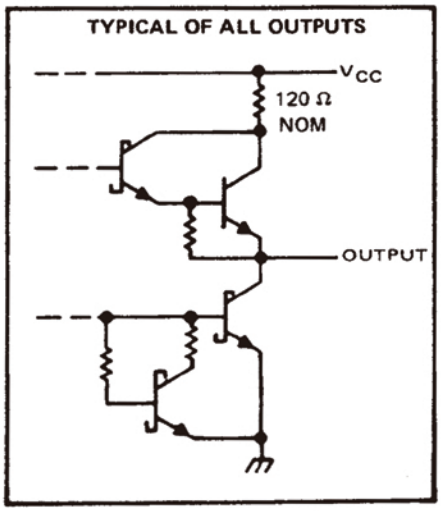
'LS75



'75



'LS75



recommended operating conditions

	XD74LS75			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Width of enabling pulse, t_w	20			ns
Setup time, t_{su}	20			ns
Hold time, t_h	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		C input					160	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		C input					−6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54′	−20		−57	mA
				SN74′	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54′		32	46	mA
				SN74′		32	53	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		16	30	ns
t_{PHL}					14	25	
t_{PLH}¶	D	$\overline{Q}$			24	40	ns
t_{PHL}¶					7	15	
t_{PLH}	C	Q			16	30	ns
t_{PHL}					7	15	
t_{PLH}¶	C	$\overline{Q}$			16	30	ns
t_{PHL}¶					7	15	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

recommended operating conditions

	XD74LS75			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Width of enabling pulse, t_w	20			ns
Setup time, t_{su}	20			ns
Hold time, t_h	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			XD74LS75			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4	V
				I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	D input			0.1	mA
				C input			0.4	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	D input			20	μA
				C input			80	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	D input			−0.4	mA
				C input			−1.6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	'LS75		6.3	12	mA
				'LS77				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

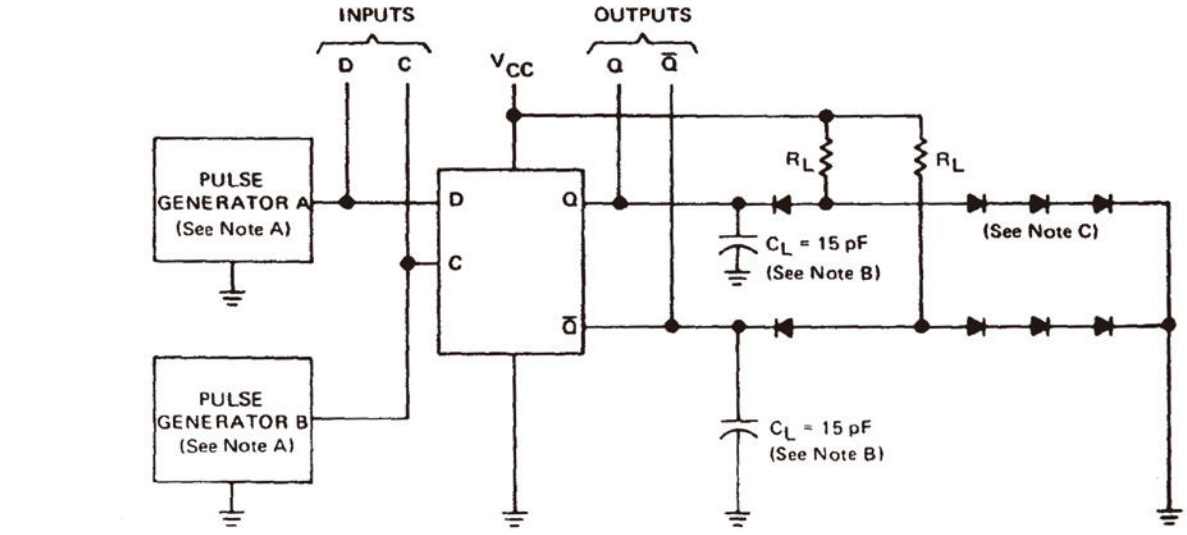
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			UNIT
				MIN	TYP	MAX	
t_{PLH}	D	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1		15	27	ns
t_{PHL}					9	17	
t_{PLH}	D	$\overline{Q}$			12	20	ns
t_{PHL}					7	15	
t_{PLH}	C	Q			15	27	ns
t_{PHL}					14	25	
t_{PLH}	C	$\overline{Q}$			16	30	ns
t_{PHL}					7	15	

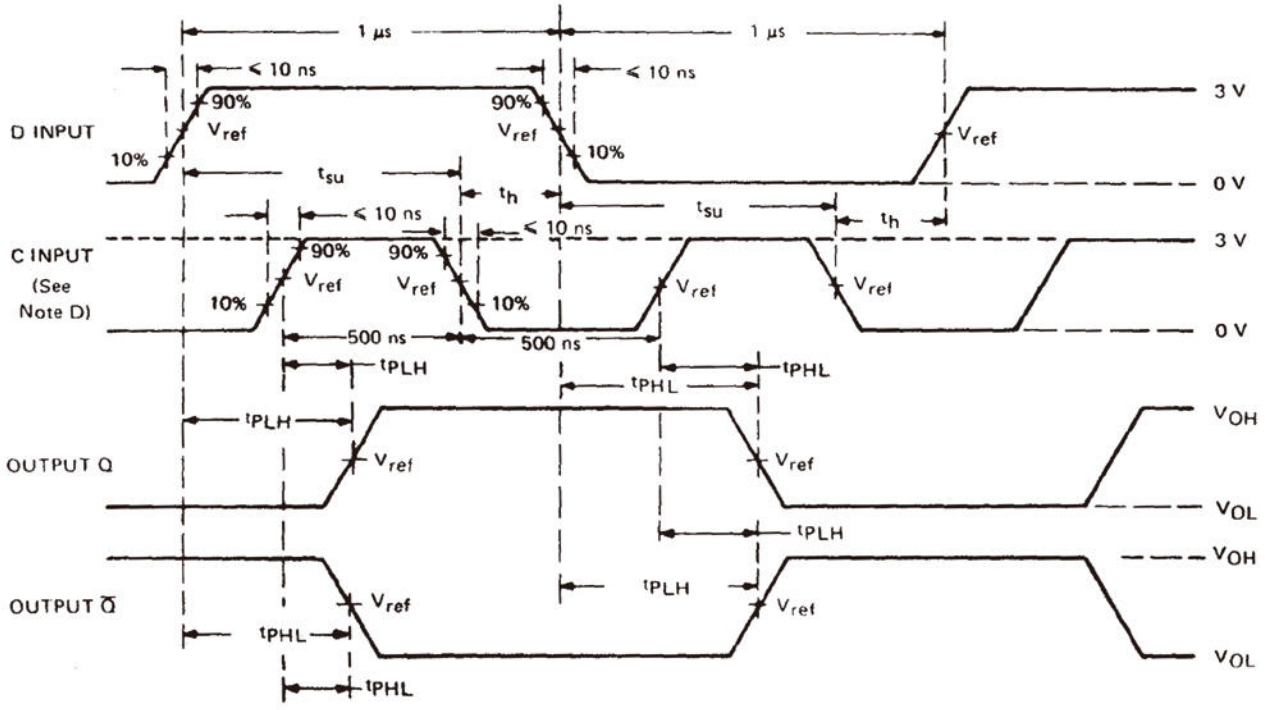
¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PLH} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



TEST CIRCUIT



VOLTAGE WAVEFORMS

†Complementary Q outputs are on the '75 and 'LS75 only.

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for pulse generator A, PRR ≤ 500 kHz; for pulse generator B, PRR ≤ 1 MHz. Positions of D and C input pulses are varied with respect to each other to verify setup times.

B. C_L includes probe and jig capacitance.

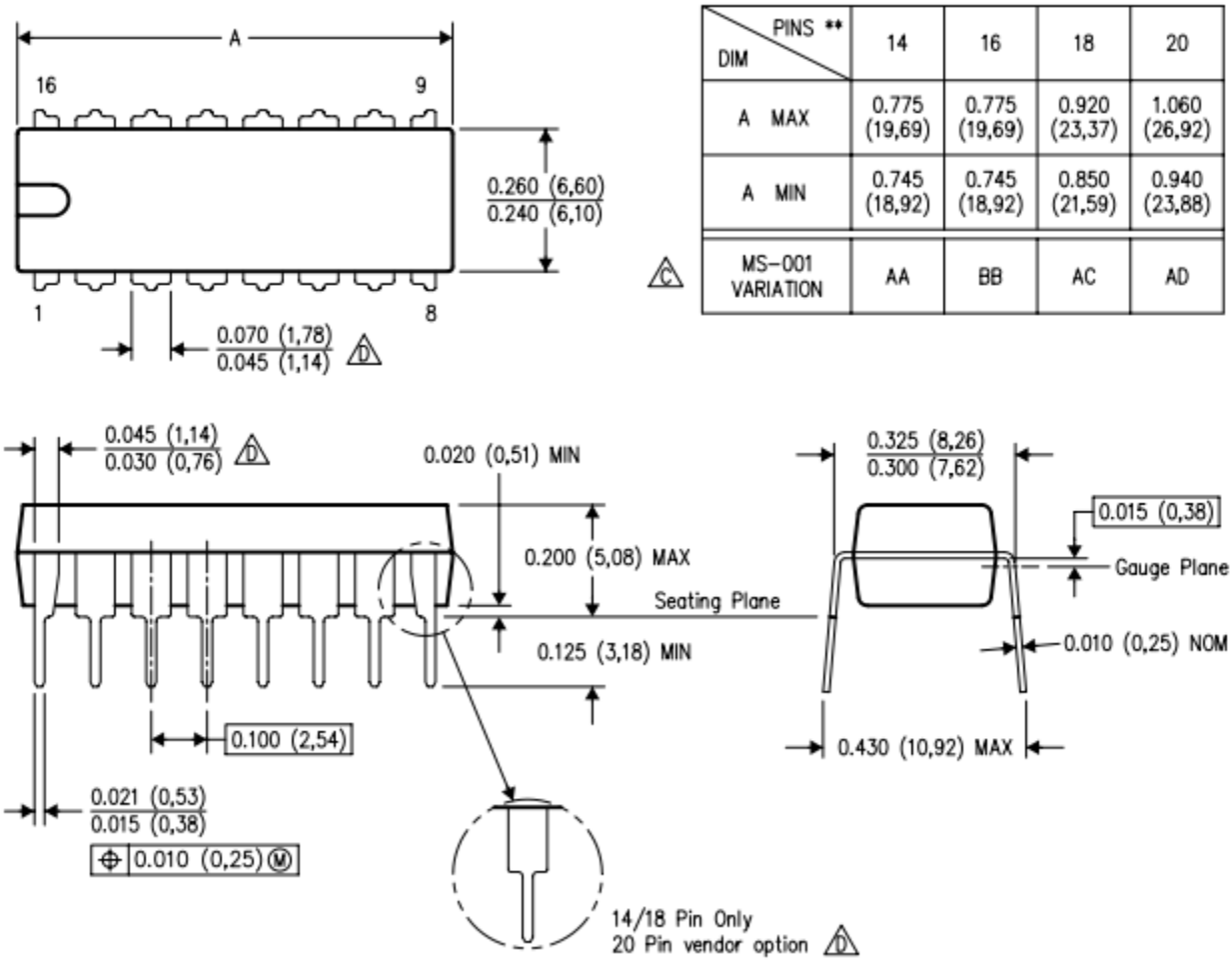
C. All diodes are 1N3064 or equivalent.

D. When measuring propagation delay times from the D input, the corresponding C input must be held high.

E. For '75, V_{ref} = 1.5 V; for 'LS75, V_{ref} = 1.3 V.

FIGURE 1

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

C

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA

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