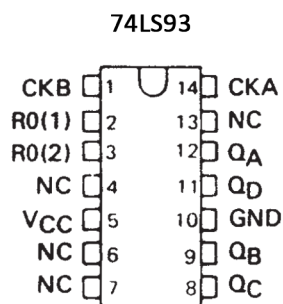
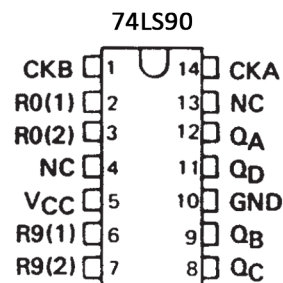


description

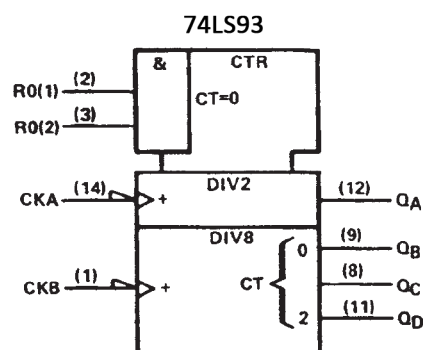
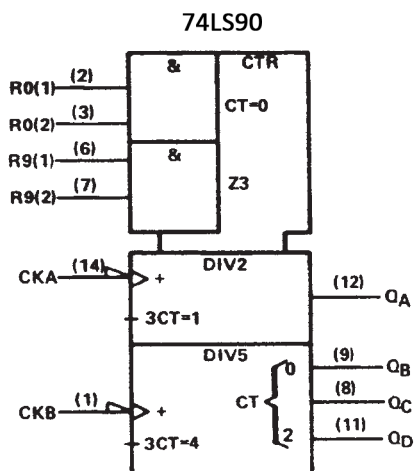
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 74LS90 divide-by-four and the divide-by-eight for the 74LS93

All of these counters have a gated zero reset and the 74LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Qa output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 74LS90 counters by connecting the Qd output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Qa.



logic symbols†



74LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

74LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

74LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

74LS93
COUNT SEQUENCE
(See Note C)

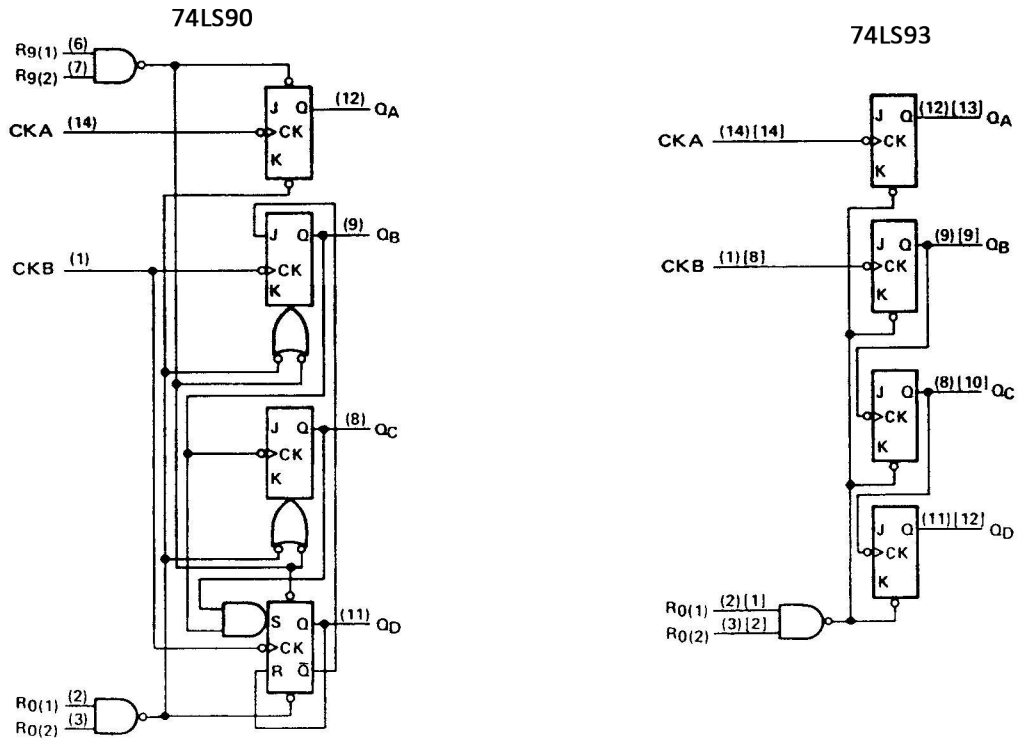
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

74LS93 74LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

- NOTES: A. Output Q_A is connected to input CKB for BCD count.
 B. Output Q_D is connected to input CKA for bi-quinary count.
 C. Output Q_A is connected to Input CKB.
 D. H = high level, L = low level, X = irrelevant

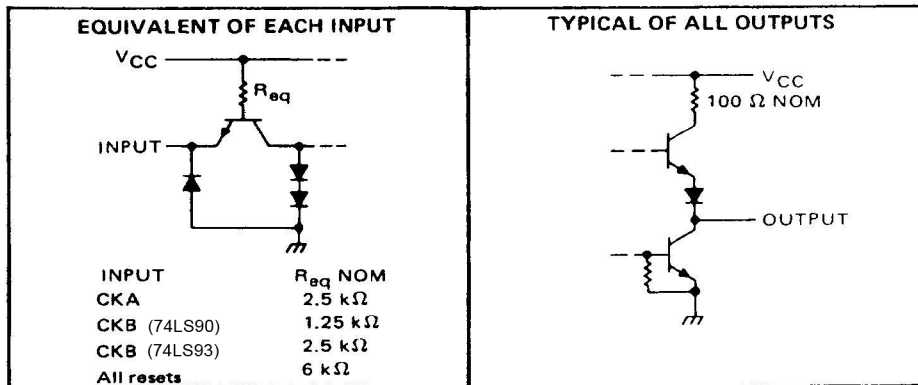
logic diagrams (positive logic)



In « J and K inputs » shown without connection or * for « Ur*r » c« only and are functionally at • high level.
Pin numbers shown in O are (or the 74LS93 and pin numbers shown in I] ar* for

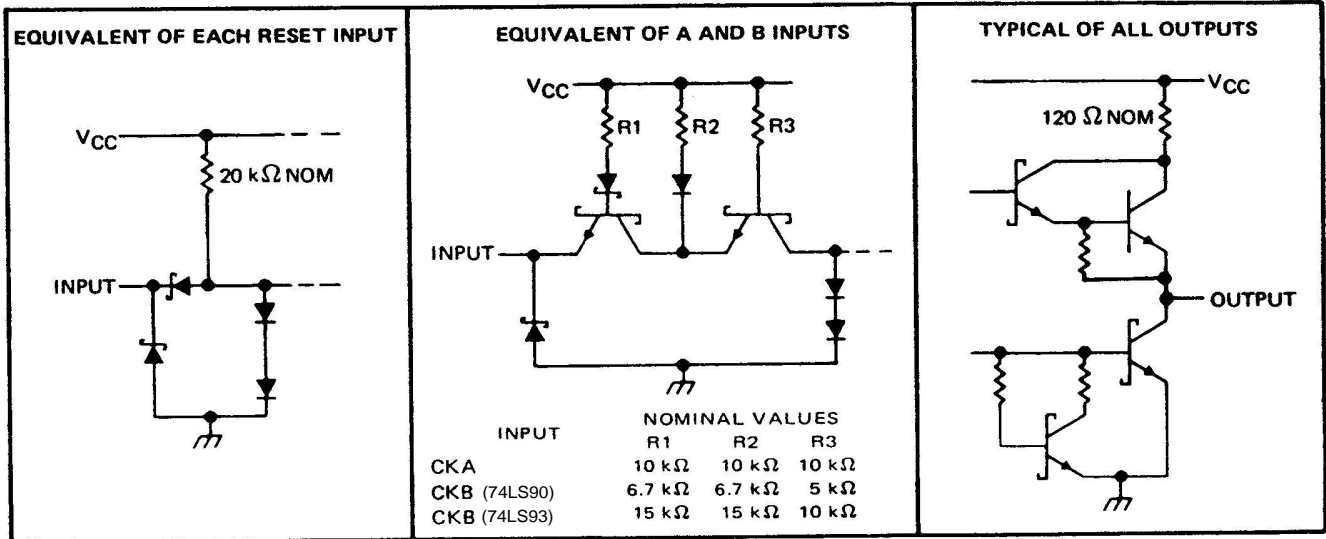
schematics of inputs and outputs

74LS90 74LS93



schematics of inputs and outputs (continued)

74LS90 74LS93



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: 74LS90 74LS93	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	74LS90 74LS93			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Count frequency, f_{count} (see Figure 1)	A input	0	32	MHz
	B input	0	16	
Pulse width, t_w	A input	15		ns
	B input	30		
	Reset inputs	30		
Reset inactive-state setup time, t_{su}	25			ns
Operating free-air temperature, T_A	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	74LS90 74LS93		UNIT
		MIN	TYP [‡] MAX	
V_{IH} High-level input voltage		2		V
V_{IL} Low-level input voltage			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.7	3.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}^{\S}$	0.25	0.4	V
		0.35	0.5	
I_I Input current at maximum input voltage	Any reset			mA
	CKA			
	CKB			
I_{IH} High-level input current	Any reset			20
	CKA			40
	CKB			80
I_{IL} Low-level input current	Any reset			-0.4
	CKA			-2.4
	CKB			-3.2
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3	'LS90		mA
		9	15	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[¶] Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	74LS93			UNIT
			MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max} , I _{OH} = -400 µA	2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OL} = 4 mA¶	0.25	0.4	V
			I _{OL} = 8 mA¶	0.35	0.5	
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V		0.1	mA
		CKA or CKB	V _{CC} = MAX, V _I = 5.5 V		0.2	
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V		20	µA
		CKA or CKB			80	
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V		-0.4	mA
		CKA			-2.4	
		CKB			-1.6	
I _{OS}	Short-circuit output current §	V _{CC} = MAX		-20	-100	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 3		9	15	mA

†For condition* shown as MIN or MAX. um th* appropriam v»lu« t pacified und«f fecomm«nd*I opewlno conditioni, (All typical values are at Vcc • B V. TA ■ 25°C.

§Not more than one output should be shorted at time, and duration of th* hort>clrcult should not exceed on* second. 1qa outputs «r» tested at specified IOL plu« th* limit value for 1|L tM CKB Input. Thi»p*mlt«drivinfl tM CKB gut **N«» maintain <ull fan-out capability.

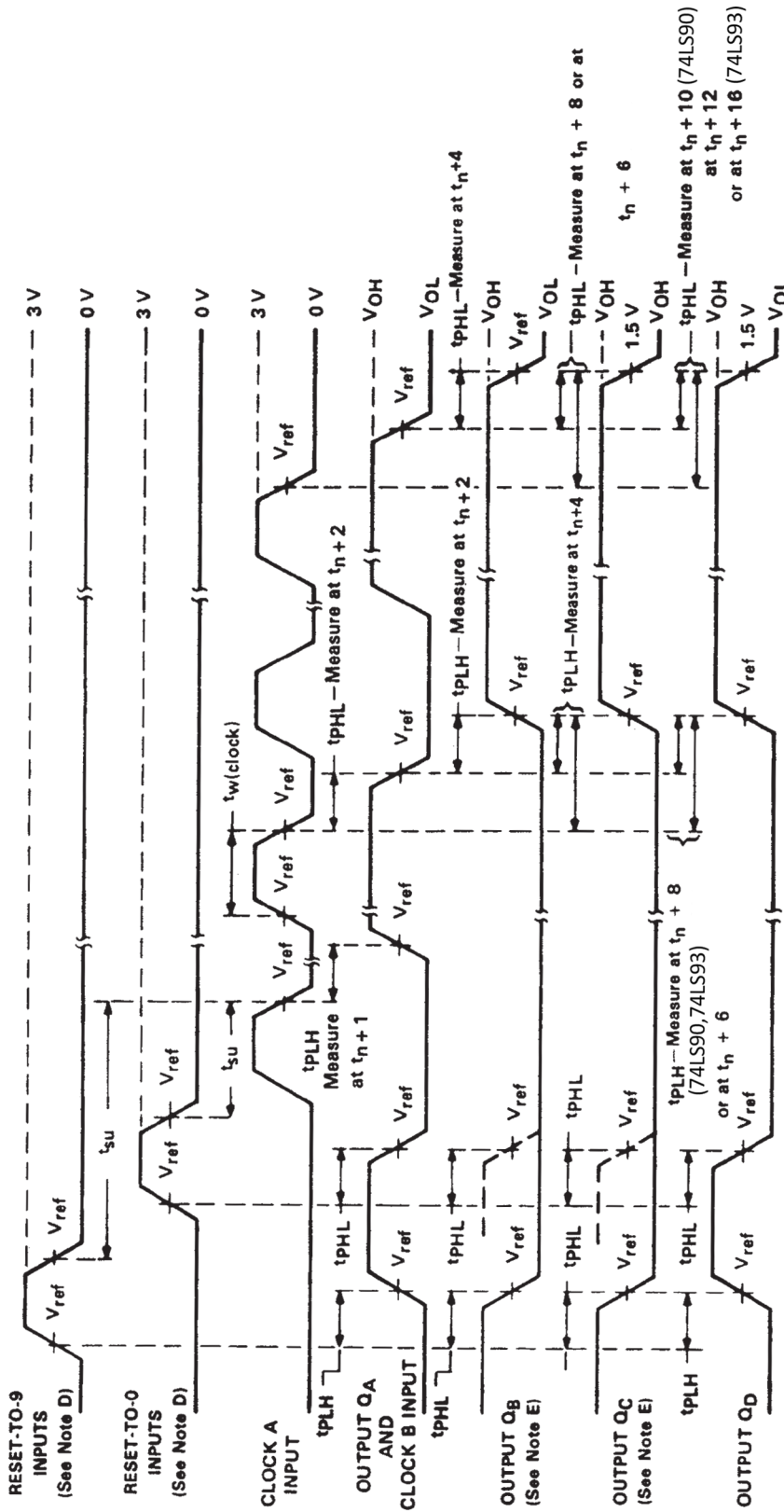
NOTE 3: Ice H m««wr«d whh «il output* op«n. both Rq inputs grounded following momentary confection to 4.5 V. and M other Inputs grounded.

switching characteristics, V_{CC} = 5 V, TA = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	74LS90			74LS93			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	CKA	Q _A	C _L = 15 pF, R _L = 2 kΩ See Figure 1	32	42		32	42	MHz	
	CKB	Q _B		16			16			
t _{PLH}	CKA	Q _A		10	16		10	16	ns	
t _{PHL}		12		18		12	18			
t _{PLH}	CKA	Q _D		32	48		46	70	ns	
t _{PHL}		34		50		46	70			
t _{PLH}	CKB	Q _B		10	16		10	16	ns	
t _{PHL}		14		21		14	21			
t _{PLH}	CKB	Q _C		21	32		21	32	ns	
t _{PHL}		23		35		23	35			
t _{PLH}	CKB	Q _D		21	32		34	51	ns	
t _{PHL}		23		35		34	51			
t _{PHL}	Set-to-0	Any		26	40		26	40	ns	
t _{PLH}	Set-to-9	Q _A , Q _D		20	30				ns	
t _{PHL}		Q _B , Q _C		26	40					

- #f_{max} = maximum count frequency
- t_{PLH} = propagation delay time, low-to-high-level output
- t_{PHL} = propagation delay time, high-to-low-level output

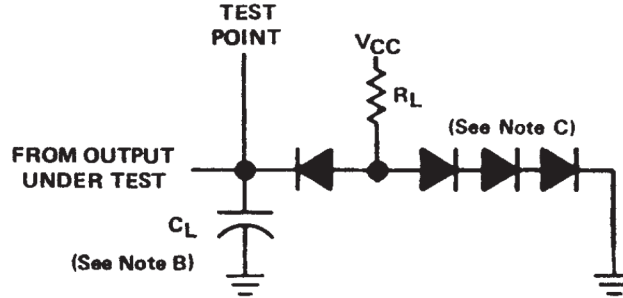
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
 $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
 for 74LS90,74LS93 $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.
 D. Each reset input is tested separately with the other reset at 4.5 V.
 E. Reference waveforms are shown with dashed lines.
 F. $V_{ref} = 1.5$ V. For 74LS90 and 74LS93 $V_{ref} = 1.3$ V.

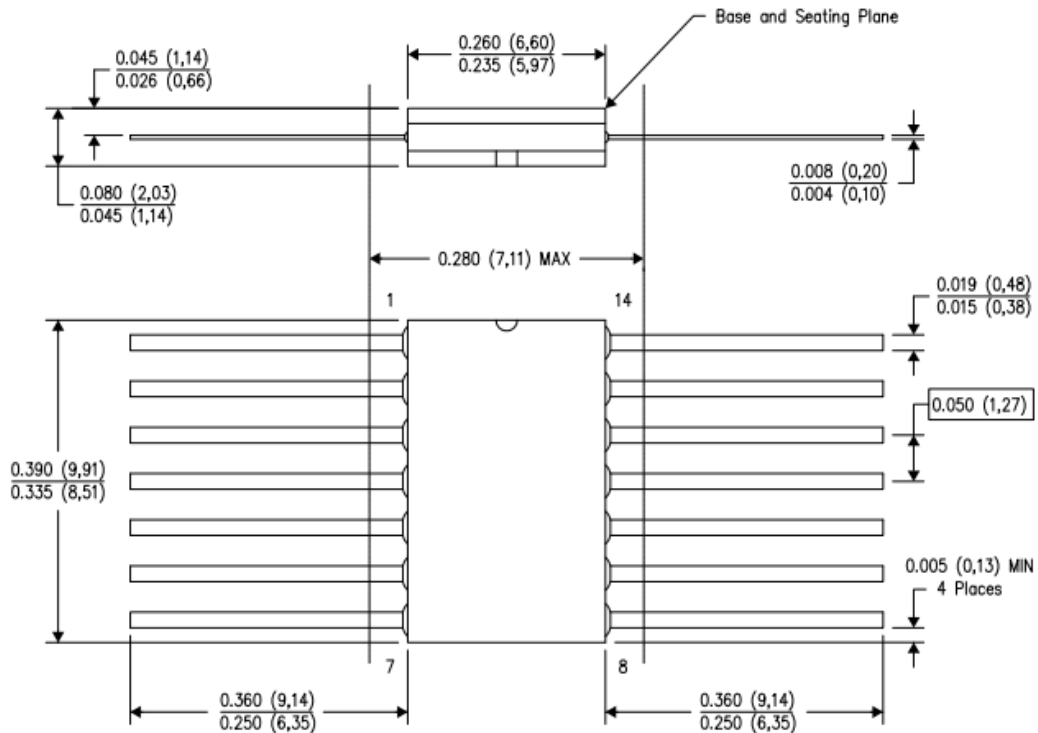
FIGURE 1A

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
 $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, duty cycle = 50%, $Z_{\text{out}} \approx 50 \text{ ohms}$;
 for 74LS90, 74LS93, $t_r \leq 15 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, duty cycle = 50%, $Z_{\text{out}} \approx 50 \text{ ohms}$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.
 D. Each reset input is tested separately with the other reset at 4.5 V.
 E. Reference waveforms are shown with dashed lines.
 F. $V_{\text{ref}} = 1.5 \text{ V}$. For 74LS90 and 74LS93; $V_{\text{ref}} = 1.3 \text{ V}$.



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