

Features

- Operating voltage: 2.5V~5.5V
- Minimal external components
- No external filter is required
- Low standby current (on power down mode)
- Excellent performance
- Tristate data output for MCU interface
- 3.58MHz crystal or ceramic resonator
- 1633Hz can be inhibited by the INH pin

General Description

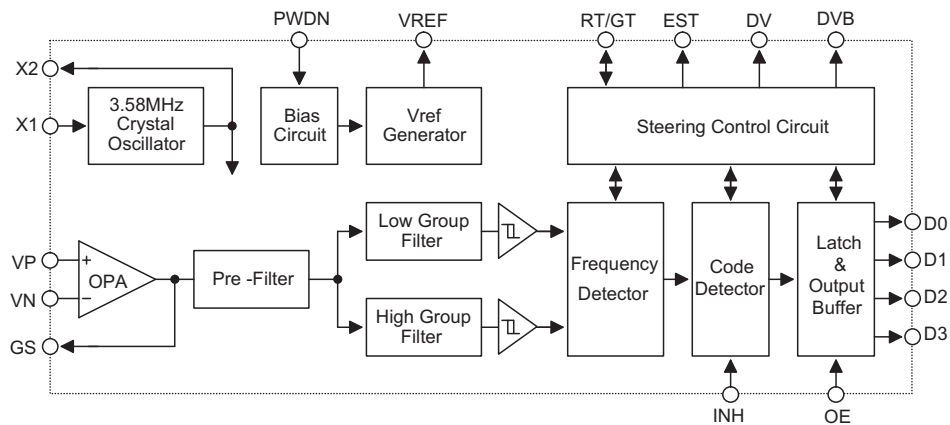
The XD/XL9170 are Dual Tone Multi Frequency (DTMF) receivers integrated with digital decoder and bandsplit filter functions as well as power-down mode and inhibit mode operations. Such devices use digital counting techniques to detect and decode all the 16 DTMF tone pairs into a 4-bit code output.

Highly accurate switched capacitor filters are implemented to divide tone signals into low and high group signals. A built-in dial tone rejection circuit is provided to eliminate the need for pre-filtering.

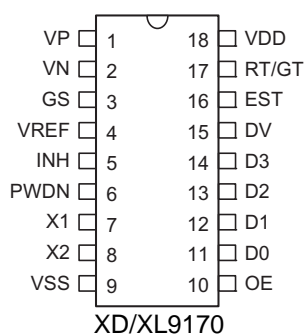
Ordering information

| Ordering Information | | | | | | | |
|----------------------|----------------|--------------|----------------|------------------|------|-----------------|------------------|
| part Number | Device Marking | Package type | Body size (mm) | Temperature (°C) | MSL | Transport Media | Package Quantity |
| XL9170 | XL9170 | SOP-18 | 11.45*7.5 | -20 to +75 | MSL3 | T&R | 1000 |
| XD9170 | XD9170 | DIP-18 | 22.90*6.50 | -20 to +75 | MSL3 | Tube 20 | 800 |

Block Diagram



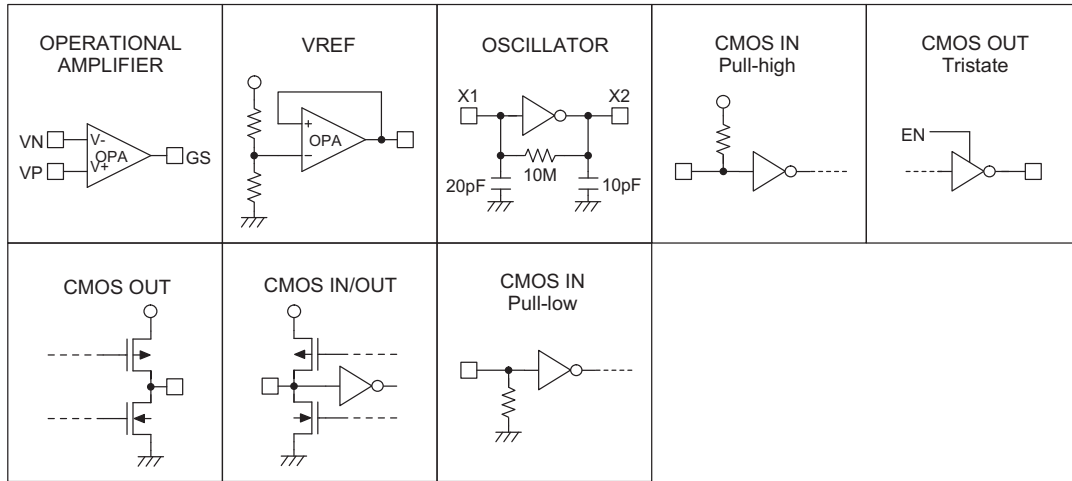
Pin Assignment



Pin Description

| Pin Name | I/O | Internal Connection | Description |
|----------|-----|-----------------------|--|
| VP | I | Operational Amplifier | Operational amplifier non-inverting input |
| VN | I | Operational Amplifier | Operational amplifier inverting input |
| GS | O | | Operational amplifier output terminal |
| VREF | O | VREF | Reference voltage output, normally $V_{DD}/2$ |
| X1 | I | oscillator | The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. A standard 3.579545MHz crystal connected to X1 and X2 terminals implements the oscillator function. |
| X2 | O | | |
| PWDN | I | CMOS IN Pull-low | Active high. This enables the device to go into power down mode and inhibits the oscillator. This pin input is internally pulled down. |
| INH | I | CMOS IN Pull-low | Logic high. This inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down. |
| VSS | — | — | Negative power supply, ground |
| OE | I | CMOS IN Pull-high | D0~D3 output enable, high active |
| D0~D3 | O | CMOS OUT Tristate | Receiving data output terminals OE="H": Output enable OE="L": High impedance |
| DV | O | CMOS OUT | Data valid output When the chip receives a valid tone (DTMF) signal, the DV goes high; otherwise it remains low. |
| EST | O | CMOS OUT | Early steering output (see Functional Description) |
| RT/GT | I/O | CMOS IN/OUT | Tone acquisition time and release time can be set through connection with external resistor and capacitor. |
| VDD | — | — | Positive power supply, 2.5V~5.5V for normal operation |

Approximate internal connection circuits



Absolute Maximum Ratings

| | | | |
|----------------------|--------------------------------|-----------------------------|----------------|
| Supply Voltage | -0.3V to 6V | Storage Temperature | -50°C to 125°C |
| Input Voltage | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature | -20°C to 75°C |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------|-----------------|--------------------------------------|--------|--------|--------|------|
| | | V _{DD} | Conditions | | | | |
| V _{DD} | Operating Voltage | — | — | 2.5 | 5 | 5.5 | V |
| I _{DD} | Operating Current | 5V | — | — | 3.0 | 7 | mA |
| I _{STB} | Standby Current | 5V | PWDN=5V | — | 10 | 25 | μA |
| V _{IL} | "Low" Input Voltage | 5V | — | — | — | 1.0 | V |
| V _{IH} | "High" Input Voltage | 5V | — | 4.0 | — | — | V |
| I _{IL} | "Low" Input Current | 5V | V _{VP} =V _{VN} =0V | — | — | 0.1 | μA |
| I _{IH} | "High" Input Current | 5V | V _{VP} =V _{VN} =5V | — | — | 0.1 | μA |
| R _{OE} | Pull-high Resistance (OE) | 5V | V _{OE} =0V | 60 | 100 | 150 | kΩ |
| R _{IN} | Input Impedance (VN, VP) | 5V | — | — | 10 | — | MΩ |
| I _{OH} | Source Current (D0~D3, EST, DV) | 5V | V _{OUT} =4.5V | -0.4 | -0.8 | — | mA |
| I _{OL} | Sink Current (D0~D3, EST, DV) | 5V | V _{OUT} =0.5V | 1.0 | 2.5 | — | mA |
| f _{OSC} | System Frequency | 5V | Crystal=3.5795MHz | 3.5759 | 3.5795 | 3.5831 | MHz |

A.C. Characteristics

f_{osc}=3.5795MHz, Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|-------------------------------|---------------------------------|-----------------|--|------|------|------|-----------------|
| | | V _{DD} | Conditions | | | | |
| DTMF Signal | | | | | | | |
| | Input Signal Level | 3V | | -36 | — | -6 | dBm |
| | | 5V | | -29 | — | 1 | |
| | Twist Accept Limit (Positive) | 5V | | — | 10 | — | dB |
| | Twist Accept Limit (Negative) | 5V | | — | 10 | — | dB |
| | Dial Tone Tolerance | 5V | | — | 18 | — | dB |
| | Noise Tolerance | 5V | | — | -12 | — | dB |
| | Third Tone Tolerance | 5V | | — | -16 | — | dB |
| | Frequency Deviation Acceptance | 5V | | — | — | ±1.5 | % |
| | Frequency Deviation Rejection | 5V | | ±3.5 | — | — | % |
| t _{PU} | Power Up Time (See Figure 4.) | 5V | | — | 30 | — | ms |
| Gain Setting Amplifier | | | | | | | |
| R _{IN} | Input Resistance | 5V | — | — | 10 | — | MΩ |
| I _{IN} | Input Leakage Current | 5V | V _{SS} <(V _{VP} ,V _{VN})<V _{DD} | — | 0.1 | — | μA |
| V _{OS} | Offset Voltage | 5V | — | — | ±25 | — | mV |
| P _{SRR} | Power Supply Rejection | 5V | 100 Hz -3V<V _{IN} <3V | — | 60 | — | dB |
| C _{MRR} | Common Mode Rejection | 5V | | — | 60 | — | dB |
| A _{VO} | Open Loop Gain | 5V | | — | 65 | — | dB |
| f _T | Gain Band Width | 5V | — | — | 1.5 | — | MHz |
| V _{OUT} | Output Voltage Swing | 5V | R _L >100kΩ | — | 4.5 | — | V _{PP} |
| R _L | Load Resistance (GS) | 5V | — | — | 50 | — | kΩ |
| C _L | Load Capacitance (GS) | 5V | — | — | 100 | — | pF |
| V _{CM} | Common Mode Range | 5V | No load | — | 3.0 | — | V _{PP} |
| Steering Control | | | | | | | |
| t _{DP} | Tone Present Detection Time | | | 5 | 16 | 22 | ms |
| t _{DA} | Tone Absent Detection Time | | | — | 4 | 8.5 | ms |
| t _{ACC} | Acceptable Tone Duration | | | — | — | 42 | ms |
| t _{REJ} | Rejected Tone Duration | | | 20 | — | — | ms |
| t _{IA} | Acceptable Inter-digit Pause | | | — | — | 42 | ms |
| t _{IR} | Rejected Inter-digit Pause | | | 20 | — | — | ms |
| t _{PDO} | Propagation Delay (RT/GT to DO) | | | — | 8 | 11 | μs |
| t _{PDV} | Propagation Delay (RT/GT to DV) | | | — | 12 | — | μs |
| t _{DOV} | Output Data Set Up (DO to DV) | | | — | 4.5 | — | μs |
| t _{DDO} | Disable Delay (OE to DO) | | | — | 300 | — | ns |
| t _{EDO} | Enable Delay (OE to DO) | | | — | 50 | 60 | ns |

Note: DO=D0~D3

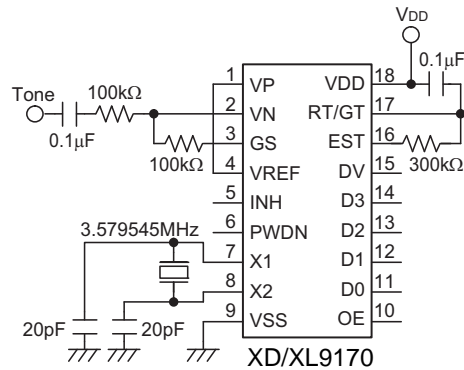


Figure 1. Test circuit

Functional Description

Overview

The XD/XL9170 tone decoders consist of three band pass filters and two digital decode circuits to convert a tone (DTMF) signal into digital code output.

An operational amplifier is built-in to adjust the input signal (refer to Figure 2).

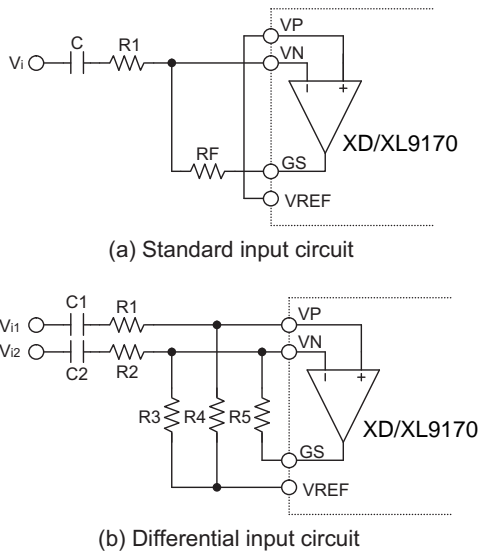


Figure 2. Input operation for amplifier application circuits

The pre-filter is a band rejection filter which reduces the dialing tone from 350Hz to 400Hz.

The low group filter filters low group frequency signal output whereas the high group filter filters high group frequency signal output.

Each filter output is followed by a zero-crossing detector with hysteresis. When each signal amplitude at the output exceeds the specified level, it is transferred to full swing logic signal.

When input signals are recognized to be effective, DV becomes high, and the correct tone code (DTMF) digit is transferred.

Steering control circuit

The steering control circuit is used for measuring the effective signal duration and for protecting against drop out of valid signals. It employs the analog delay by external RC time-constant controlled by EST.

The timing is shown in Figure 3. The EST pin is normally low and draws the RT/GT pin to keep low through discharge of external RC. When a valid tone input is detected, EST goes high to charge RT/GT through RC.

When the voltage of RT/GT changes from 0 to V_{TRT} (2.35V for 5V supply), the input signal is effective, and the correct code will be created by the code detector. After D0~D3 are completely latched, DV output becomes high. When the voltage of RT/GT falls down from VDD to V_{TRT} (i.e., when there is no input tone), DV output becomes low, and D0~D3 keeps data until a next valid tone input is produced.

By selecting adequate external RC value, the minimum acceptable input tone duration (t_{ACC}) and the minimum acceptable inter-tone rejection (t_{IR}) can be set. External components (R, C) are chosen by the formula (refer to Figure 5.):

$$t_{ACC} = t_{DP} + t_{GTP};$$

$$t_{IR} = t_{DA} + t_{GTA};$$

where t_{ACC} : Tone duration acceptable time
 t_{DP} : EST output delay time ("L"→"H")
 t_{GTP} : Tone present time
 t_{IR} : Inter-digit pause rejection time
 t_{DA} : EST output delay time ("H"→"L")
 t_{GTA} : Tone absent time

Timing Diagrams

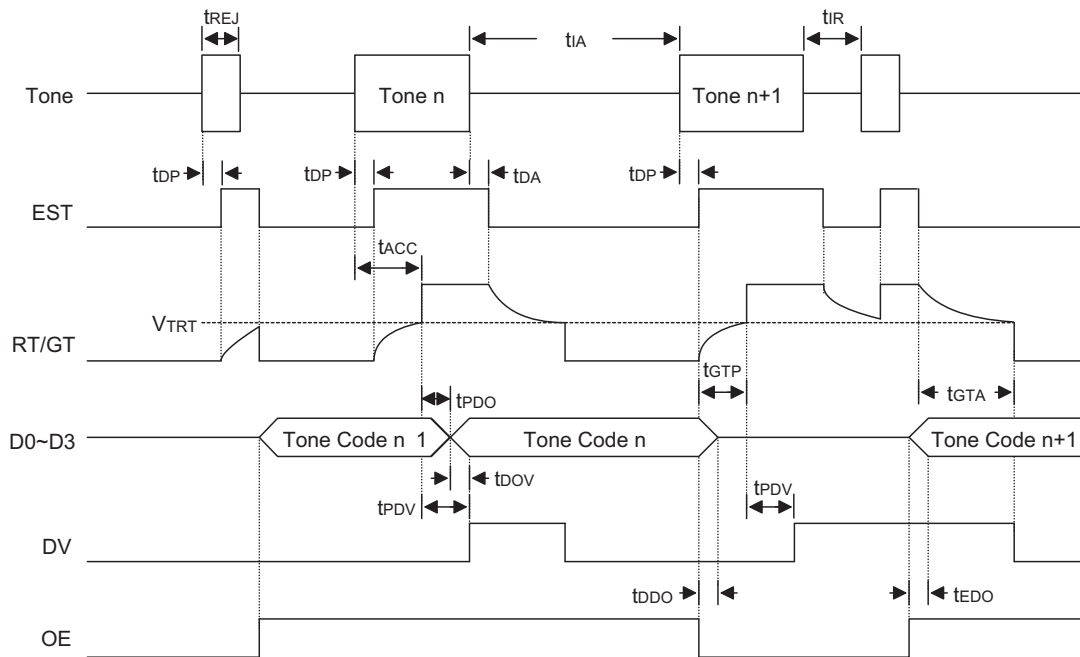


Figure 3. Steering timing

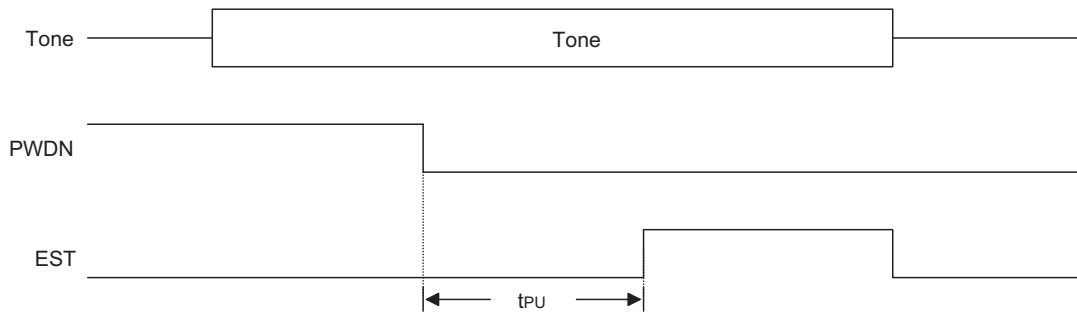
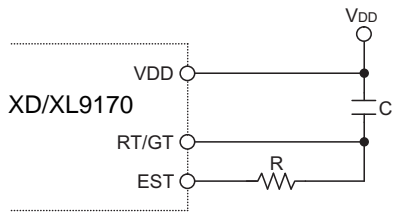


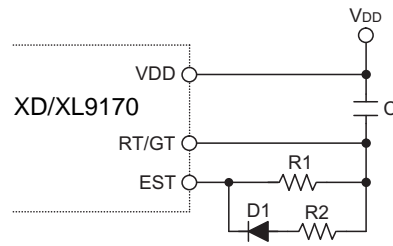
Figure 4. Power up timing



(a) Fundamental circuit:

$$t_{GTP} = R \times C \times \ln(V_{DD} / (V_{DD} - V_{TRT}))$$

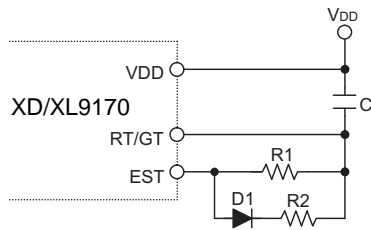
$$t_{GTA} = R \times C \times \ln(V_{DD} / V_{TRT})$$



(c) $t_{GTP} > t_{GTA}$:

$$t_{GTP} = R1 \times C \times \ln(V_{DD} / (V_{DD} - V_{TRT}))$$

$$t_{GTA} = (R1 // R2) \times C \times \ln(V_{DD} / V_{TRT})$$



(b) $t_{GTP} < t_{GTA}$:

$$t_{GTP} = (R1 // R2) \times C \times \ln(V_{DD} - V_{TRT})$$

$$t_{GTA} = R1 \times C \times \ln(V_{DD} / V_{TRT})$$

Figure 5. Steering time adjustment circuits

DTMF dialing matrix

| | COL1 | COL2 | COL3 | COL4 |
|------|------|------|------|------|
| ROW1 | 1 | 2 | 3 | A |
| ROW2 | 4 | 5 | 6 | B |
| ROW3 | 7 | 8 | 9 | C |
| ROW4 | * | 0 | # | D |

DTMF data output table

| Low Group (Hz) | High Group (Hz) | Digit | OE | D3 | D2 | D1 | D0 |
|----------------|-----------------|-------|----|----|----|----|----|
| 697 | 1209 | 1 | H | L | L | L | H |
| 697 | 1336 | 2 | H | L | L | H | L |
| 697 | 1477 | 3 | H | L | L | H | H |
| 770 | 1209 | 4 | H | L | H | L | L |
| 770 | 1336 | 5 | H | L | H | L | H |
| 770 | 1477 | 6 | H | L | H | H | L |
| 852 | 1209 | 7 | H | L | H | H | H |
| 852 | 1336 | 8 | H | H | L | L | L |
| 852 | 1477 | 9 | H | H | L | L | H |
| 941 | 1336 | 0 | H | H | L | H | L |
| 941 | 1209 | * | H | H | L | H | H |
| 941 | 1477 | # | H | H | H | L | L |
| 697 | 1633 | A | H | H | H | L | H |
| 770 | 1633 | B | H | H | H | H | L |
| 852 | 1633 | C | H | H | H | H | H |
| 941 | 1633 | D | H | L | L | L | L |
| — | — | ANY | L | Z | Z | Z | Z |

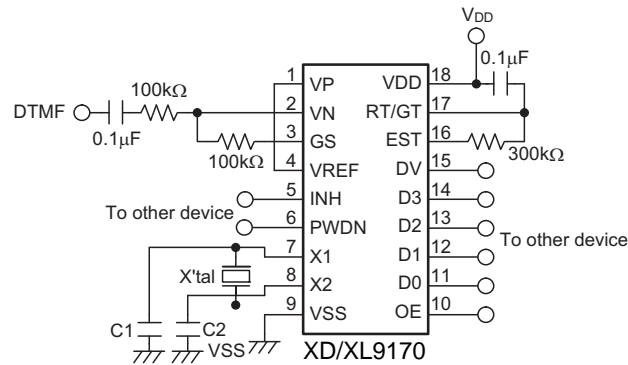
Note: "Z" High impedance; "ANY" Any digit

Data output

The data outputs (D0~D3) are tristate outputs. When OE input becomes low, the data outputs (D0~D3) are high impedance.

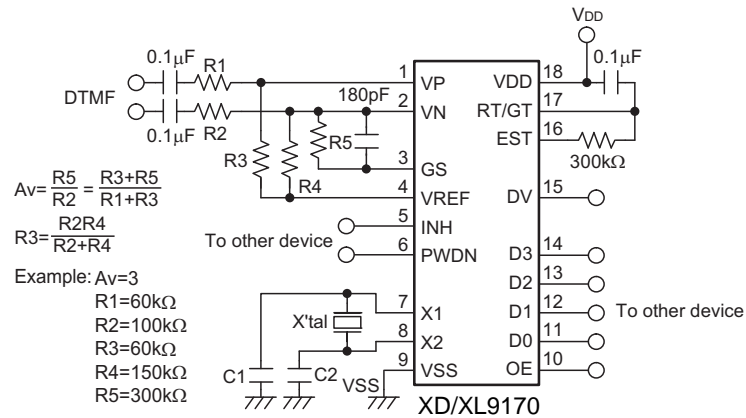
Application Circuits

Application Circuit 1



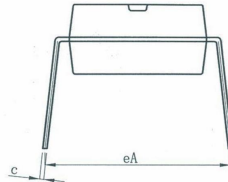
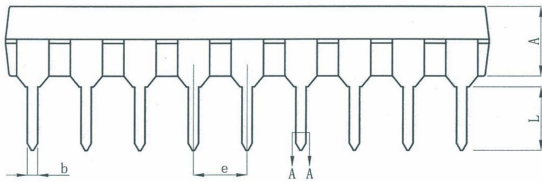
Note: X'tal = 3.579545MHz crystal
 C1 = C2 ≅ 20pF
 X'tal = 3.58MHz ceramic resonator
 C1 = C2 ≅ 39pF

Application Circuit 2

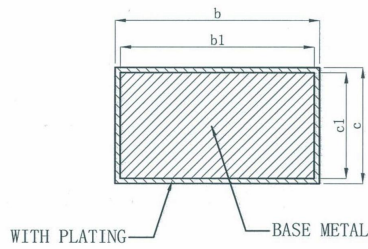
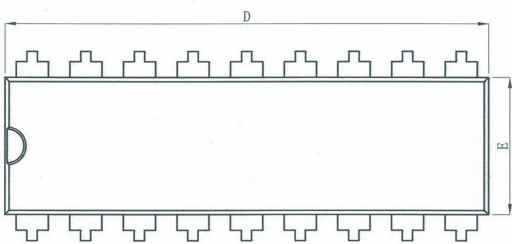


Note: X'tal = 3.579545MHz crystal
 C1 = C2 ≅ 20pF
 X'tal = 3.58MHz ceramic resonator
 C1 = C2 ≅ 39pF

DIP18封装尺寸图

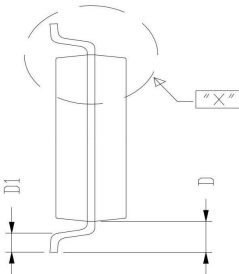
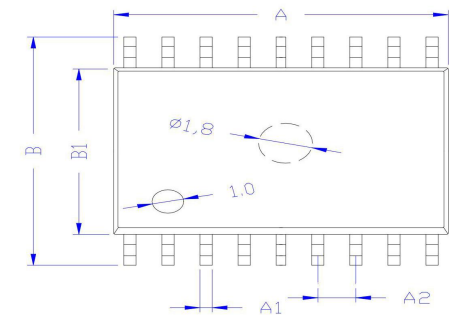


| symbol | millimeter | | |
|--------|------------|-------|-------|
| | Min | Nom | Max |
| A | 3.20 | 3.30 | 3.40 |
| b | 0.44 | — | 0.53 |
| b1 | 0.43 | 0.46 | 0.49 |
| c | 0.25 | — | 0.30 |
| c1 | 0.24 | 0.25 | 0.26 |
| D | 22.80 | 22.90 | 23.00 |
| E | 6.40 | 6.50 | 6.60 |
| e | 2.54BSC | | |
| eA | 8.30 | 8.80 | 9.30 |
| L | 3.00 | — | — |

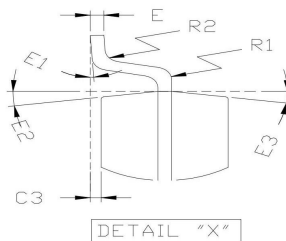
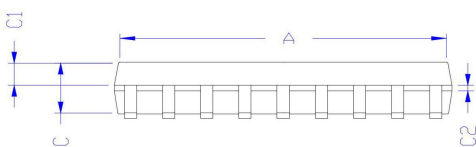


SECTION A-A

SOP18封装尺寸图



| SYMBOL | 表示 | MIN | NOM | MAX |
|--------|------|----------|-------|-------|
| A | 总长 | 11.25 | 11.45 | 11.65 |
| A1 | 脚宽 | 0.40TYP | | |
| A2 | 脚间距 | 1.27 TYP | | |
| B | 跨度 | 10.10 | 10.30 | 10.50 |
| B1 | 胶体宽度 | 7.30 | 7.50 | 7.70 |
| C | 胶体厚度 | 2.24 | 2.34 | 2.44 |
| C1 | 上胶体厚 | 1.05TYP | | |
| C2 | | 0.20 | 0.26 | 0.33 |
| C3 | 站高 | 0.10 | 0.15 | 0.25 |
| D | 单边长 | 1.30 | 1.40 | 1.50 |
| D1 | 脚长 | 0.70 | 0.80 | 1.00 |
| E | 脚厚 | 0.20 | 0.25 | 0.30 |
| E1 | 脚角度 | 0° | 4° | 8° |
| E2 | | 7° TYP | | |
| E3 | | 5° TYP | | |
| R1 | | | | |
| R2 | | | | |



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