

XD07 DIP-8 / XL07Z SOP-8

FEATURES

- Low V_{os} : 75 μV maximum
- Low V_{os} drift: 1.3 $\mu\text{V}/^\circ\text{C}$ maximum
- Ultrastable vs. time: 1.5 μV per month maximum
- Low noise: 0.6 μV p-p maximum
- Wide input voltage range: $\pm 14\text{ V}$ typical
- Wide supply voltage range: $\pm 3\text{ V}$ to $\pm 18\text{ V}$
- 125 $^\circ\text{C}$ temperature-tested dice

APPLICATIONS

- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls
 - Thermocouples
 - Resistor thermal detectors (RTDs)
 - Strain bridges
 - Shunt current measurements
- Precision filters

GENERAL DESCRIPTION

The XD07 has very low input offset voltage (75 μV maximum for XL07Z) that is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The XD07 also features low input bias current ($\pm 4\text{ nA}$ for the XL07Z) and high open-loop gain (200 V/mV for the XL07Z). The low offset and high open-loop gain make the XD07 particularly useful for high gain instrumentation applications.

PIN CONFIGURATION

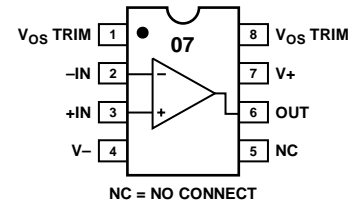
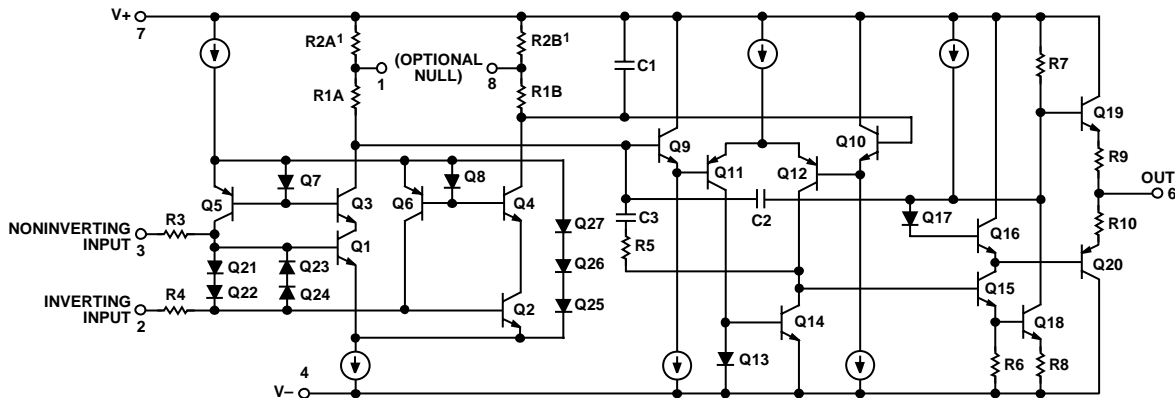


Figure 1.

The wide input voltage range of $\pm 13\text{ V}$ minimum combined with a high CMRR of 106 dB (XL07Z) and high input impedance provide high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the XD07, even at high gain, combined with the freedom from external nulling have made the XD07 an industry standard for instrumentation applications.

The XD07 is available in two standard performance grades. The XL07Z is specified for operation over the $0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ range, and the XD07Z is specified over the $-40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ temperature range.

The XD07 is available in epoxy 8-lead PDIP and 8-lead narrow SOIC packages. For CERDIP and TO-99 packages and standard microcircuit drawing (SMD) versions, see the XD07



¹ R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

Figure 2. Simplified Schematic

SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
$T_A = 25^\circ\text{C}$						
Input Offset Voltage ¹	V_{OS}			30	75	μV
Long-Term V_{OS} Stability ²	V_{OS}/Time			0.3	1.5	$\mu\text{V}/\text{Month}$
Input Offset Current	I_{OS}			0.5	3.8	nA
Input Bias Current	I_B			± 1.2	± 4.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz ³		0.35	0.6	μV p-p
Input Noise Voltage Density	e_n	$f_0 = 10\text{ Hz}$		10.3	18.0	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 100\text{ Hz}^3$		10.0	13.0	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 1\text{ kHz}$		9.6	11.0	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current	I_n p-p			14	30	pA p-p
Input Noise Current Density	I_n	$f_0 = 10\text{ Hz}$		0.32	0.80	$\text{pA}/\sqrt{\text{Hz}}$
		$f_0 = 100\text{ Hz}^3$		0.14	0.23	$\text{pA}/\sqrt{\text{Hz}}$
		$f_0 = 1\text{ kHz}$		0.12	0.17	$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance, Differential Mode ⁴	R_{IN}		15	50		$\text{M}\Omega$
Input Resistance, Common Mode	R_{INCM}			160		$\text{G}\Omega$
Input Voltage Range	IVR		± 13	± 14		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	106	123		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		5	20	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	200	500		V/mV
		$R_L \geq 500\ \Omega, V_O = \pm 0.5\text{ V}, V_S = \pm 3\text{ V}^4$	150	400		V/mV
$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$						
Input Offset Voltage ¹	V_{OS}			45	130	μV
Voltage Drift Without External Trim ⁴	TCV_{OS}			0.3	1.3	$\mu\text{V}/^\circ\text{C}$
Voltage Drift with External Trim ³	TCV_{OSN}	$R_P = 20\text{ k}\Omega$		0.3	1.3	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCI_{OS}			8	35	$\text{pA}/^\circ\text{C}$
Input Bias Current	I_B			± 1.5	± 5.5	nA
Input Bias Current Drift	TCI_B			13	35	$\text{pA}/^\circ\text{C}$
Input Voltage Range	IVR		± 13	± 13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	103	123		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		7	32	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	180	450		V/mV
OUTPUT CHARACTERISTICS						
$T_A = 25^\circ\text{C}$						
Output Voltage Swing	V_O	$R_L \geq 10\text{ k}\Omega$	± 12.5	± 13.0		V
		$R_L \geq 2\text{ k}\Omega$	± 12.0	± 12.8		V
		$R_L \geq 1\text{ k}\Omega$	± 10.5	± 12.0		V
$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$						
Output Voltage Swing	V_O	$R_L \geq 2\text{ k}\Omega$	± 12	± 12.6		V

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
T_A = 25°C						
Slew Rate	SR	R _L ≥ 2 kΩ ³	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A _{VOL} = 1 ⁵	0.4	0.6		MHz
Open-Loop Output Resistance	R _O	V _O = 0, I _O = 0		60		Ω
Power Consumption	P _d	V _S = ±15 V, No load		75	120	mW
		V _S = ±3 V, No load		4	6	mW
Offset Adjustment Range		R _P = 20 kΩ		±4		mV

¹ Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

² Long-term input offset voltage stability refers to the averaged trend time of V_{OS} vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.

³ Sample tested.

⁴ Guaranteed by design.

⁵ Guaranteed but not tested.

OP07C ELECTRICAL CHARACTERISTICS

V_S = ±15 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
T_A = 25°C						
Input Offset Voltage ¹	V _{OS}			60	150	μV
Long-Term V _{OS} Stability ²	V _{OS} /Time			0.4	2.0	μV/Month
Input Offset Current	I _{OS}			0.8	6.0	nA
Input Bias Current	I _B			±1.8	±7.0	nA
Input Noise Voltage	e _n p-p	0.1 Hz to 10 Hz ³		0.38	0.65	μV p-p
Input Noise Voltage Density	e _n	f _O = 10 Hz		10.5	20.0	nV/√Hz
		f _O = 100 Hz ³		10.2	13.5	nV/√Hz
		f _O = 1 kHz		9.8	11.5	nV/√Hz
Input Noise Current	I _n p-p			15	35	pA p-p
Input Noise Current Density	I _n	f _O = 10 Hz		0.35	0.90	pA/√Hz
		f _O = 100 Hz ³		0.15	0.27	pA/√Hz
		f _O = 1 kHz		0.13	0.18	pA/√Hz
Input Resistance, Differential Mode ⁴	R _{IN}		8	33		MΩ
Input Resistance, Common Mode	R _{INCM}			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13 V	100	120		dB
Power Supply Rejection Ratio	PSRR	V _S = ±3 V to ±18 V		7	32	μV/V
Large Signal Voltage Gain	A _{VO}	R _L ≥ 2 kΩ, V _O = ±10 V	120	400		V/mV
		R _L ≥ 500 Ω, V _O = ±0.5 V, V _S = ±3 V ⁴	100	400		V/mV
-40°C ≤ T_A ≤ +85°C						
Input Offset Voltage ¹	V _{OS}			85	250	μV
Voltage Drift Without External Trim ⁴	TCV _{OS}			0.5	1.8	μV/°C
Voltage Drift with External Trim ³	TCV _{OSN}	R _P = 20 kΩ		0.4	1.6	μV/°C
Input Offset Current	I _{OS}			1.6	8.0	nA
Input Offset Current Drift	TCI _{OS}			12	50	pA/°C
Input Bias Current	I _B			±2.2	±9.0	nA
Input Bias Current Drift	TCI _B			18	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13 V	97	120		dB
Power Supply Rejection Ratio	PSRR	V _S = ±3 V to ±18 V		10	51	μV/V
Large Signal Voltage Gain	A _{VO}	R _L ≥ 2 kΩ, V _O = ±10 V	100	400		V/mV

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
T_A = 25°C						
Output Voltage Swing	V _O	R _L ≥ 10 kΩ	±12.0	±13.0		V
		R _L ≥ 2 kΩ	±11.5	±12.8		V
		R _L ≥ 1 kΩ		±12.0		V
-40°C ≤ T_A ≤ +85°C						
Output Voltage Swing	V _O	R _L ≥ 2 kΩ	±12	±12.6		V
DYNAMIC PERFORMANCE						
T_A = 25°C						
Slew Rate	SR	R _L ≥ 2 kΩ ³	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A _{VOL} = 1 ⁵	0.4	0.6		MHz
Open-Loop Output Resistance	R _O	V _O = 0, I _O = 0		60		Ω
Power Consumption	P _d	V _S = ±15 V, No load		80	150	mW
		V _S = ±3 V, No load		4	8	mW
Offset Adjustment Range		R _P = 20 kΩ		±4		mV

¹ Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

² Long-term input offset voltage stability refers to the averaged trend time of V_{OS} vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.

³ Sample tested.

⁴ Guaranteed by design.

⁵ Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage (V _s)	±22 V
Input Voltage ¹	±22 V
Differential Input Voltage	±30 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range S and P Packages	-65°C to +125°C
Operating Temperature Range XD07	0°C to 70°C
XL07Z	-40°C to +85°C
Junction Temperature	150°C
Lead Temperature, Soldering (60 sec)	300°C

¹For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC_N (S-Suffix)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

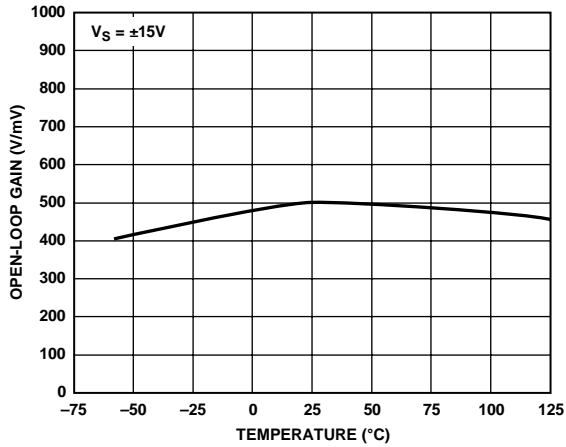


Figure 3. Open-Loop Gain vs. Temperature

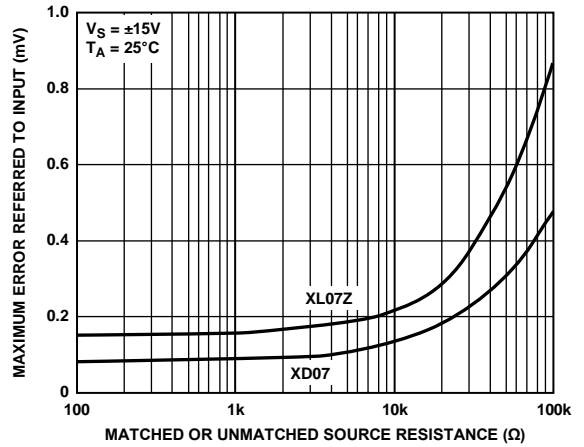


Figure 6. Maximum Error vs. Source Resistance

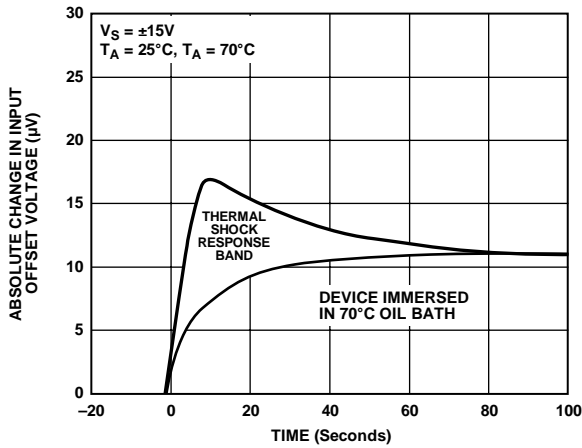


Figure 4. Offset Voltage Change due to Thermal Shock

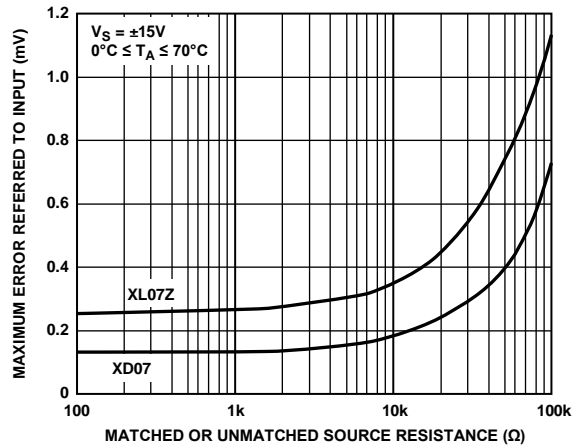


Figure 7. Maximum Error vs. Source Resistance

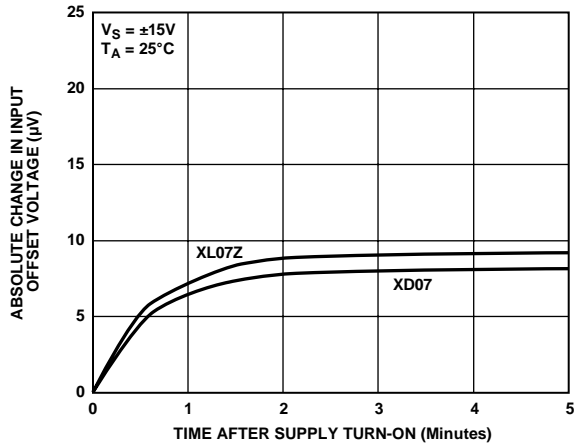


Figure 5. Warm-Up Drift

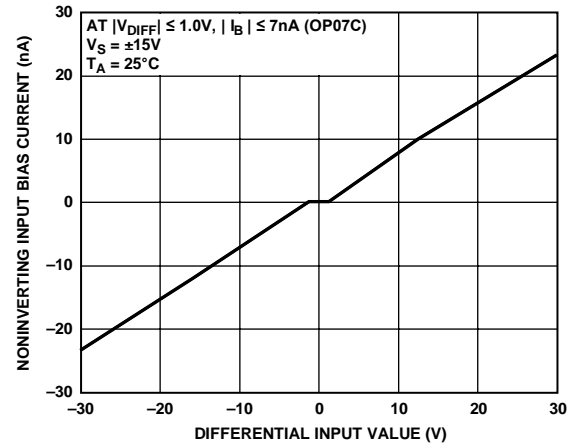


Figure 8. Input Bias Current vs. Differential Input Voltage

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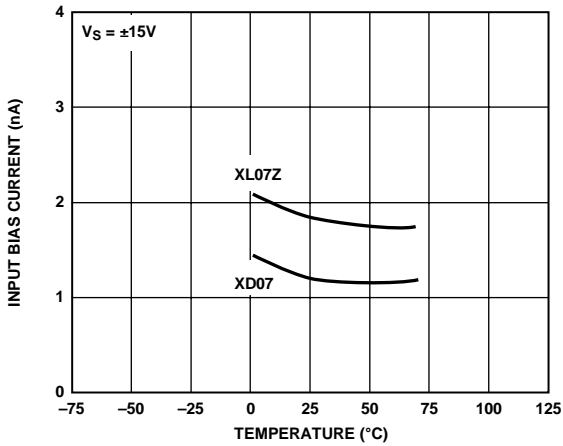


Figure 9. Input Bias Current vs. Temperature

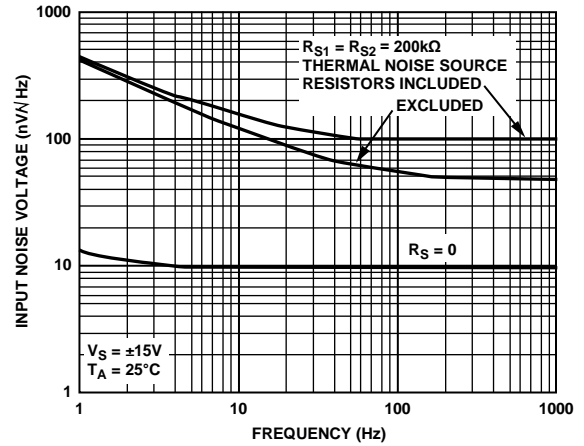


Figure 12. Total Input Noise Voltage vs. Frequency

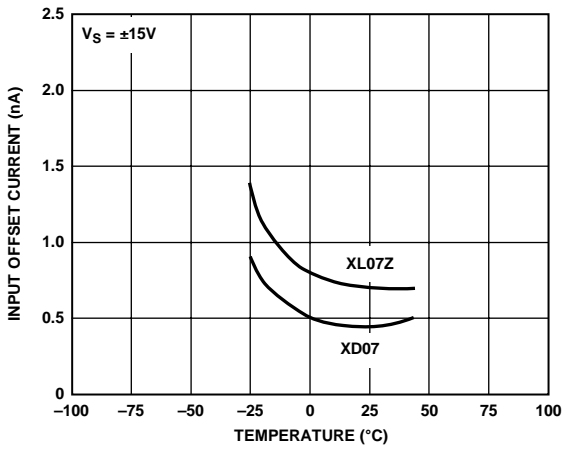


Figure 10. Input Offset Current vs. Temperature

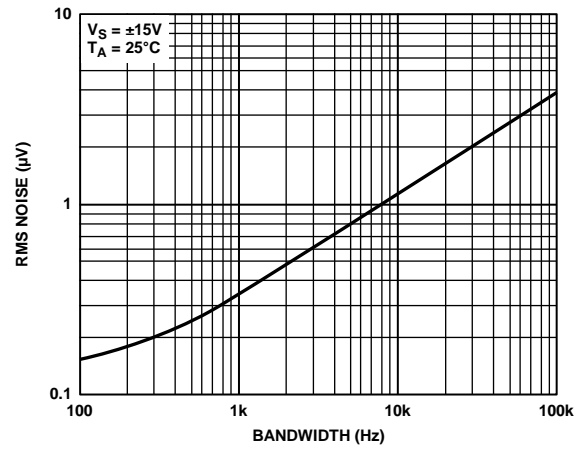


Figure 13. Input Wideband Noise vs. Bandwidth, 0.1 Hz to Frequency Indicated

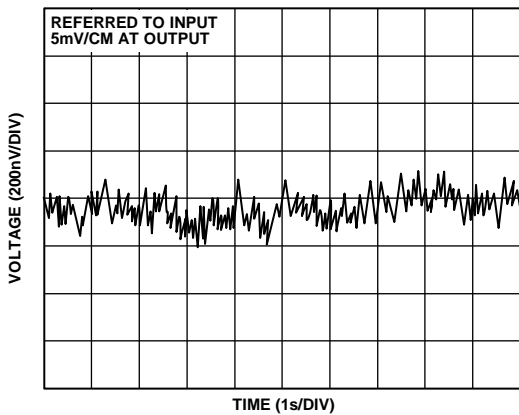


Figure 11. Low Frequency Noise

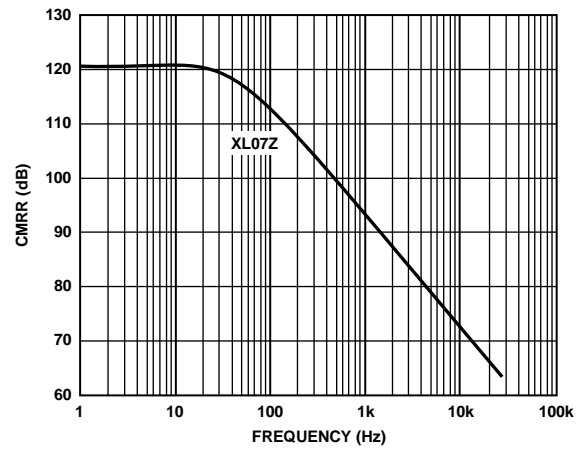


Figure 14. CMRR vs. Frequency

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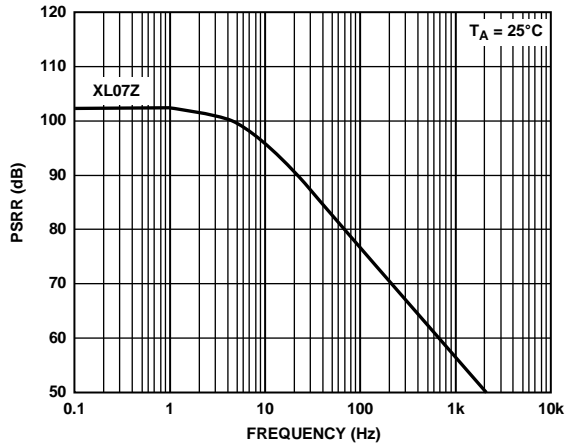


Figure 15. PSRR vs. Frequency

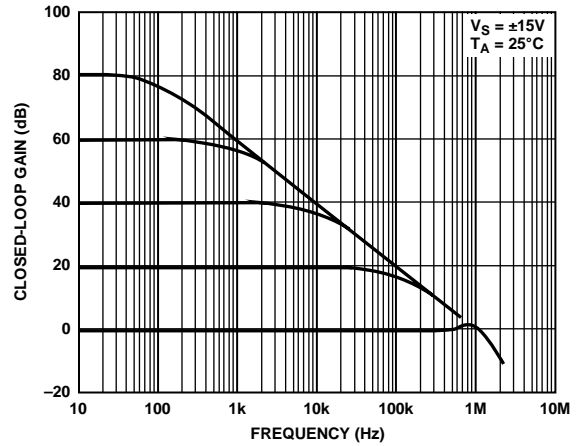


Figure 18. Closed-Loop Frequency Response for Various Gain Configurations

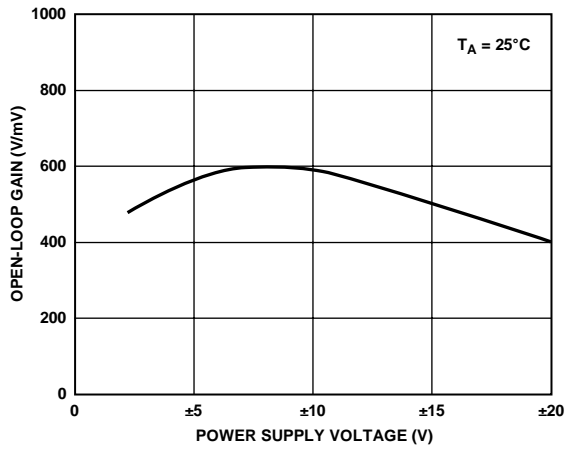


Figure 16. Open-Loop Gain vs. Power Supply Voltage

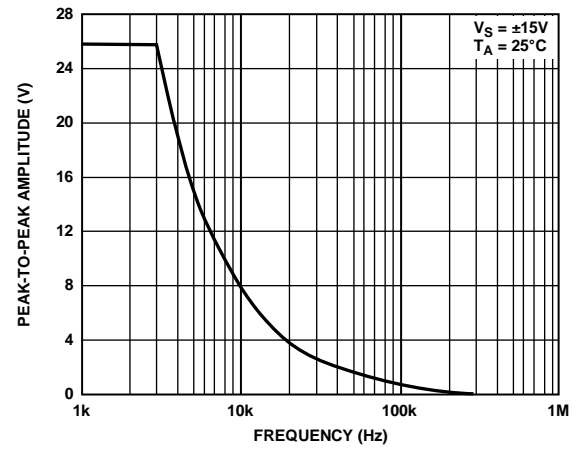


Figure 19. Maximum Output Swing vs. Frequency

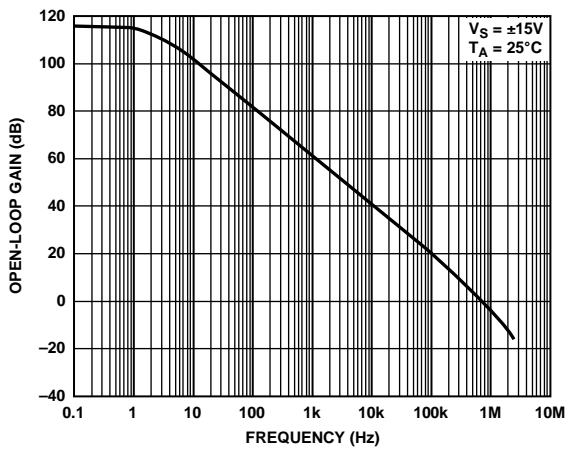


Figure 17. Open-Loop Frequency Response

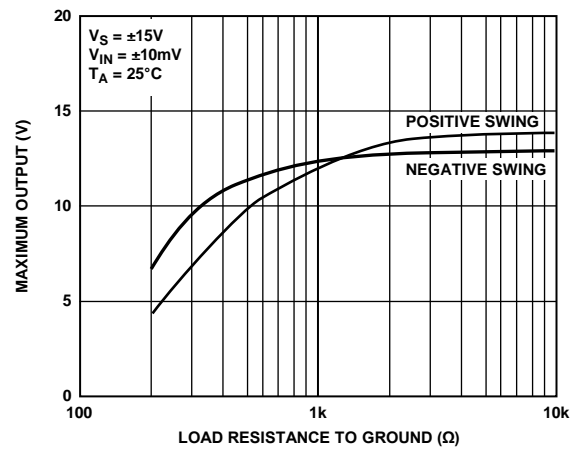


Figure 20. Maximum Output Voltage vs. Load Resistance

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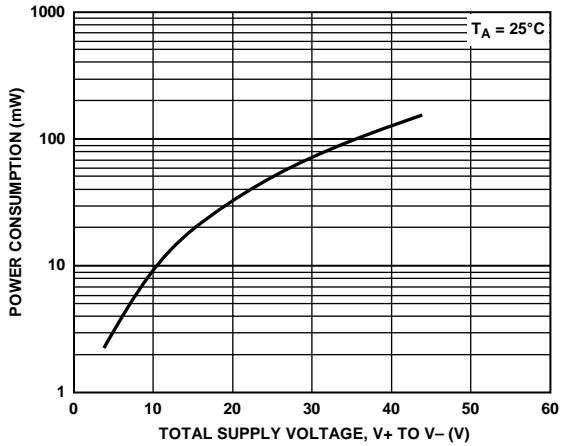


Figure 21. Power Consumption vs. Power Supply

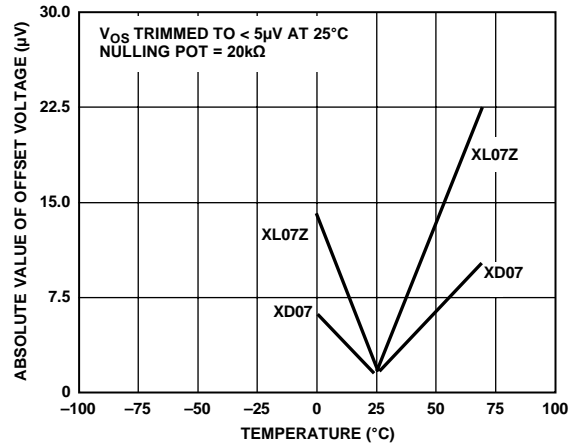


Figure 24. Trimmed Offset Voltage vs. Temperature

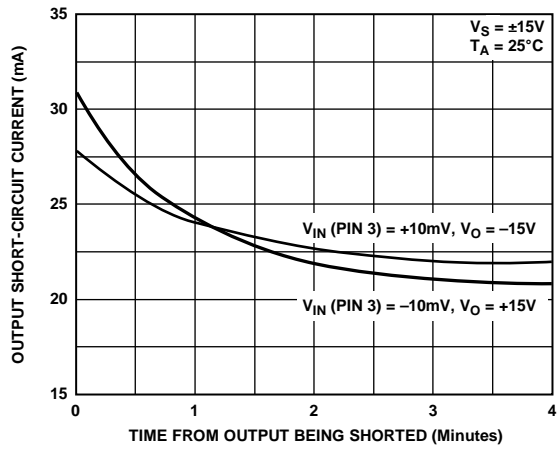


Figure 22. Output Short-Circuit Current vs. Time

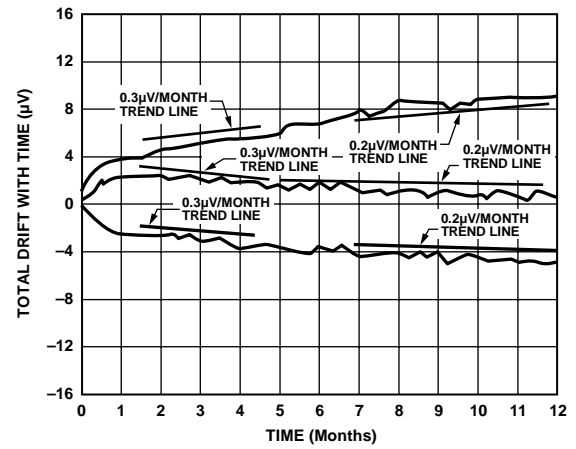


Figure 25. Offset Voltage Drift vs. Time

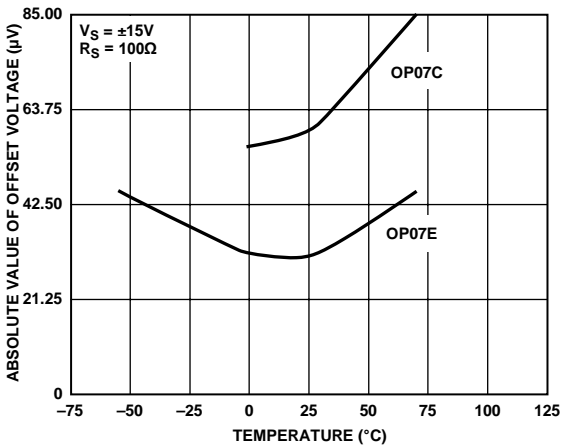


Figure 23. Untrimmed Offset Voltage vs. Temperature

TYPICAL APPLICATIONS

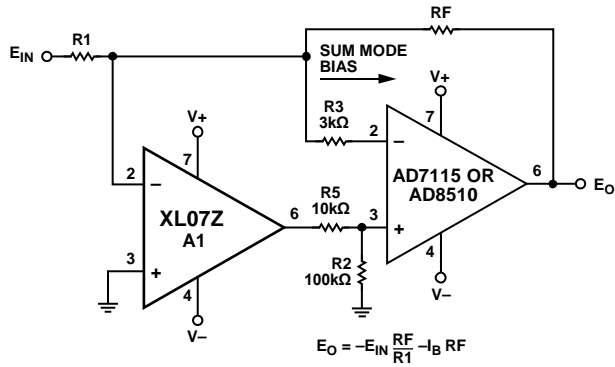


Figure 26. Typical Offset Voltage Test Circuit

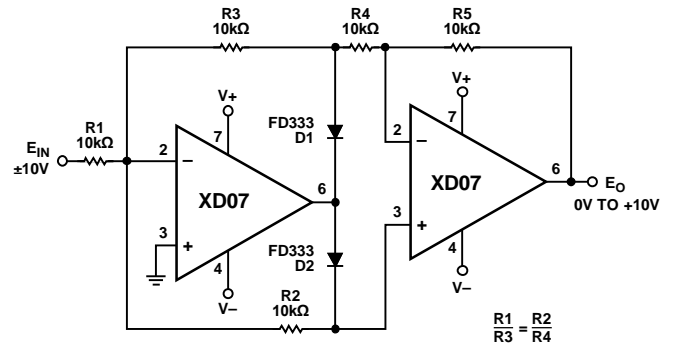


Figure 29. Absolute Value Circuit

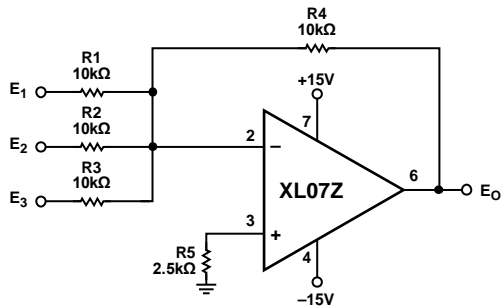
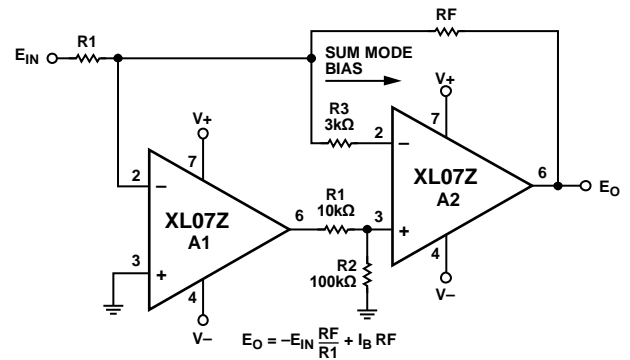


Figure 27. Typical Low Frequency Noise Circuit



NOTES
1. PINOUT SHOWN FOR P PACKAGE

Figure 30. High Speed, Low V_{0s} Composite Amplifier

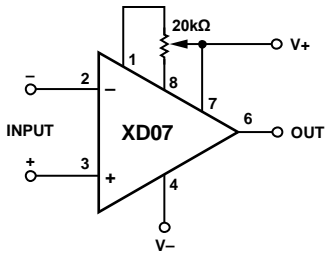
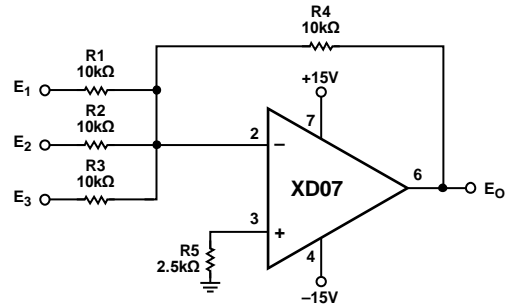


Figure 28. Optional Offset Nulling Circuit

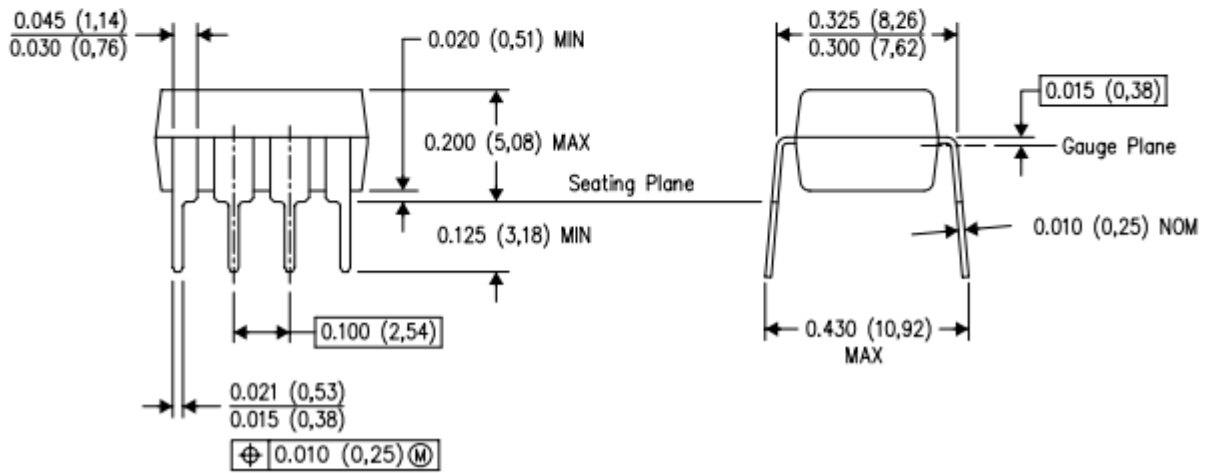
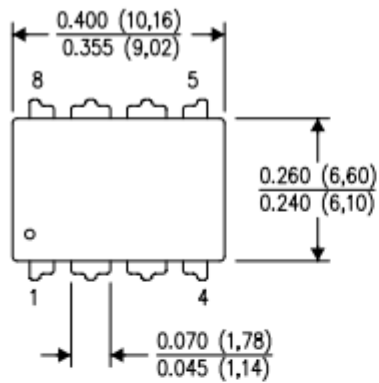


NOTES
1. PINOUT SHOWN FOR P PACKAGE

Figure 31. Adjustment-Free Precision Summing Amplifier

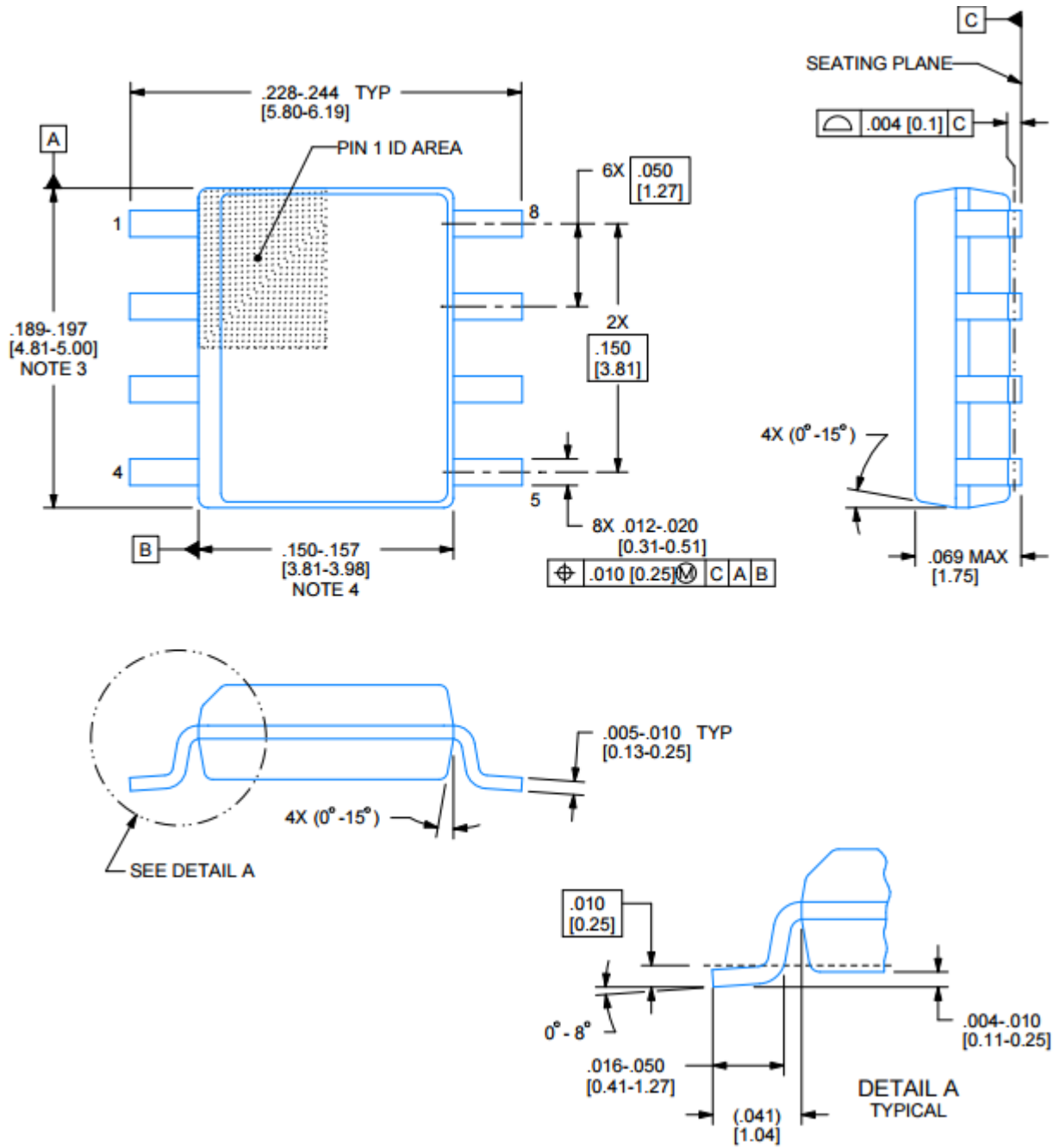
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SOP8



以上信息仅供参考. 如需帮助联系客服人员. 谢谢 XINLUDA

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