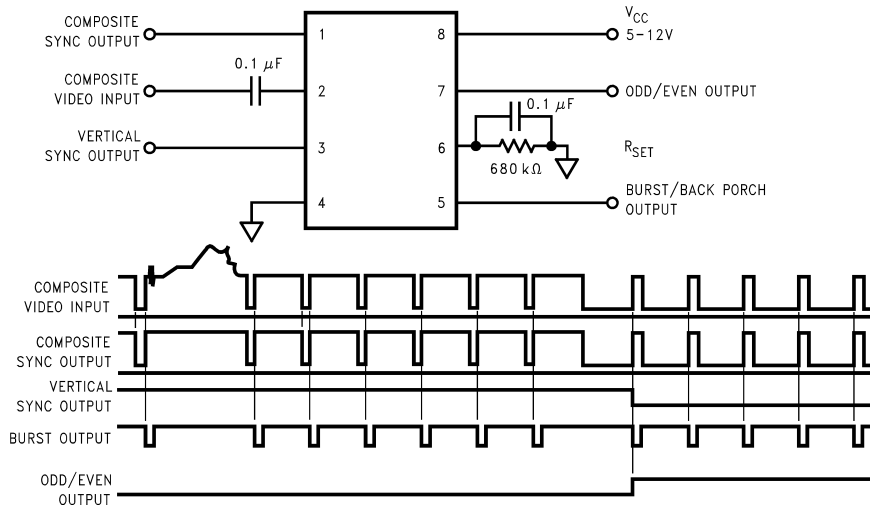## FEATURES

- **AC Coupled Composite Input Signal**
- **>10 kΩ Input Resistance**
- **<10 mA Power Supply Drain Current**
- **Composite Sync and Vertical Outputs**
- **Odd/Even Field Output**
- **Burst Gate/Back Porch Output**
- **Horizontal Scan Rates to 150 kHz**
- **Edge Triggered Vertical Output**
- **Default Triggered Vertical Output for Non-standard Video Signal (Video Games-Home Computers)**

DESCRIPTION

The 1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL [1] and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Connection Diagram

Absolute Maximum Ratings [1][2]

Supply Voltage			13.2V
Input Voltage			3 V_{P-P} (V_{CC} = 5V) 6 V_{P-P} (V_{CC} ≥ 8V)
Output Sink Currents; Pins, 1, 3, 5			5 mA
Output Sink Current; Pin 7			2 mA
Package Dissipation [3]			1100 mW
Storage Temperature Range			−65°C to +150°C
ESD Susceptibility [4]			2 kV
ESD Susceptibility [5]			200 V
Soldering Information	PDIP Package (10 sec.)		260°C
	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110°C/W, junction to ambient.
(3) ESD susceptibility test uses the "human body model, 100 pF discharged through a 1.5 kΩ resistor".
(4) Machine Model, 220 pF – 240 pF discharged through all pins.

Electrical Characteristics 1881

V_{CC} = 5V; R_{SET} = 680 kΩ; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A=25°C

Parameter	Conditions		Min	Typ [1]	Max	Units
Supply Current	Outputs at Logic 1	V_{CC} = 5V V_{CC} = 12V		5.2 5.5	10 12	mA
DC Input Voltage	Pin 2		1.3	1.5	1.8	V
Input Threshold Voltage	[2]		55	70	85	mV
Input Discharge Current	Pin 2; V_{IN} = 2V		6	11	16	µA
Input Clamp Charge Current	Pin 2; V_{IN} = 1V		0.2	0.8		mA
R_{SET} Pin Reference Voltage	Pin 6; [3]		1.10	1.22	1.35	V
Composite Sync. & Vertical Outputs	I_{OUT} = 40 µA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.0 11.0	4.5		V
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5V V_{CC} = 12V	2.4 10.0	3.6		V
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 µA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.0 11.0	4.5		V
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1			0.2	0.8	V
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3			0.2	0.8	V
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5			0.2	0.8	V
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7			0.2	0.8	V
Vertical Sync Width			190	230	300	µs
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		2.5	4	4.7	µs
Vertical Default Time	[4]		32	65	90	µs

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.
(3) Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5 and 7) to the R_{SET} pin (Pin 6).
(4) Delay time between the start of vertical sync (at input) and the vertical output pulse.

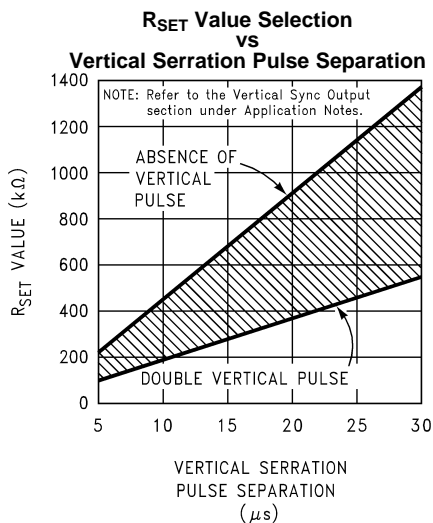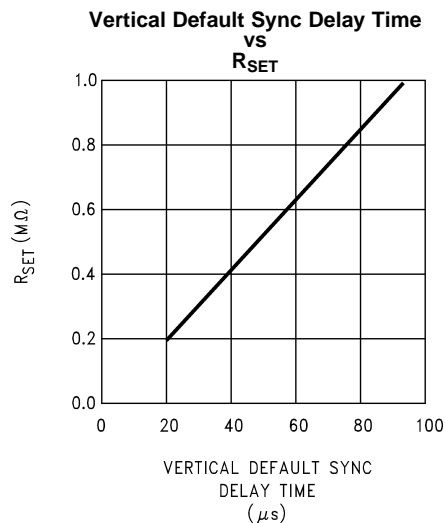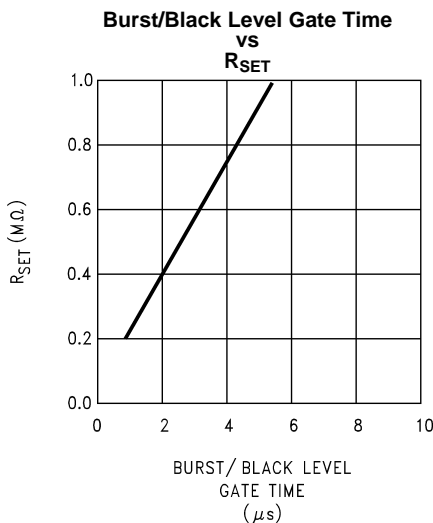## Typical Performance Characteristics

**R$_{SET}$ Value Selection
vs
Vertical Serration Pulse Separation**

NOTE: Refer to the Vertical Sync Output
section under Application Notes.

ABSENCE OF
VERTICAL
PULSE

DOUBLE VERTICAL PULSE

R$_{SET}$ VALUE (kΩ)

VERTICAL SERRATION
PULSE SEPARATION
(μs)

Figure 1.

**Vertical Default Sync Delay Time
vs
R$_{SET}$**

R$_{SET}$ (MΩ)

VERTICAL DEFAULT SYNC
DELAY TIME
(μs)

Figure 2.

**Burst/Black Level Gate Time
vs
R$_{SET}$**

R$_{SET}$ (MΩ)

BURST/ BLACK LEVEL
GATE TIME
(μs)

Figure 3.

**Vertical Pulse Width
vs
R$_{SET}$**

R$_{SET}$ (MΩ)

VERTICAL PULSE WIDTH

(μs)

Figure 4.

**Vertical Pulse Width
vs
Temperature**

VERTICAL PULSE WIDTH (μs)

TEMPERATURE (℃)

Figure 5.

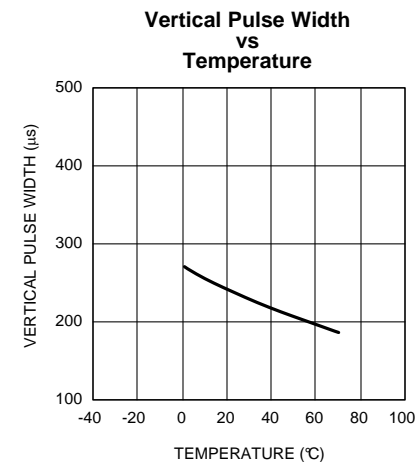**Supply Current
vs
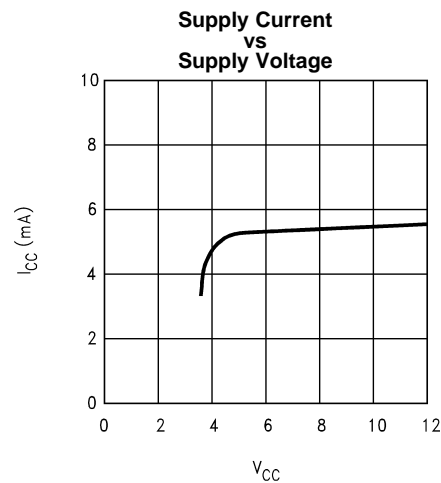Supply Voltage**

I$_{CC}$ (mA)

V$_{CC}$

Figure 6.

3

Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 µs in this example. This graph is linear, meaning that a value as large as 2.7 MΩ can be used for R_{SET} (twice the value as the maximum at 30 µs). Due to leakage currents it is advisable to keep the value of R_{SET} under 2.0 MΩ. In this example a value of 1.0 MΩ is selected, well above the minimum of 680 kΩ. With this value for R_{SET} the pulse width of the vertical sync output pulse of the 1881 is about 340 µs.
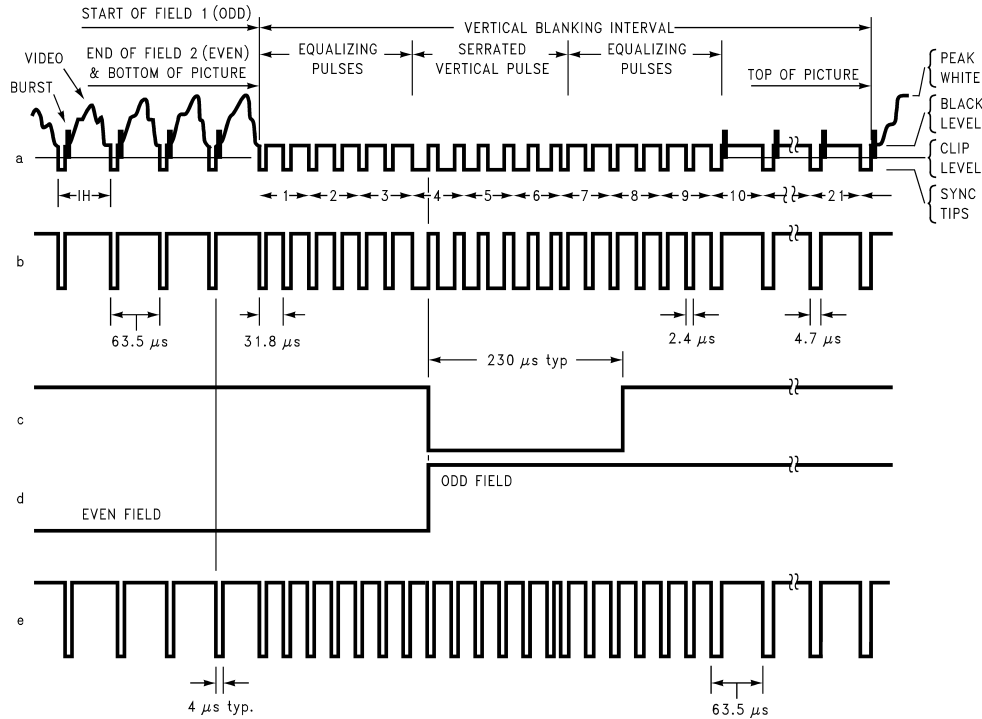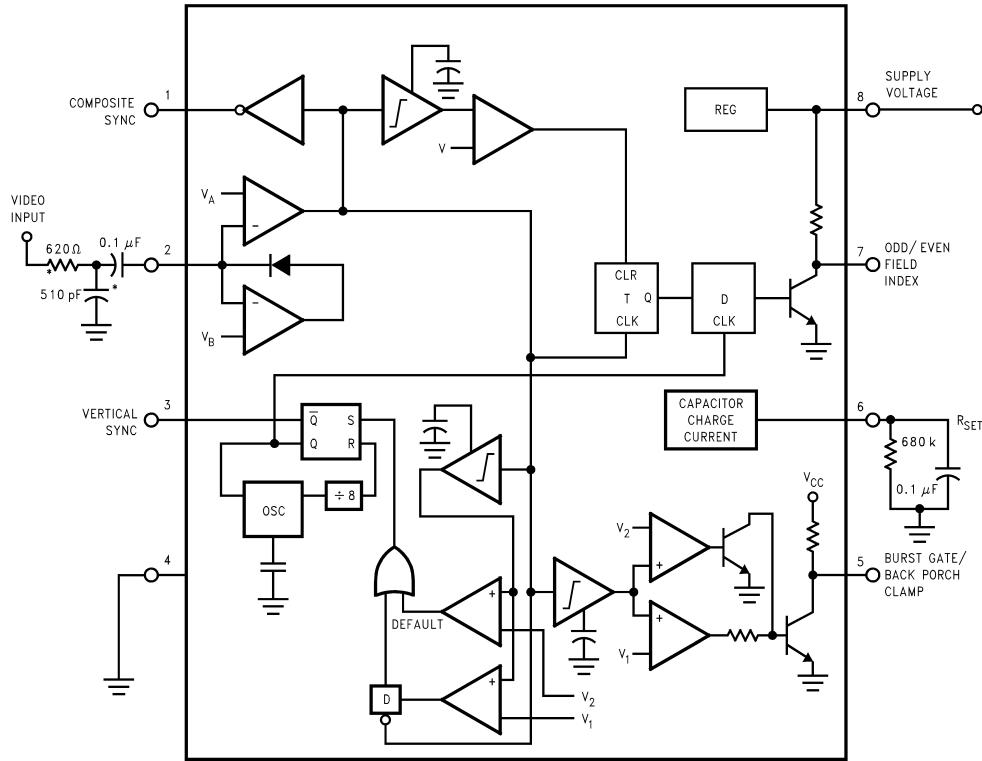

Figure 7. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp

*Components Optional, See Text

Figure 8.

ODD/EVEN FIELD PULSE

An unusual feature of 1881 is an output level from Pin 7 that identifies the video field present at the input to the 1881. This can be useful in frame memory storage applications or in extracting test signals that occur in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the "odd field" or "even field". The "even field" or "field 2" has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. Figure 8*(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the 1881 again integrates the composite sync waveform (Figure 8). A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flip-flop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

MULTIPLE CONTIGUOUS VIDEO LINE
SELECTOR WITH BLACK LEVEL RESTORATION

The circuit in Figure 10 will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the 1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.
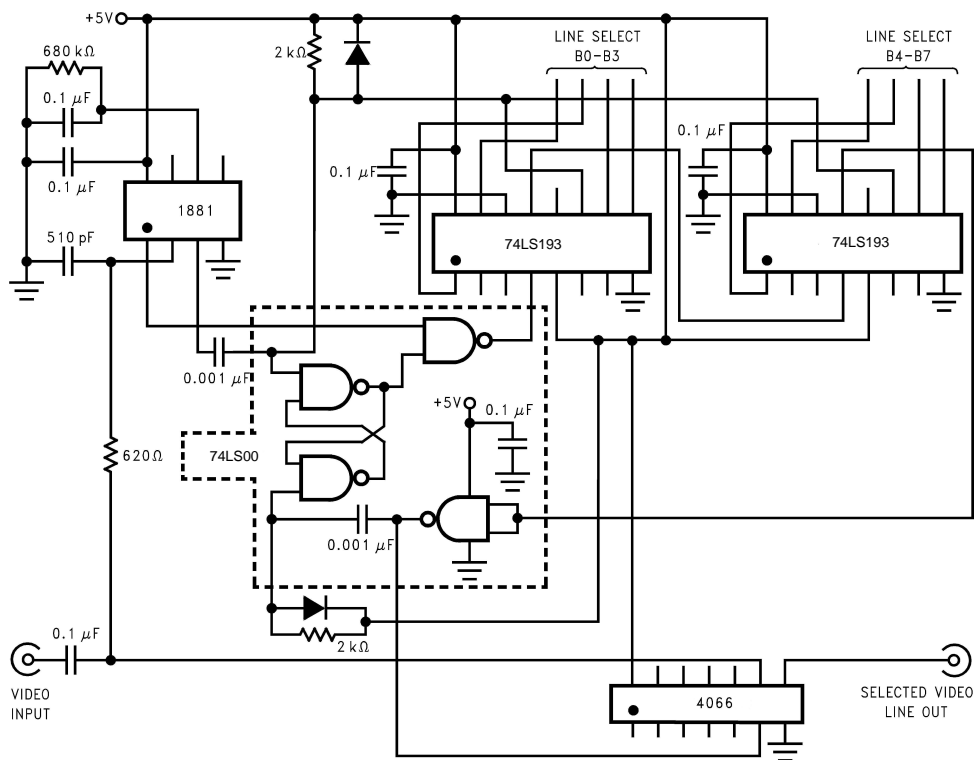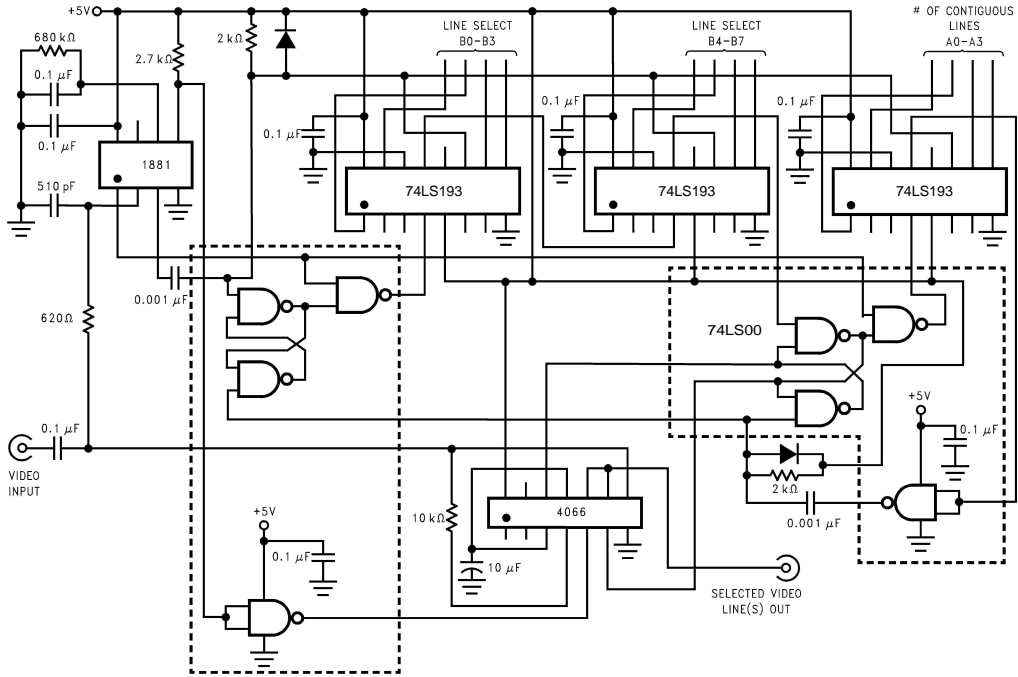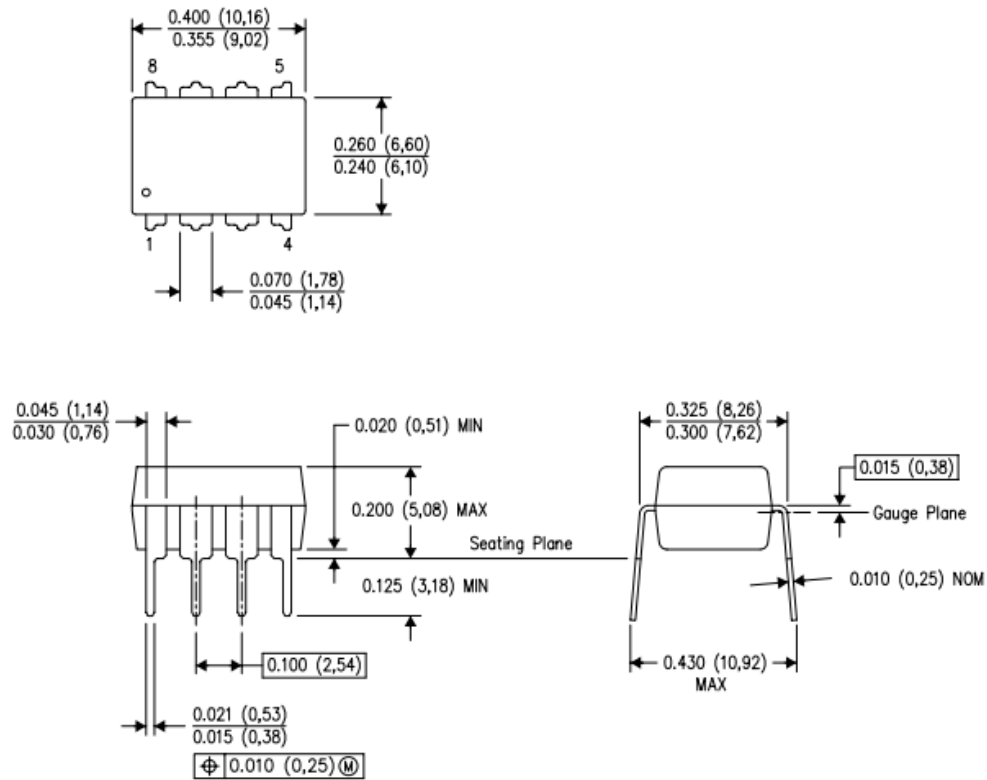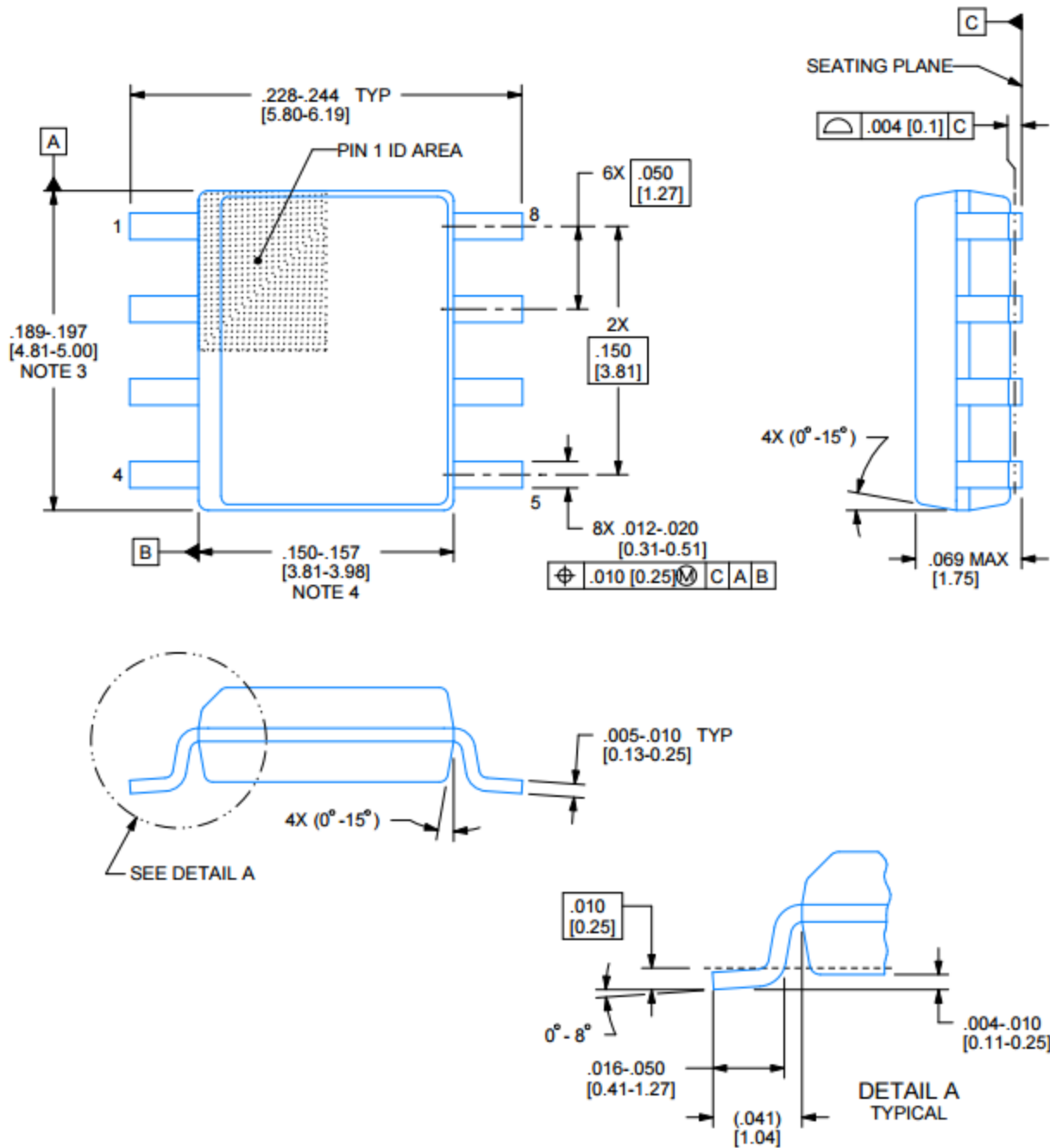
Typical Applications

Figure 9.   Video Line Selector

Figure 10. Multiple Contiguous Video Line Selector with Black Level Restoration

.228-.244 TYP
[5.80-6.19]

PIN 1 ID AREA

A

1

.189-.197
[4.81-5.00]
NOTE 3

4

B

.150-.157
[3.81-3.98]
NOTE 4

8

6X .050
[1.27]

2X
.150
[3.81]

5

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25]Ⓜ C A B

C

SEATING PLANE

◯ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA

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