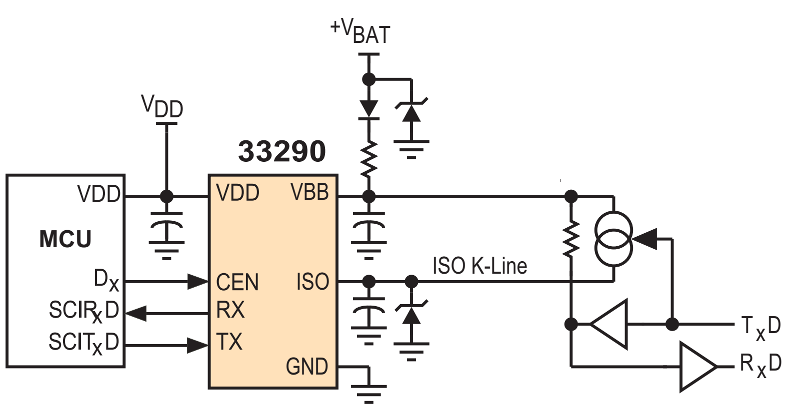
ISO K Line Serial Link Interface

The 33290 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller and systems off-board the vehicle via the special ISO K line. The 33290 is designed to meet the Diagnostic Systems ISO9141 specification. The device's K line bus driver's output is fully protected against bus shorts and overtemperature conditions.

The 33290 derives its robustness to temperature and voltage extremes by being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Although the 33290 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of -40ºC ≤ T_A ≤ 125ºC and 8.0 V ≤ V_{BB} ≤ 18 V supply. The economical SO-8 surface-mount plastic package makes the 33290 very cost effective.

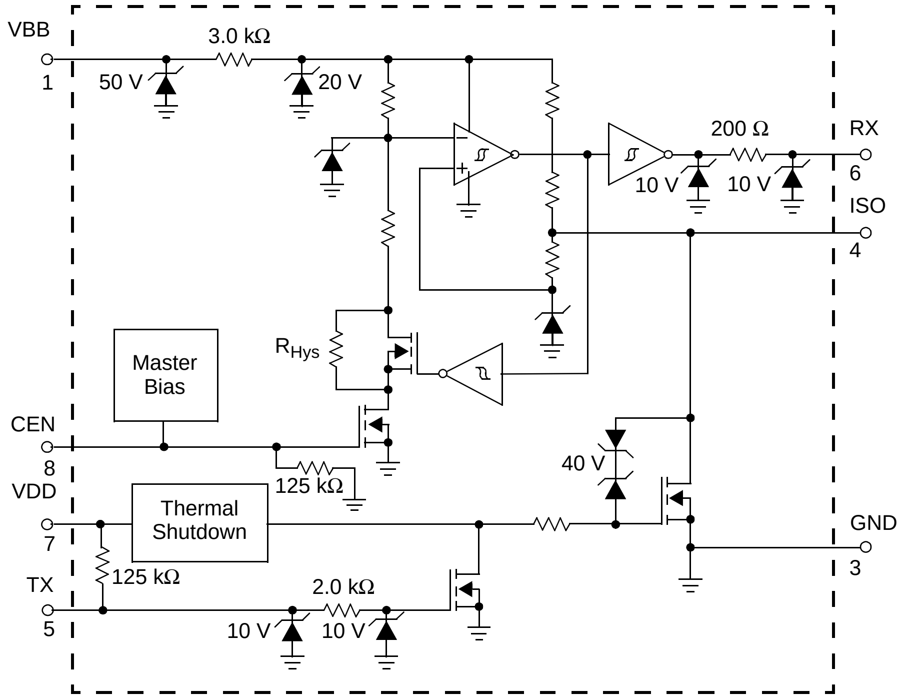
Features

- Operates Over Wide Supply Voltage of 8.0 to 18V
- Operating Temperature of -40 to 125°C
- Interfaces Directly to Standard CMOS Microprocessors
- ISO K Line Pin Protected Against Shorts to Ground
- Thermal Shutdown with Hysteresis
- ISO K Line Pin Capable of High Currents
- ISO K Line Can Be Driven with up to 10 nF of Parasitic Capacitance
- 8.0 kV ESD Protection Attainable with Few Additional Components
- Standby Mode: No V_{Bat} Current Drain with V_{DD} at 5.0 V
- Low Current Drain During Operation with V_{DD} at 5.0 V
- Pb-Free Packaging Designated by Suffix Code EF



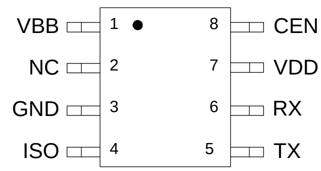
33290 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM



33290 Simplified Block Diagram

PIN CONNECTIONS



33290 Pin Connections

Table 1. 33290 Pin Definitions

Pin Number	Pin Name	Definition
1	VBB	Battery power through external resistor and diode.
2	NC	Not to be connected. (1)
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	TX	Logic level input for data to be transmitted on the bus.
6	RX	Logic output of data received on the bus.
7	VDD	Logic power source input.
8	CEN	Chip enable. Logic “1” for active state. Logic “0” for sleep state.

Notes

1. NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
VDD DC Supply Voltage	V_{DD}	-0.3 to 7.0	V
VBB Load Dump Peak Voltage	$V_{BB(LD)}$	45	V
ISO Pin Load Dump Peak Voltage (2)	V_{ISO}	40	V
ISO Short Circuit Current Limit	$I_{ISO(LIM)}$	1.0	A
ESD Voltage (3) Human Body Model (4) Machine Model (4)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
ISO Clamp Energy (5)	E_{clamp}	10	mJ
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Case Temperature	T_C	-40 to +125	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Power Dissipation $T_A = 25°C$	P_D	 0.8	W
Peak Package Reflow Temperature During Reflow (6), (7)	T_{PPRT}	Note 7.	°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	 150	°C/W

Notes

2. Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.
3. ESD data available upon request.
4. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500\ \Omega$), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0\ \Omega$).
5. Nonrepetitive clamping capability at 25°C.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
V_{DD} Sleep State Current T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{DD(SS)}$	–	–	0.1	mA
V_{DD} Quiescent Operating Current T_x = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{DD(Q)}$	–	–	1.0	mA
V_{BB} Sleep State Current V_{BB} = 16 V, T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{BB(SS)}$	–	–	50	µA
V_{BB} Quiescent Operating Current T_X = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable Input High-Voltage Threshold (8) Input Low-Voltage Threshold (9)	 $V_{IH(CEN)}$ $V_{IL(CEN)}$	 0.7 V_{DD} –	 – –	 – 0.3 V_{DD}	V
Chip Enable Pull-Down Current (10)	$I_{PD(CEN)}$	2.0	–	40	µA
T_X Input Low-Voltage Threshold R_{ISO} = 510 Ω (11)	$V_{IL(Tx)}$	–	–	0.3 x V_{DD}	V
T_X Input High-Voltage Threshold R_{ISO} = 510 Ω (12)	$V_{IH(Tx)}$	0.7 x V_{DD}	–	–	V
T_X Pull-Up Current (13)	$I_{PU(Tx)}$	-40	–	-2.0	µA
R_X Output Low-Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}, R_x Sinking 1.0 mA	$V_{OL(Rx)}$	–	–	0.2 V_{DD}	V
R_X Output High-Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}, R_X Sourcing 250 µA	$V_{OH(Rx)}$	0.8 V_{DD}	–	–	V
Thermal Shutdown (14)	T_{LIM}	150	170	–	°C

Notes

8. When IBB transitions to >100 µA.
9. When IBB transitions to <100 µA.
10. Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at 0.3 V_{DD}.
11. Measured by ramping T_X down from 0.7 V_{DD} and noting T_X value at which ISO falls below 0.2 V_{BB}.
12. Measured by ramping T_X up from 0.3 V_{DD} and noting the value at which ISO rises above 0.9 V_{BB}.
13. T_x pin has internal current pull-up. Pull-up current is measured with T_X pin at 0.7 V_{DD}.
14. Thermal Shutdown performance (T_{LIM}) is guaranteed by design but not production tested.

Table 3. Static Electrical Characteristics (Continued)

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ISO I/O					
Input Low Voltage Threshold R_{ISO} = 0 Ω, T_X = 0.8 V_{DD} (15)	$V_{IL(ISO)}$	–	–	0.4 x V_{BB}	V
Input High Voltage Threshold R_{ISO} = 0 Ω, T_X = 0.8 V_{DD} (16)	$V_{IH(ISO)}$	0.7 x V_{BB}	–	–	V
Input Hysteresis (17)	$V_{Hys(ISO)}$	0.05 x V_{BB}	–	0.1 x V_{BB}	V
Internal Pull-Up Current R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}, V_{ISO} = 9.0 V, V_{BB} = 18 V	$I_{PU(ISO)}$	-5.0	–	-140	µA
Short Circuit Current Limit (18) R_{ISO} = 0 Ω, T_X = 0.4 V_{DD}, V_{ISO} = V_{BB}	$I_{SC(ISO)}$	50	–	1000	mA
Output Low Voltage R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}	$V_{OL(ISO)}$	–	–	0.1 x V_{BB}	V
Output High Voltage R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}	$V_{OH(ISO)}$	0.95 x V_{BB}	–	–	V

Notes

15. ISO ramped from 0.8 V_{BB} to 0.4 V_{BB}, Monitor R_X, Value of ISO voltage at which R_X transitions to 0.3 V_{DD}.
16. ISO ramped from 0.4 V_{BB} to 0.8 V_{BB}, Monitor R_X, Value of ISO voltage at which R_X transitions to 0.7 V_{DD}.
17. Input Hysteresis, $V_{Hys(ISO)} = V_{IH(ISO)} - V_{IL(ISO)}$.
18. ISO has internal current limiting.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

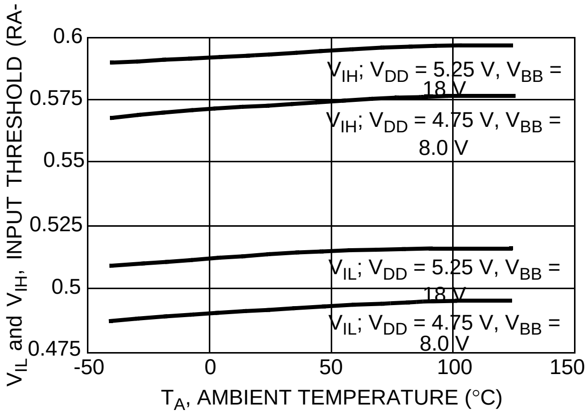
Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Fall Time [19]	$t_{fall(ISO)}$				µs
R_{ISO} = 510 Ω to V_{BB}, C_{ISO} = 10 nF to Ground		–	–	2.0	
ISO Propagation Delay [20]	$t_{PD(ISO)}$				µs
High to Low: R_{ISO} = 510 Ω, C_{ISO} = 500 pF [21]		–	–	2.0	
Low to High: R_{ISO} = 510 Ω, C_{ISO} = 500 pF [22]		–	–	2.0	

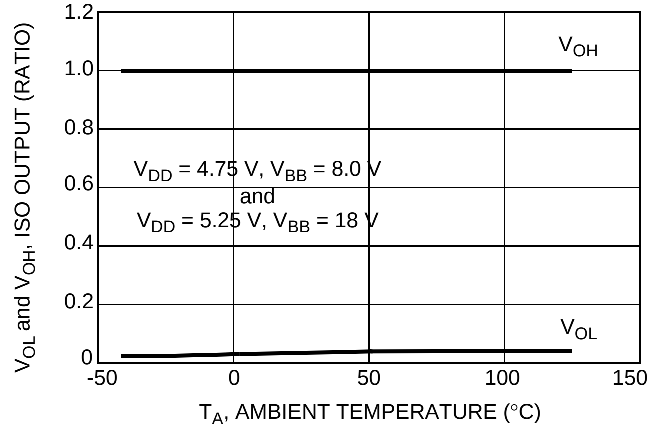
Notes

19. Time required ISO voltage to transition from 0.8 V_{BB} to 0.2 V_{BB}.
20. Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.
21. Step T_X voltage from 0.2 V_{DD} to 0.8 V_{DD}. Time measured from $V_{IH(ISO)}$ until V_{ISO} reaches 0.3 V_{BB}.
22. Step T_X voltage from 0.8 V_{DD} to 0.2 V_{DD}. Time measured from $V_{IL(ISO)}$ until V_{ISO} reaches 0.7 V_{BB}.

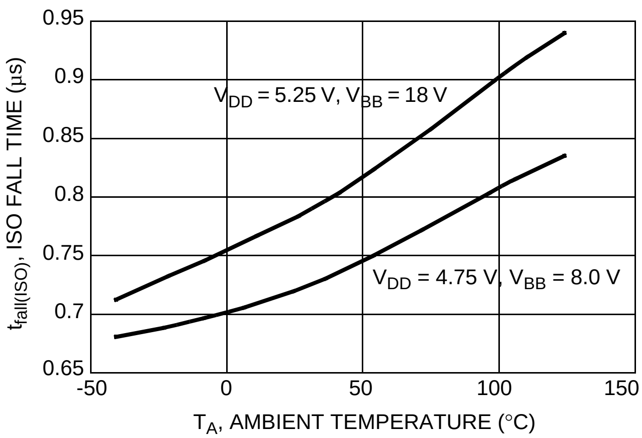
ELECTRICAL PERFORMANCE CURVES



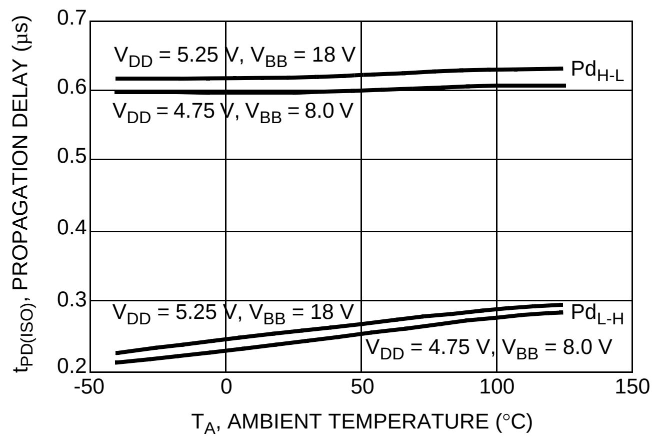
ISO Input Threshold/V_{BB} vs. Temperature



ISO Fall Time vs. Temperature



ISO Output/V_{BB} vs. Temperature



ISO Propagation Delay vs. Temperature

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