1. DESCRIPTION

The XL4021B is a 8-stage parallel- or serial-input/serial output chip having common CLOCK and PARALLEL/SERIALCONTROL inputs, a single SERIAL data input, and individual parallel “JAM” inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q“ outputs are also available from stages 6 and 7. In the XL4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CON- TROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the XL4021B, the CLOCK input of the internal stage is “forced” when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

The XL4021B is supplied in packages SOP16.

2. FEATURES

- Medium-speed operation ... 12 MHz (typ.) clock rate at V_{DQ}-V_{SS} = 10 V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- 100% tested for quiescent current at 20 V
- Maximum input current of 1µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 µA at V_{DD} «= 5 V

  2 Vat V_{DD} = 10V

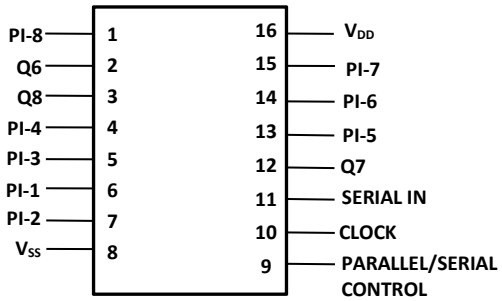
  2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, “Standard Specifications for Description of 'B' Series CMOS Devices”

3. Applications

- Parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

4. PIN FUNCTIONS

XL4021B



(TOP VIEW)

Pin number	Symbol	Name and function
6, 7, 5, 4, 13, 14, 15, 1	PI-1 to PI-8	Parallel input
11	SERIAL IN	Serial input
9	PARALLEL/SERIAL CONTROL	Parallel/serial input control
10	CLOCK	Clock input
2, 3, 12	Q6, Q7, Q8	Buffered outputs
8	V_{SS}	Negative supply voltage
16	V_{DD}	Positive supply voltage

5. LOGIC DIAGRAM

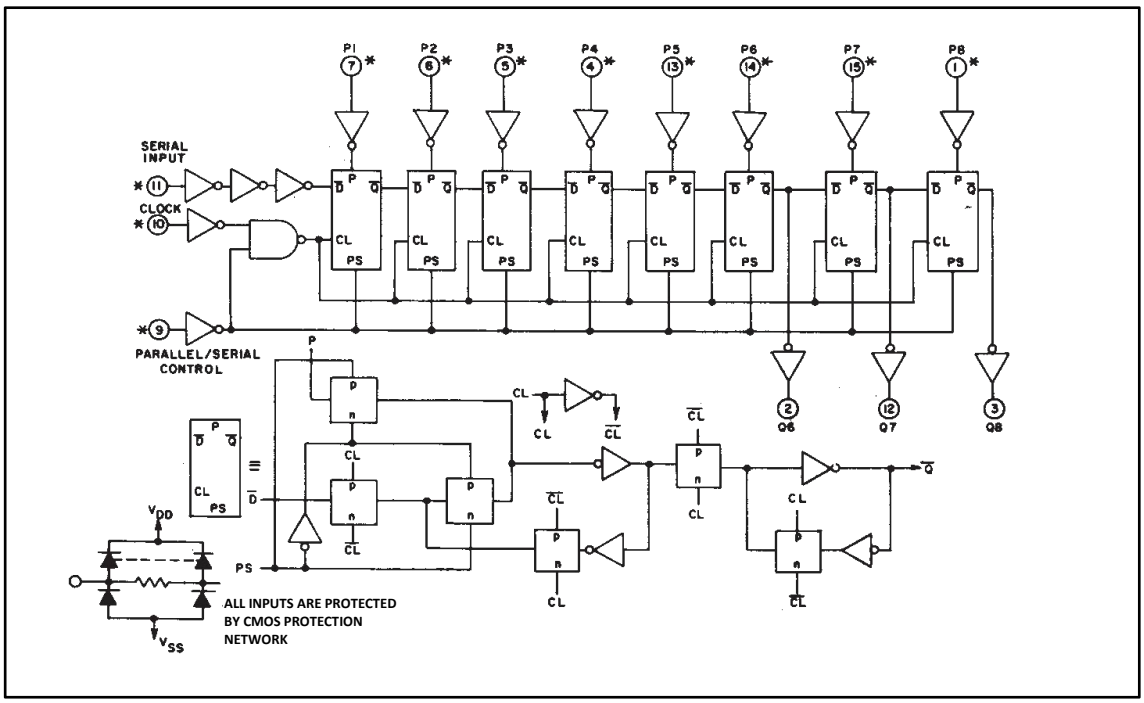


Fig. 1 Logic diagram for XL4021B.

CL	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Qi (Internal)	On
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
⎍	0	0	X	X	0	Qn 1
⎍	1	0	X	X	1	Qn 1
⎎	X	0	X	X	Q_1	On

[1] X - DON'T CARE CASE

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{DD}	DC SUPPLY-VOLTAGE RANGE	Voltages referenced to Vgg Terminal	-	+20	V
V_{IN}	INPUT VOLTAGE RANGE, ALL INPUTS	ALL INPUTS	-	VDD+0.5	V
V_O	DC INPUT CURRENT, ANY ONE INPUT		-10	+10	mA
P_D	POWER DISSIPATION PER PACKAGE	For T_A = -55°C to +100°C	-	500	mW
		For T_A = +100°C to +125°C	Derate linearity at 12mW/°C to 200mW		
P_{DDO}	DEVICE DISSIPATION PER OUTPUT TRANSISTOR	FORT_A = FULL PACKAGE-fEMPERATURE RANGE (All Package Types)	-	+100	mW
T_A	OPERATING^EMPERAYURE RANGE (TA)		-40	+85	°C
T_{stg}	STORAGETEMPERATURE RANG		-50	+125	°C
T_L	LEAD TEMPERATURE(DURING SOLDERING)	At distance 1 /16 ± 1/32 inch (1.59 ± 0,79mm) from case for 10s max	-	+265	°C

6.2. Recommended Operating Conditions at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (T_A = Full Package-Temperature Range)	-	3	18	V
Clock Pulse Width, t_w	5 10 15	180 80 50	-	ns
Clock Frequency, f_{CL}	5 10 15	-	3 6 8.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10 15	-	15 15 15	MS
Set-up Time, t_S: Serial Input (ref. to CL)	 5 10 15	 120 80 60	-	ns
Parallel Inputs XL4021B (ref. to P/S)	5 10 15	50 30 20	-	ns
Parallel/Serial Pulse Width, t_W (XL4021B)	5 10 15	160 80 50	-	ns
Parallel/Sertal Removal Time, t_{REM} (XL4021B)	5 10 15	280 140 100	-	ns

6.3. Static Electrical Characteristics

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_0 (V)	V_{IN} <V>	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{QD} Max.	-	0,5	5	5	5	150	150	-	0.04	5	MA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{QL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{QH\ MIN}$	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
		0,10	10	0.05				-	0	0.05	
	-	0,15	15	005				-	0	0.05	
Output Voltage: High-Level, V_{QH} Min.	-	0,5	5	4.95				4.95	5	—	
		0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage V_{IL} Max.	0.5,4.5	-	5	1.5				-	-	1.5	V
	1,9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10"5	±0.1	MA

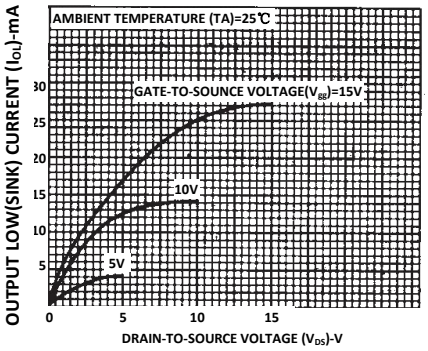


Fig. 2 Typical output low (sink) current characteristics.

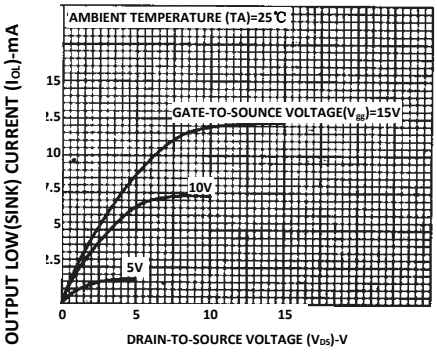


Fig. 3 Minimum output low (sink) current characteristics.

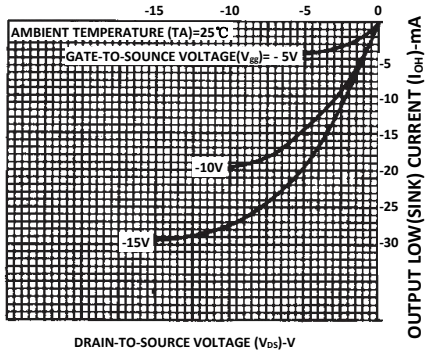


Fig. 4 Typical output low (source) current characteristics.

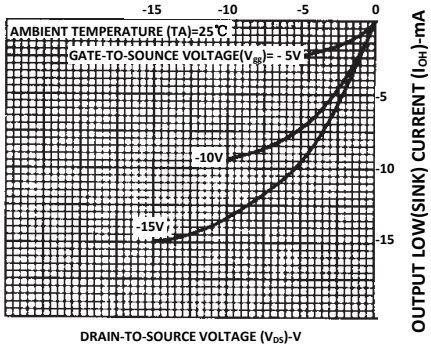


Fig. 5 Minimum output low (source) current characteristics.

6.4. DYNAMIC ELECTRICAL CHARACTERISTICS at TA=25°C, Input t_r,t_f=20 ns, C_L=50 pF, RL=200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time, t_{PLH}, t_{PHL}		5 10 15	-	160 80 60	320 160 120	ns
Transition Time, t_{THL}- t_{TLH}		5 10 15	-	100 50 40	200 100 80	ns
Maximum Clock Input Frequency, f_{CL}		5 10 15	3 6 8.5	6 12 17	-	MHz
Minimum Clock Pulse Width, t_W		5 10 15	-	90 40 25	180 80 50	ns
Clock Rise and Fall Time, t_rCL, t_fCL[1]		5 10 15	-	-	15 15 15	µs
Minimum Set-up Time, t_S: Serial Input (ref. to CL)		5 10 15	- - -	60 **40** 30	120 80 60	ns
Parallel Inputs XL4021B (ref. to P/S)		5 10 15	- - -	25 15 10	50 30 20	ns
Minimum Hold Time, t_H: Serial In, Parallel In, Parallel/Serial Control		5 10 15	- - -	- - -	0 0 0	ns
Minimum P/S Pulse Width, t_{WH} (XL4021B)		5 10 15	- - -	80 40 25	160 80 50	ns
Minimum P/S Removal Time, r_{REM} XL4021B (ref. to CL)		5 10 15	- - -	140 70 50	280 140 100	ns
Average Input Capacitance, CI	Any Input		-	5	7.5	pF

[2] If more than one unit is cascaded trCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

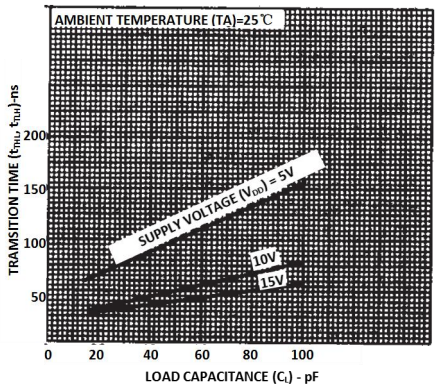


Fig.6 Typical transition time as a function of load capacitance.

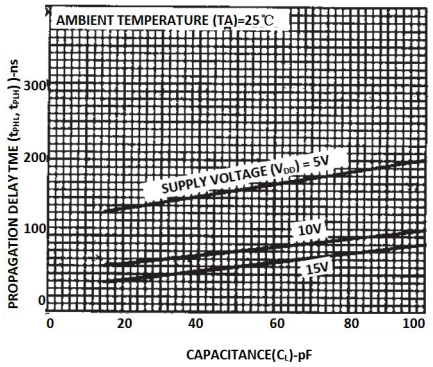


Fig. 7 Typical propagation delay time as a function of load capacitance.

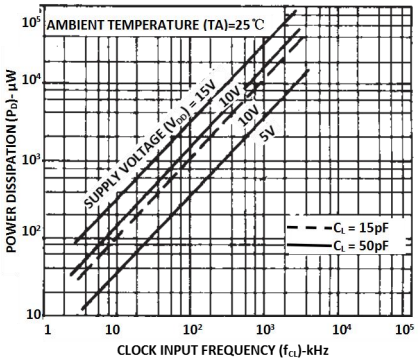


Fig.8 Typical dynamic power dissipation as a function of dock input frequency.

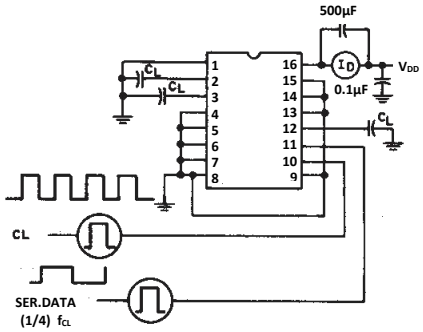


Fig.9 Dynamic power dissipation test circuit.

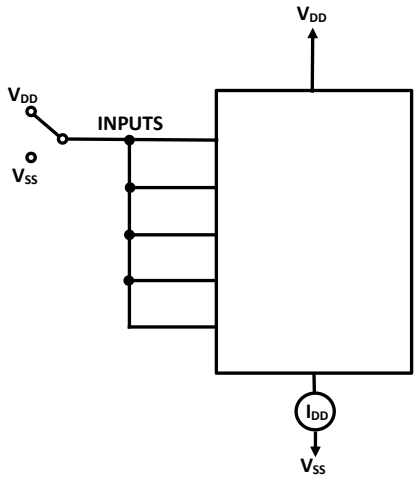


Fig. 10 Quiescent device current test circuit.

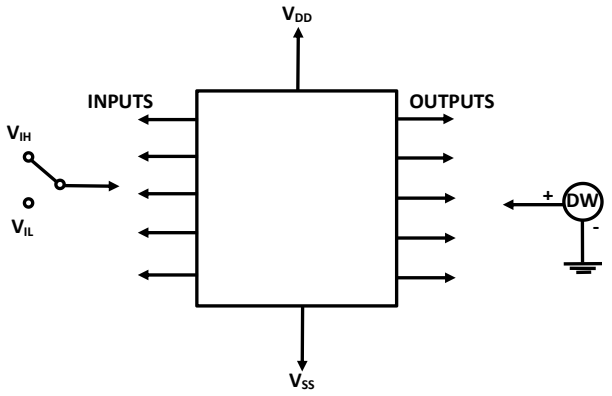
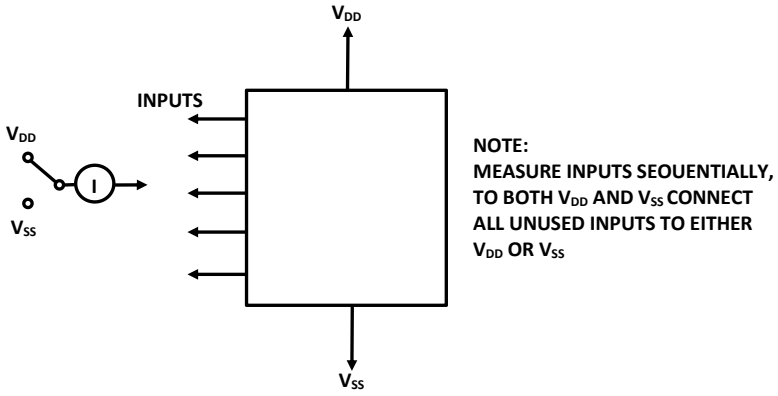


Fig. 11 Input voltage test circuit.



NOTE:
MEASURE INPUTS SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS} CONNECT
ALL UNUSED INPUTS TO EITHER
V_{DD} OR V_{SS}

Fig. 12 Input current test circuit.

7. ORDERING INFORMATION

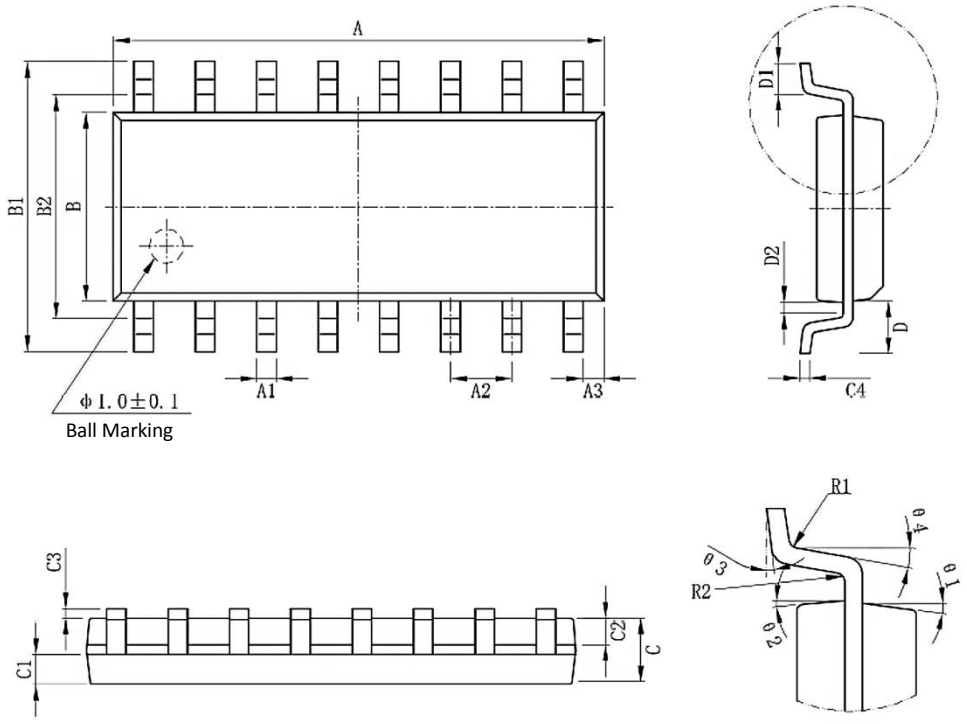
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL4021B	XL4021B	SOP16	10.00 * 3.95	-40 to +85	MSL3	T &R	2500

8. DIMENSIONAL DRAWINGS

SOP16

Size / Mark	Min (mm)	Max (mm)	Size / Mark	Min (mm)	Max (mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.40	1.60	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.05	0.25			



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