XD4558 DIP8 / XL4558 SOP8

1 Features

- Continuous Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth: 3 MHz Typ
- Gain and Phase Match Between Amplifiers
- Low Noise: 8 nV/√Hz Typ at 1 kHz

2 Applications

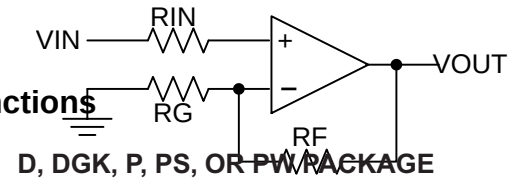
- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The XDXL/4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the μA741, except that offset null capability is not provided.

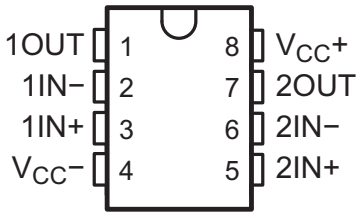
The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

4 Noninverting Amplifier Schematic



5 Pin Configuration and Functions

D, DGK, P, PS, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting Input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting Input
2OUT	7	O	Output
V_{CC}+	8	—	Positive Supply
V_{CC}-	4	—	Negative Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)		18	V
V_{CC-}			–18	
V_{ID}	Differential input voltage(3)		±30	V
V_I	Input voltage (any input)(2)(4)		±15	V
	Duration of output short circuit to ground, one amplifier at a time(5)		Unlimited	
T_J	Operating virtual junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	0	500	V
		Charged device model (CDM), per AEC Q100-011 (2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}			–5	–15	
T_A	Operating free-air temperature	XD4558	0	70	°C
		XL4558	–40	85	

6.4 Thermal Information

THERMAL METRIC(1)		XDXL/4558					UNIT
		D	DGK	P	PS	PW	
		8 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	172	85	95	149	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = –15 V

PARAMETER			TEST CONDITIONS(1)	T_A (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		V_O = 0	25°C		0.5	6	mV
				Full range			7.5	
I_{IO}	Input offset current		V_O = 0	25°C		5	200	nA
				Full range			300	
I_{IB}	Input bias current		V_O = 0	25°C		150	500	nA
				Full range			800	
V_{ICR}	Common-mode input voltage range			25°C	±12	±14		V
V_{OM}	Maximum output voltage swing		R_L = 10 kΩ	25°C	±12	±14		V
			R_L = 2 kΩ	25°C	±10	±13		
				Full range	±10			
A_{VD}	Large-signal differential voltage amplification		R_L ≥ 2 kΩ, V_O = ±10 V	25°C	20	300		V/mV
				Full range	15			
B_1	Unity-gain bandwidth			25°C		3		MHz
r_i	Input resistance			25°C	0.3	5		MΩ
CMRR	Common-mode rejection ratio			25°C	70	90		dB
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)		V_{CC} = ±15 V to ±9 V	25°C		30	150	μV/V
V_n	Equivalent input noise voltage (closed loop)		A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C		8		nV/√Hz
I_{CC}	Supply current (both amplifiers)		V_O = 0, No load	25°C		2.5	5.6	mA
				T_A min		3	6.6	
				T_A max		2.3	5	
P_D	Total power dissipation (both amplifiers)		V_O = 0, No load	25°C		75	170	mW
				T_A min		90	200	
				T_A max		70	150	
V_{O1}/V_{O2}	Crosstalk attenuation	Open loop	R_S = 1 kΩ, f = 10 kHz	25°C		85		dB
		A_{VD} = 100				105		

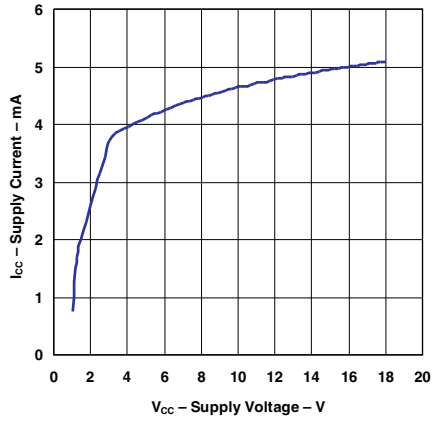
(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.
(2) Full range is 0°C to 70°C for XD4558 and –40°C to 85°C for XL4558

6.6 Operating Characteristics

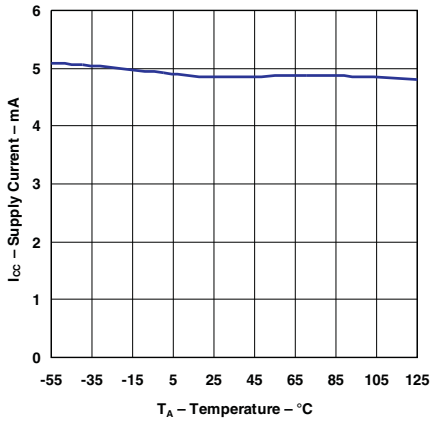
V_{CC+} = 15 V, V_{CC-} = –15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF		0.13		ns
	Overshoot	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF		5%		
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF	1.1	1.7		V/μs

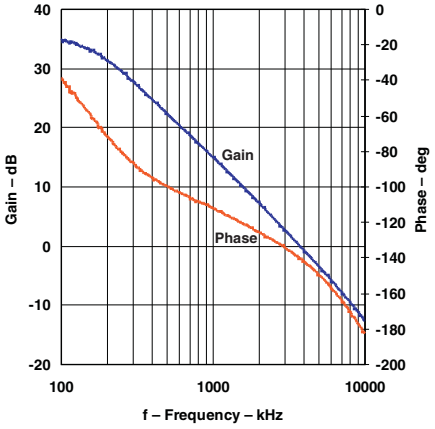
6.7 Typical Characteristics



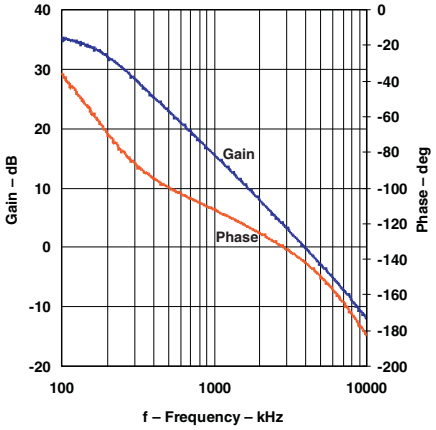
Supply Current vs Supply Voltage (T_A = 25°C)



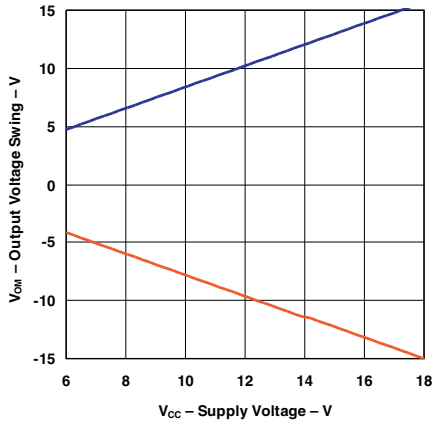
Supply Current vs Temperature (V_{CC} = ±15 V)



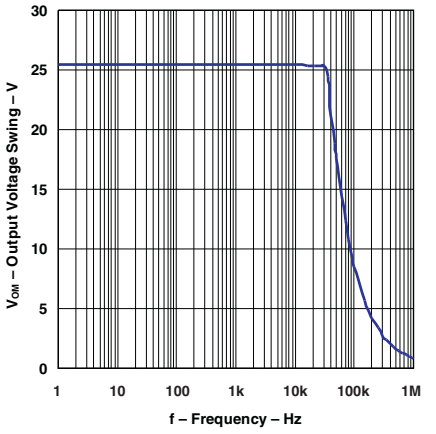
Gain and Phase vs Frequency (V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 22 pF)



Gain and Phase vs Frequency (V_{CC} = ±15 V, R_L = 10 kΩ, C_L = 22 pF)

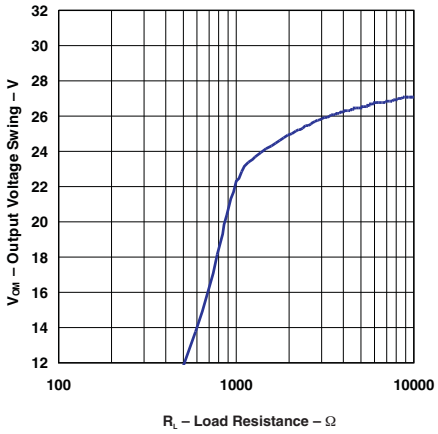


Output Voltage Swing vs Supply Voltage (R_L = 2 kΩ, T_A = 25°C)

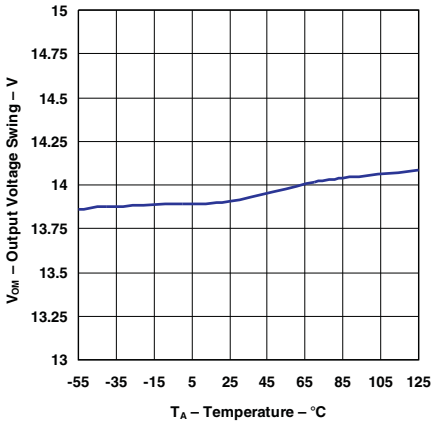


Output Voltage Swing vs Frequency (V_{CC} = ±15 V, R_L = 2 kΩ, T_A = 25°C)

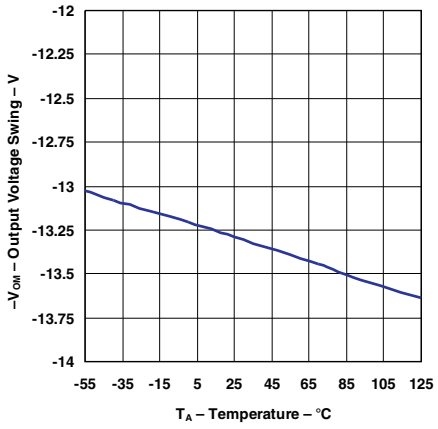
Typical Characteristics (continued)



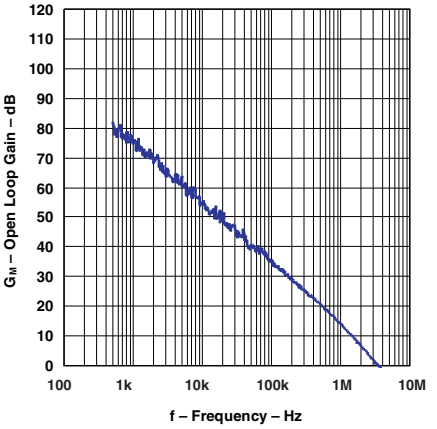
Output Voltage Swing vs Load Resistance
(V_{CC} = ±15 V, T_A = 25°C)



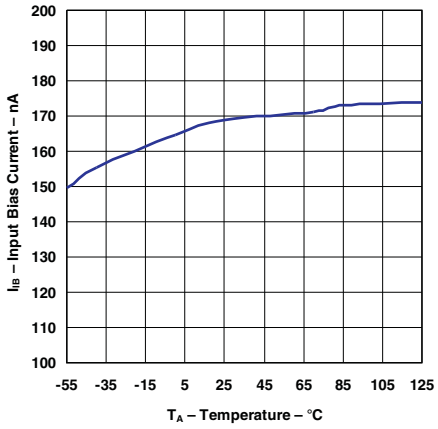
Output Voltage Swing vs Temperature
(V_{CC} = ±15 V, R_L = 10 kΩ)



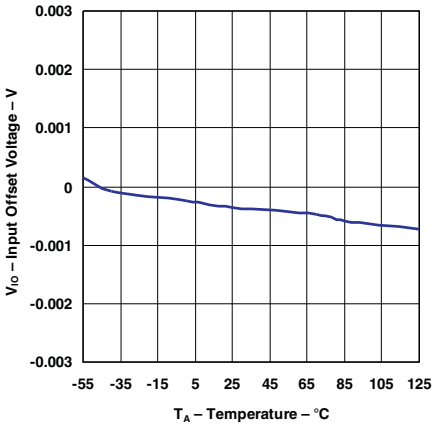
Negative Output Voltage Swing vs Temperature
(V_{CC} = ±15 V, R_L = 10 kΩ)



Open Loop Gain vs Frequency
(V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 22 pF, T_A = 25°C)

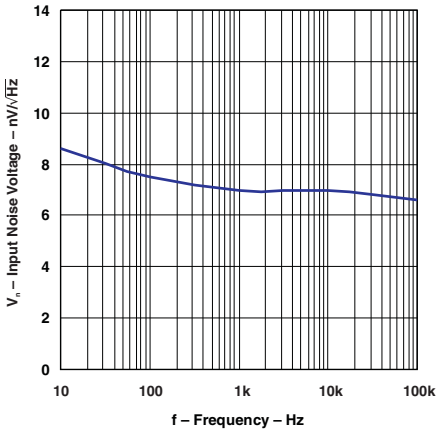


Input Bias Current vs Temperature
(V_{CC} = ±15 V)



Input Offset Voltage vs Temperature
(V_{CC} = ±15 V)

Typical Characteristics (continued)



Input Noise Voltage vs Frequency
(V_{CC} = ±15 V, T_A = 25°C)

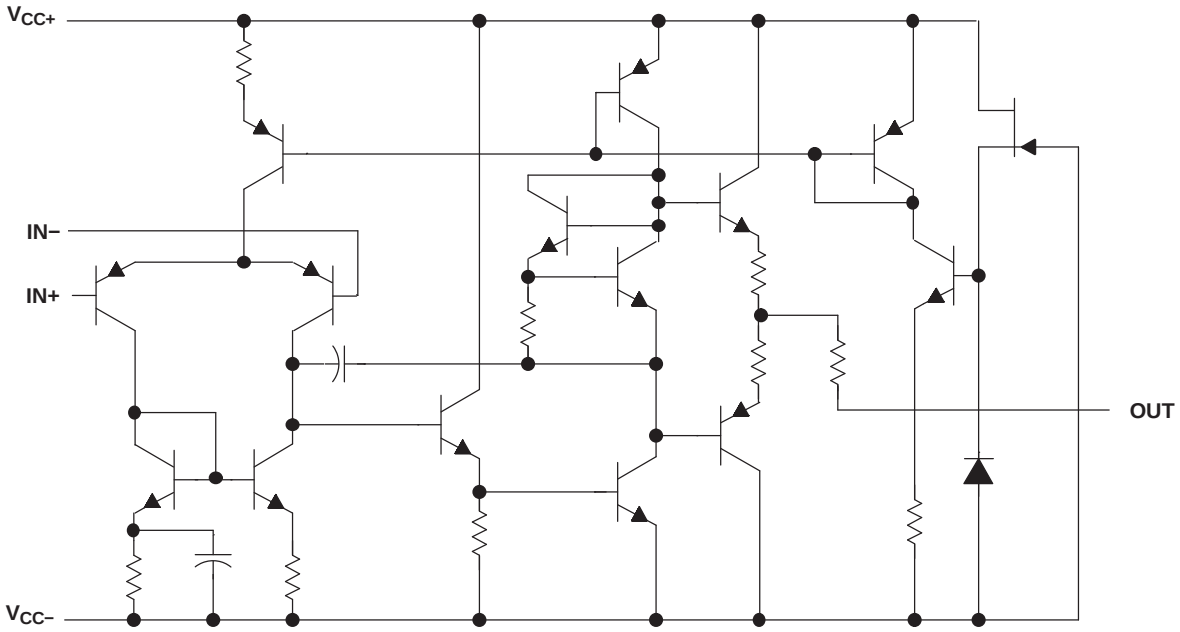
7 Detailed Description

7.1 Overview

The XDXL/4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the μA741, except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The XDXL/4558 device has a 3-MHz unity-gain bandwidth.

7.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the XDXL/4558device is 90 dB.

7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The XDXL/4558 device has a 1.7 V/μs slew rate.

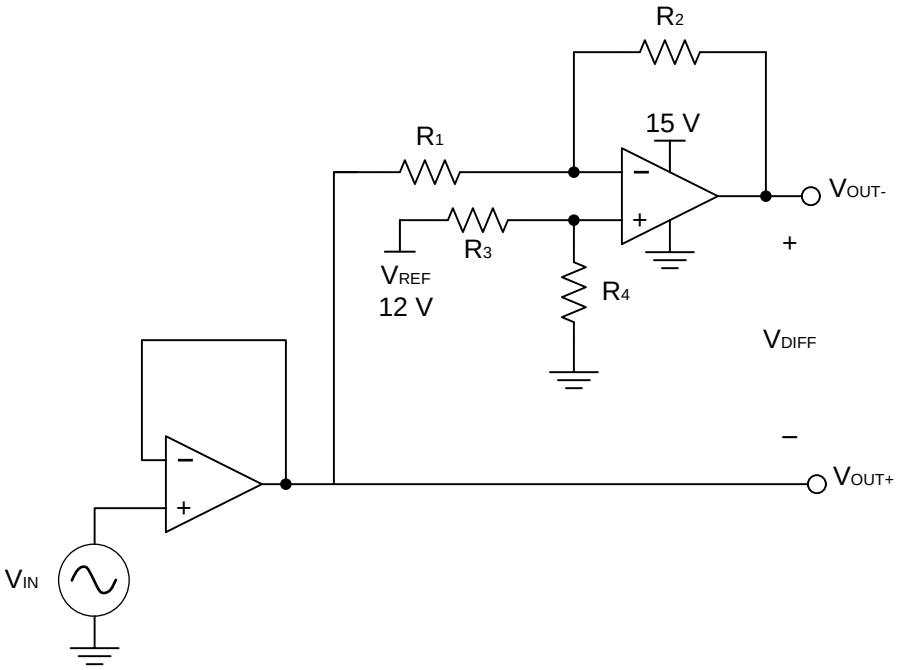
7.4 Device Functional Modes

The XDXL/4558 device is powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8 Application and Implementation

8.1 Typical Application

Some applications require differential signals. Figure 14 shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of ±8 V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 2 V to 10 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$.



Schematic for Single-Ended Input to Differential Output Conversion

Typical Application (continued)

8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential: ±8 V

8.1.2 Detailed Design Procedure

The circuit in Figure 14 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see Equation 1). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \tag{7}$$

8.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because XDXL/4558 has a bandwidth of 3 MHz, this circuit will only be able to process signals with frequencies of less than 3 MHz.

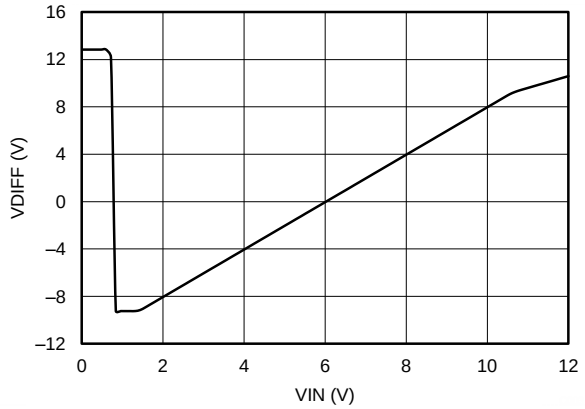
8.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

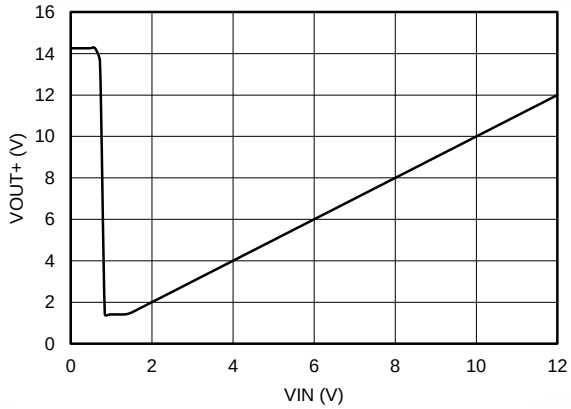
Typical Application (continued)

8.1.3 Application Curves

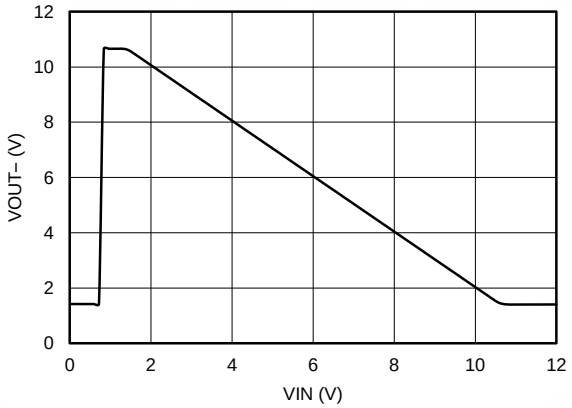
The measured transfer functions in Figure 15, Figure 16, and Figure 17 were generated by sweeping the input voltage from 0 V to 12 V. However, this design should only be used between 2 V and 10 V for optimum linearity.



Differential Output Voltage Node vs Input Voltage



Positive Output Voltage Node vs Input Voltage



Positive Output Voltage Node vs Input Voltage

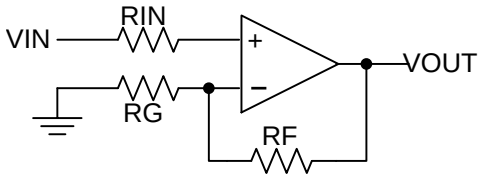
9 Layout

9.1 Layout Guidelines

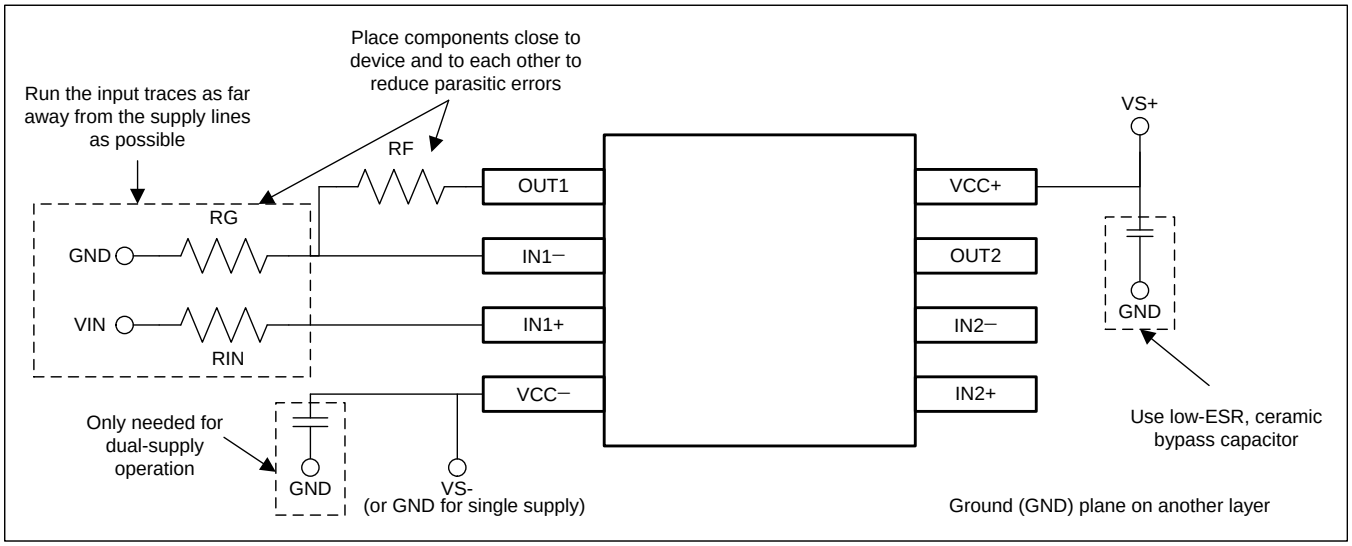
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.2 Layout Example



Operational Amplifier Schematic for Noninverting Configuration



Operational Amplifier Board Layout for Noninverting Configuration

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA

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