XL5532 SOP-8
XD5532 DIP-8

1 Features

- Equivalent Input Noise Voltage: 5 nV/√Hz Typ at 1 kHz
- Unity-Gain Bandwidth: 10 MHz Typ
- Common-Mode Rejection Ratio: 100 dB Typ
- High DC Voltage Gain: 100 V/mV Typ
- Peak-to-Peak Output Voltage Swing 26 V Typ With $V_{CC\pm}$ = ±15 V and R_L = 600 Ω
- High Slew Rate: 9 V/μs Typ

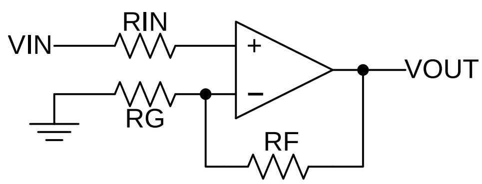
2 Applications

- AV Receivers
- Embedded PCs
- Netbooks
- Video Broadcasting and Infrastructure: Scalable Platforms
- DVD Recorders and Players
- Multichannel Video Transcoders
- Pro Audio Mixers

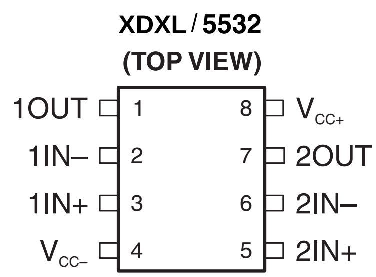
3 Description

The XDXL/5532 devices are high-performance operational amplifiers combining excellent DC and AC characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

4 Simplified Schematic



5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting Input
OUT1	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting Input
2OUT	7	O	Output
VCC+	8	—	Positive Supply
VCC-	4	—	Negative Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC+}	0	22	V
		V_{CC-}	–22	0	V
	Input voltage, either input(2)(3)		V_{CC-}	V_{CC+}	V
	Input current(4)		–10	10	mA
	Duration of output short circuit(5)		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
T_A	Operating free-air temperature	XDXL/5532	0	70	°C

6.4 Thermal Information

THERMAL METRIC(1)		XDXL/5532			UNIT
		D	P	PS	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	97	85	95	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.5 Electrical Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	T_A = 25°C		0.5	4	mV
			T_A = Full range[2]			5	
I_{IO}	Input offset current	T_A = 25°C			10	150	nA
		T_A = Full range[2]				200	
I_{IB}	Input bias current	T_A = 25°C			200	800	nA
		T_A = Full range[2]				1000	
V_{ICR}	Common-mode input-voltage range			±12	±13		V
V_{OPP}	Maximum peak-to-peak output-voltage swing	R_L ≥ 600 Ω, $V_{CC\pm}$ = ±15 V		24	26		V
A_{VD}	Large-signal differential-voltage amplification	R_L ≥ 600 Ω, V_O = ±10 V	T_A = 25°C	15	50		V/mV
			T_A = Full range[2]	10			
		R_L ≥ 2 kΩ, V_O±10 V	T_A = 25°C	25	100		
			T_A = Full range[2]	15			
A_{vd}	Small-signal differential-voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum output-swing bandwidth	R_L = 600 Ω, V_O = ±10 V			140		kHz
B_1	Unity-gain bandwidth	R_L = 600 Ω, C_L = 100 pF			10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	A_{VD} = 30 dB, R_L = 600 Ω, f = 10 kHz			0.3		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min		70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		80	100		dB
I_{OS}	Output short-circuit current			10	38	60	mA
I_{CC}	Total supply current	V_O = 0, No load			8	16	mA
	Crosstalk attenuation (V_{O1}/V_{O2})	V_{01} = 10 V peak, f = 1 kHz			110		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Full temperature ranges are: 0°C to 70°C for the XDXL/5532 devices.

6.6 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	XDXL/5532			XDXL/5532			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/μs
	Overshoot factor	V_I = 100 mV, R_L = 600 Ω, A_{VD} = 1, C_L = 100 pF		10			10		%
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

6.7 Typical Characteristics

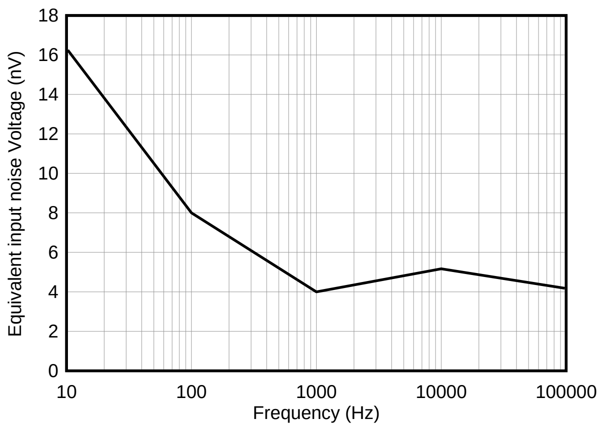


Figure 1. Equivalent Input Noise Voltage vs Frequency

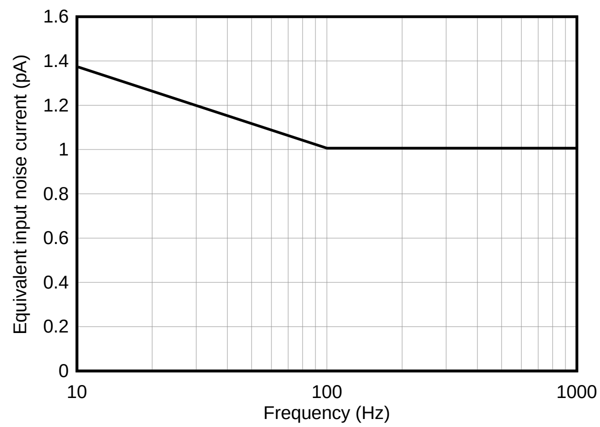


Figure 2. Equivalent Input Noise Current vs Frequency

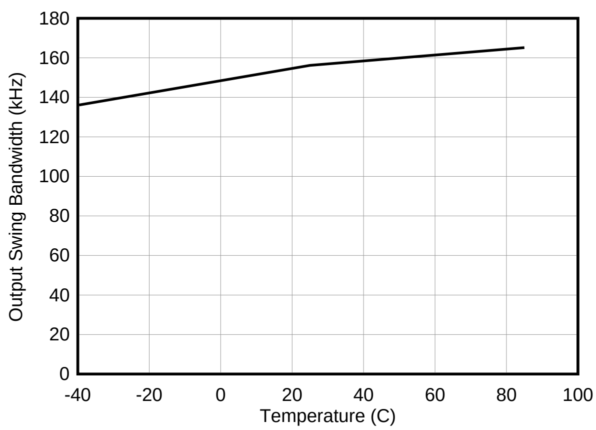


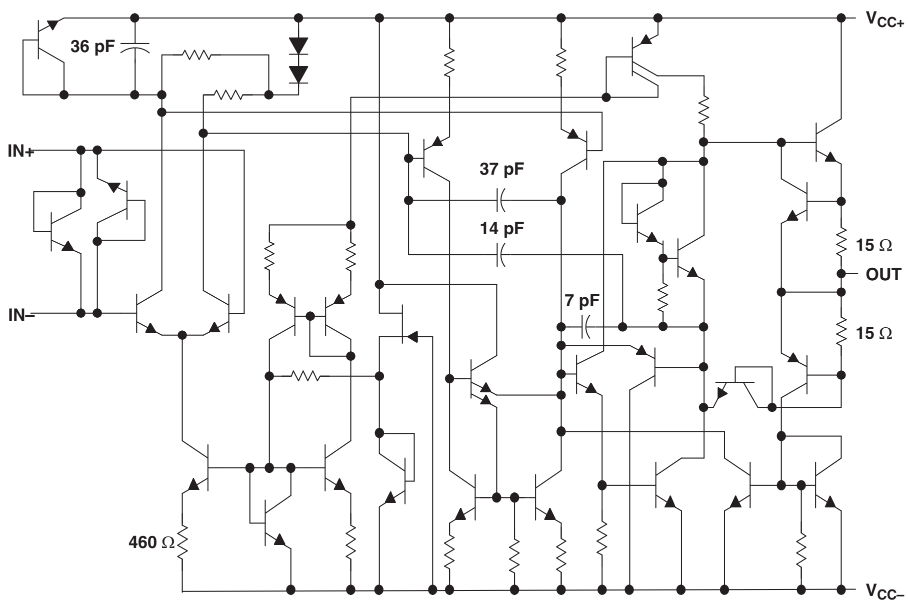
Figure 3. Output Swing Bandwidth vs Temperature at V_{CC} = ±10 V

7 Detailed Description

7.1 Overview

The XDXL/5532 devices are high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

7.2 Functional Block Diagram



Component values shown are nominal.

7.3 Feature Description

7.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The XDXL/5532 devices have a 10-MHz unity-gain bandwidth.

7.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR would be infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the XDXL/5532 devices is 100 dB.

7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The XDXL/5532 devices have a 9-V/ms slew rate.

7.4 Device Functional Modes

The XDXL/5532 devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8 Application and Implementation

8.1 Typical Application

Some applications require differential signals. Figure 4 shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of ±8 V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-}. Both V_{OUT+} and V_{OUT-} range from 2 V to 10 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and V_{OUT-}.

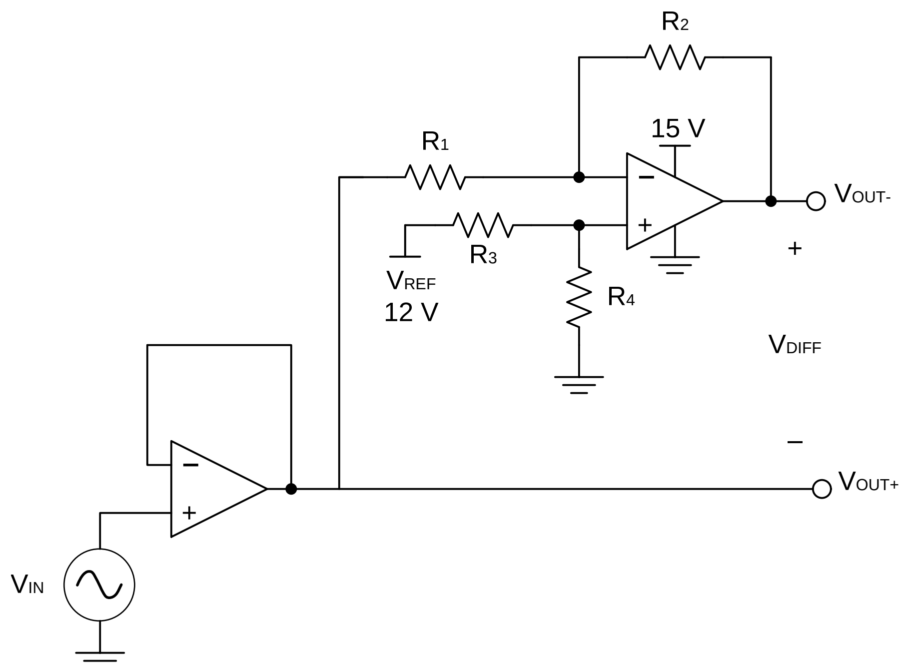


Figure 4. Schematic for Single-Ended Input to Differential Output Conversion

8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential: ±8 V

Typical Application (continued)

8.1.2 Detailed Design Procedure

The circuit in Figure 4 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} Equation 1. V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{out-} = V_{ref} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{in} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \quad (7)$$

8.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Since the 5532 has a bandwidth of 10 MHz, this circuit will only be able to process signals with frequencies of less than 10 MHz.

81.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

8.1.3 Application Curves

The measured transfer functions in Figure 5, Figure 6, and Figure 7 were generated by sweeping the input voltage from 0 V to 12V. However, this design should only be used between 2 V and 10 V for optimum linearity.

Typical Application (continued)

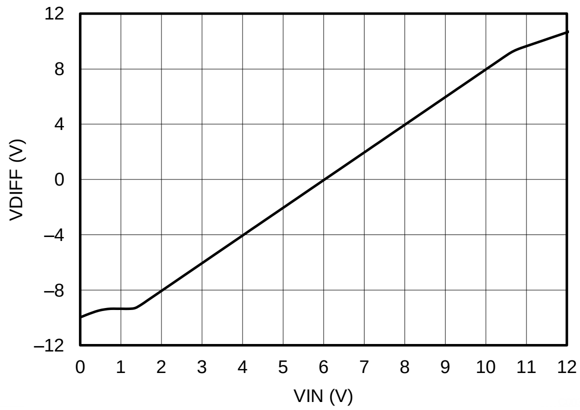


Figure 5. Differential Output Voltage vs Input Voltage

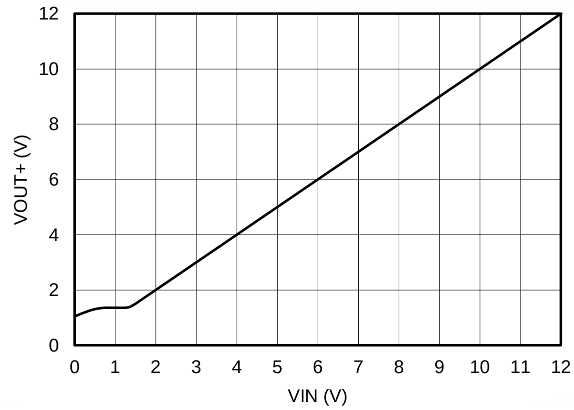


Figure 6. Positive Output Voltage Node vs Input Voltage

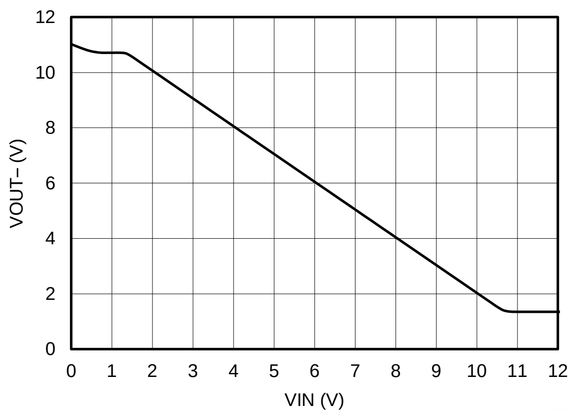


Figure 7. Positive Output Voltage Node vs Input Voltage

9 Power Supply Recommendations

The XDXL/5532 devices are specified for operation over the range of ±5 to ±15 V; many specifications apply from 0°C to 70°C (XDXL/5532) The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

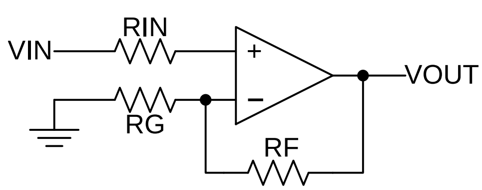


Figure 8. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

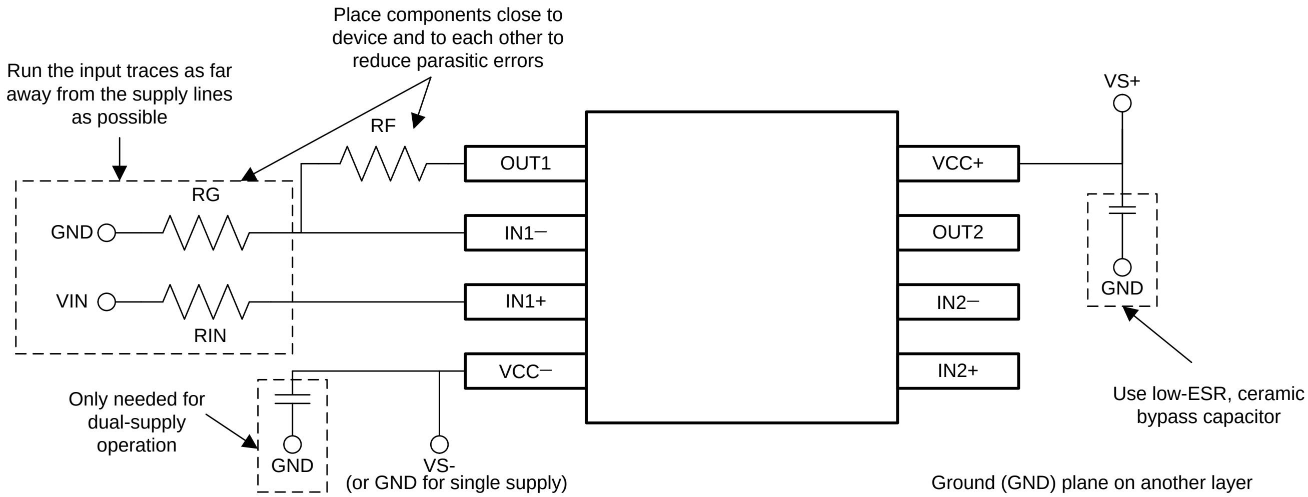
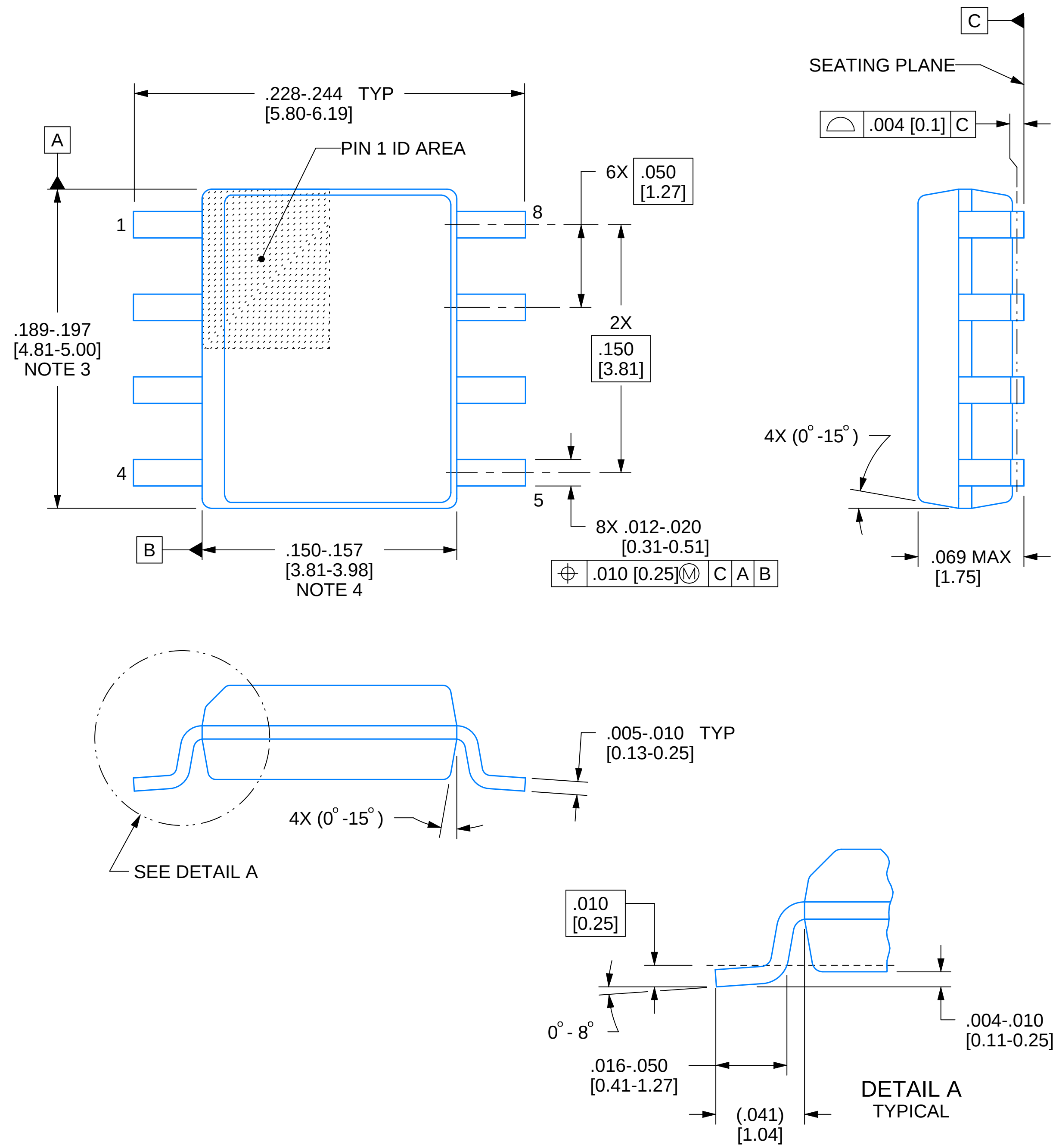


Figure 9. Operational Amplifier Board Layout for Noninverting Configuration

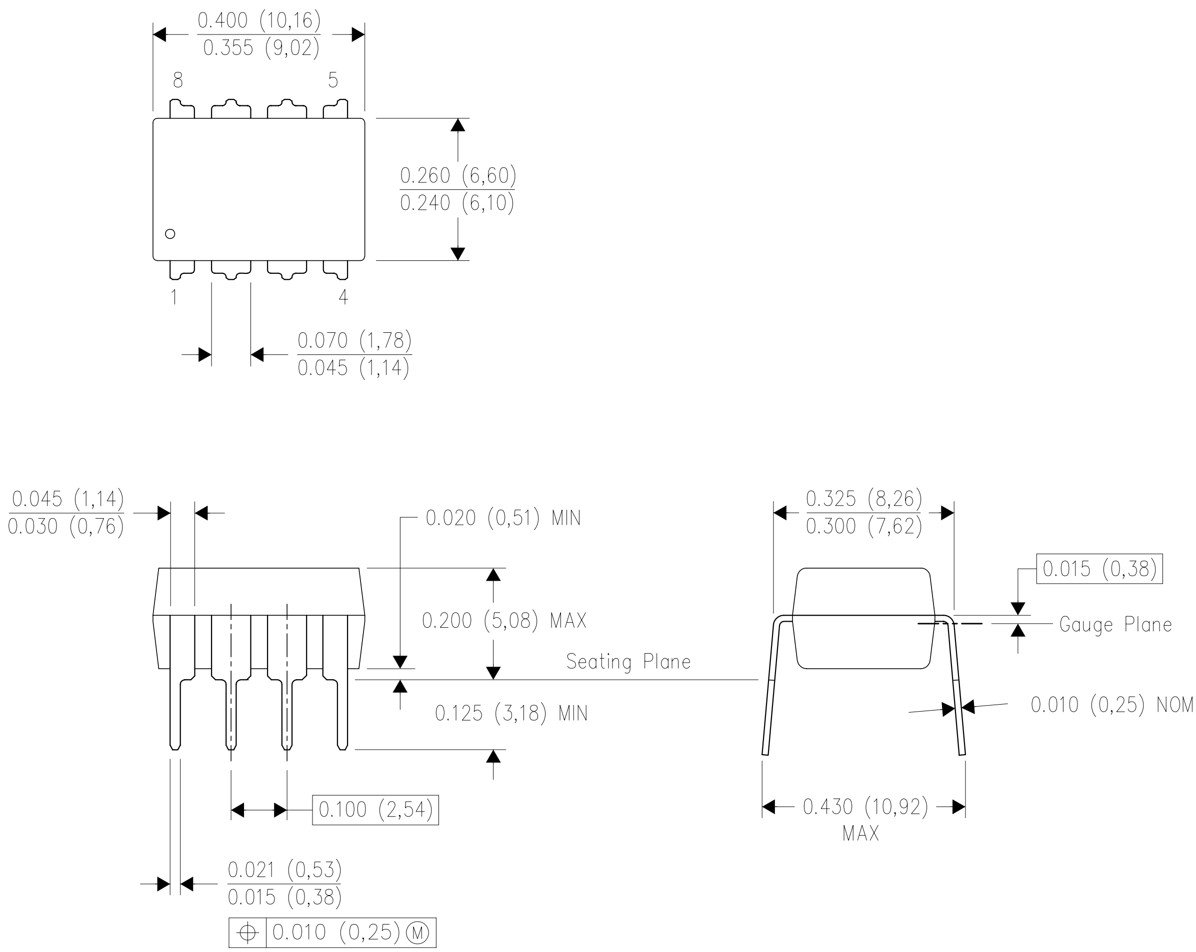
SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA