1. DESCRIPTION

The 74HC595TS and 74HC595 are low noise, low power, high speed COMS shift register capable of driving 15 LS-TTL loads.

The device consists of an 8-bit serial input, parallel output shift register and 8-bit D-type memory with tri-state output control. The shift register and memory are signalled by separate clocks. The shift register has built-in direct clear, serial inputs and serial outputs for cascading. The rising edge of the clock triggers the shift register and the memory. If the same clock provides the signal, the state of the shift register must be one pulse ahead of the memory.

The 74HC595TS and 74HC595 are compatible with the 74LS series. The device has diode protection between power and ground on all input pins to prevent static damage to the circuitry.

2. FEATURES

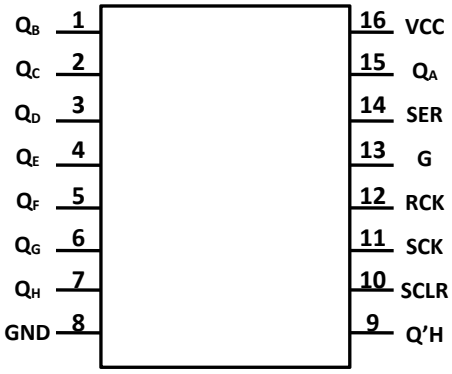
- Low quiescent current: 80uA max.
- Low input current: 1uA max.
- 8-bit serial input, parallel output shift register with memory function
- Wide operating voltage range: 2V-6V
- Cascadable
- Shift register can be cleared directly
- Shift clock frequency: DC-30MHz
- Package: TSSOP16 (XL74HC595TS) , SOP16(XL74HC595)

3. APPLICATIONS

- Shift register counters
- Sequential pulse generator
- Serial to parallel data conversion
- LED Driver

4. PIN CONFIGURATIONS AND FUNCTIONS

XL74HC595TS,XL74H595



(TOP VIEW)

Pin Functions

Pin	Name	I/O	Description
1	Q_B	DO	Tri-State Outputs
2	Q_C	DO	Tri-state outputs
3	Q_D	DO	Tri-state outputs
4	Q_E	DO	Tri-state outputs
5	Q_F	DO	Tri-state outputs
6	Q_G	DO	Tri-state outputs
7	Q_H	DO	Tri-state outputs
8	GND	P	Digital ground
9	Q'_H	DO	Serial data outputs
10	SCLR	DI	Shift register clear
11	SCK	DI	Data input clock
12	RCK	DI	Output register latch clock
13	G	DI	Output Enable
14	SER	DI	Data inputs
15	Q	DO	Tri-state outputs
16	VCC	P	Digital power supply

Logical Relationships:

RCK	SCK	SCLR	G	Function
×	×	×	H	QA -- QH Output high resistance state
×	×	L	L	Shift register clear Q'H =0
×	↑	H	L	Shift register store state: clock QN = QN-1, QA =SER
↑	×	H	L	Output memory latch shift register state

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
V_{CC}	Supply voltage range			-0.5	+7	V
I_{CC}	Power supply current			-	+70	mA
V_{IN}	DC Input Voltage			-1.5	VCC+1.5	V
V_{OUT}	DC Output Voltage			-0.5	VCC+0.5	V
I_{OK}, I_{IK}	Clamp Diode Current			-	+20	mA
I_{OUT}	DC Output Current			-	+35	mA
P_D	Power Consumption	DIP		600		mW
		SOP		500		
T_{STG}	Operating Ambient Temperature			-40	+85	V
T_{amb}	Storage Temperature			-65	+125	℃
T_L	welding temperature	10s	DIP	245		℃
			SOP	250		

5.2. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	2		6	V
V_{OUT}/V_{IN}	DC Input or output voltage	0		VCC	V
tr,tf	Input rise and fall times				
	VCC =2.0V			1000	ns
	VCC =4.5V		6	500	ns
	VCC =6.0V			400	ns

5.3. DC characteristics:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
DC Parameters 1 Tamb =-40°C ~ 85°C					
Input high level voltage (VIH)	VCC=2.0V	1.5	1.2		V
	VCC=4.5V	3.15	2.4		V
	VCC=6.0V	4.2	3.2		V
Input low level voltage (VIL)	VCC=2.0V		0.8	0.5	V
	VCC=4.5V		2.1	1.35	V
	VCC=6.0V		2.8	1.8	V
Output high level voltage (VOH)	Vi=VIH or VIL VCC=2.0VIO=-20uA	1.9	2.0		V
	Vi=VIH or VIL VCC=4.5VIO=-20uA	4.4	4.5		V
	Vi=VIH or VIL VCC=6.0VIO=-20uA	5.9	6.0		V
Q'H Output high level voltage (VOH)	Vi=VIH or VIL VCC=4.5VIO=-4.0mA	4.5	3.7		V
	Vi=VIH or VIL VCC=6.0VIO=-5.2mA	6	5.2		V
QA-QH Output high level voltage (VOH)	Vi=VIH or VIL VCC=4.5VIO=-6.0mA	4.5	3.7		V
	Vi=VIH or VIL VCC=6.0VIO=-7.8mA	6	5.2		V
Output Low Level Voltage (VOL)	Vi=VIH or VIL		0	0.1	V
	VCC=2.0V IO=20uA				
	Vi=VIH or VIL VCC=4.5VIO=20uA		0	0.1	V
	Vi=VIH or VIL VCC=6.0VIO=20uA		0	0.1	V
Q'H Output Low Level Voltage(VOL)	Vi=VIH or VIL VCC=4.5V IO=4.0mA		0.15	0.33	V
	Vi=VIH or VIL VCC=6.0V IO=5.2mA		0.16	0.33	
QA-QH Output Low Level Voltage(VOL)	Vi=VIH or VIL VCC=4.5V IO=6mA		0.15	0.33	V
	Vi=VIH or VIL VCC=6.0V IO=7.8mA		0.16	0.33	
Input Leakage Current (ILI)	VCC=6.0V Vi= VCC or GND			±0.1	uA
Tri-state output cut-off current(IOZ)	VCC=6.0V Vi=VIH or VIL Vo= VCC or GND			±0.5	uA
Quiescent Current (ICCQ)	VCC=6.0V Vi =VCC or GND IO=0			80	uA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
DC Parameters 2 Tamb =-40°C ~ 125°C					
Input high level voltage (VIH)	VCC=2.0V	1.5			V
	VCC=4.5V	3.15			V
	VCC=6.0V	4.2			V
Input low level voltage (VIL)	VCC=2.0V			0.5	V
	VCC=4.5V			1.35	V
	VCC=6.0V			1.8	V
Output high level voltage (VOH)	Vi=VIH or VIL VCC=2.0VIO=-20uA	1.9			V
	Vi=VIH or VIL VCC=4.5VIO =-20uA	4.4			V
	Vi=VIH or VIL VCC=6.0VIO=-20uA	5.9			V
Q'H Output high level voltage (VOH)	Vi=VIH or VIL VCC=4.5VIO=-4.0mA	3.7			V
	Vi=VIH or VIL VCC=6.0VIO=-5.2mA	5.2			V
QA-QH Output high level voltage (VOH)	Vi=VIH or VIL VCC=4.5VIO=-6.0mA	3.7			V
	Vi=VIH or VIL VCC=6.0VIO=-7.8mA	5.2			V
Output Low Level Voltage (VOL)	Vi=VIH or VIL VCC=2.0VIO=20uA			0.1	V
	Vi=VIH or VIL VCC=4.5VIO =20uA			0.1	
	Vi=VIH or VIL VCC=6.0VIO=20uA			0.1	V
	Vi=VIH or VIL VCC=4.5V IO=4mA			0.4	V
Q'H Output Low Level Voltage(VOL)	Vi=VIH or VIL VCC=6.0VIO=5.2mA			0.4	V
	Vi=VIH or VIL VCC=4.5V IO=6mA			0.4	
QA-QH Output Low Level Voltage(VOL)	Vi=VIH or VIL VCC=6.0VIO=7.8mA			0.4	V
	VCC=6.0V Vi= VCCor GND			±1	
Input Leakage Current (ILI)	VCC=6.0V Vi=VIHor VIL Vo= VCC or GND			±10	uA
Tri-state output cut-off current(IOZ)	VCC=6.0V Vi =VCCor GND IO=0			160	uA
Quiescent Current (ICCQ)	Vi=VIH or VIL VCC=6.0VIO=-5.2mA	5.2			uA

5.4. AC Characteristics:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AC Parameters 1 Tamb=25°C					
SCK/RCK Maximum operating frequency (fMAX)	VCC=2.0V	9	30		MHz
	VCC=4.5V	30	91		MHz
	VCC=6.0V	35	108		MHz
SCK to Q'H Maximum transmission delay (tPHL ,tPLH)(As shown in Fig. 1)	VCC=2.0V		52	160	ns
	VCC=4.5V		19	32	ns
	VCC=6.0V		15	27	ns
RCK to QA-QH Maximum transmission delay (tPHL ,tPLH) (as in Fig. 2)	VCC=2.0V		55	175	ns
	VCC=4.5V		20	35	ns
	VCC=6.0V		16	30	ns
G to QA-QH output enable maximum time (tPZH ,tPZL) (as Fig. 5)	VCC=2.0V		47	150	ns
	VCC=4.5V		17	30	ns
	VCC=6.0V		14	26	ns
G to QA-QH output disable max. Time (tPHZ ,tPLZ)(Figure 5)	VCC=2.0V		41	150	ns
	VCC=4.5V		15	30	ns
	VCC=6.0V		12	26	ns
SCK Pulse width (tw) (Fig. 1)	VCC=2.0V	75	17		ns
	VCC=4.5V	15	6		ns
	VCC=6.0V	13	5		ns
RCK pulse width (tw) (Fig. 2)	VCC=2.0V	75	11		ns
	VCC=4.5V	15	4		ns
	VCC=6.0V	13	3		ns
SCLR low level width (tw) (as in Fig. 4)	VCC=2.0V	75	17		ns
	VCC=4.5V	15	6		ns
	VCC=6.0V	13	5		ns
SCLR to Q'H Transmit Delay (tPHL) (as in Figure 4)	VCC=2.0V		47	175	ns
	VCC=4.5V		17	35	ns
	VCC=6.0V		14	30	ns
SCLR to SCK wait time (trem) (as in Figure 4)	VCC=2.0V	50	-19		ns
	VCC=4.5V	10	-7		ns
	VCC=6.0V	9	-6		ns
SER to SCK Establishment Time (tSU) (as in Figure 3)	VCC=2.0V	50	11		ns
	VCC=4.5V	10	4		ns
	VCC=6.0V	9	3		ns
SCK to RCK Establishment Time (tSU) (as in Figure 2)	VCC=2.0V	75	22		ns
	VCC=4.5V	15	8		ns
	VCC=6.0V	13	7		ns
SER to SCK hold time (tH) (as in Fig. 3) (as in Fig. 3)	VCC=2.0V	3	-6		ns
	VCC=4.5V	3	-2		ns
	VCC=6.0V	3	-2		ns

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AC Parameters 2 Tamb=-40°C ~ 85°C					
SCK/RCK Maximum operating frequency (fMAX)	VCC=2.0V	4.8			MHz
	VCC=4.5V	24			MHz
	VCC=6.0V	28			MHz
SCK to Q'H Maximum transmission delay (tPHL ,tPLH)(As shown in Fig. 1)	VCC=2.0V			200	ns
	VCC=4.5V			40	ns
	VCC=6.0V			34	ns
RCK to QA-QH Maximum transmission delay (tPHL ,tPLH) (as in Fig. 2)	VCC=2.0V			220	ns
	VCC=4.5V			44	ns
	VCC=6.0V			37	ns
G to QA-QH output enable maximum time (tPZH ,tPZL) (as Fig. 5)	VCC=2.0V			190	ns
	VCC=4.5V			38	ns
	VCC=6.0V			33	ns
G to QA-QH output disable max. Time (tPHZ ,tPLZ)(Figure 5)	VCC=2.0V			190	ns
	VCC=4.5V			38	ns
	VCC=6.0V			33	ns
SCK Pulse width (tw) (Fig. 1)	VCC=2.0V	95			ns
	VCC=4.5V	19			ns
	VCC=6.0V	16			ns
RCK pulse width (tw) (Fig. 2)	VCC=2.0V	95			ns
	VCC=4.5V	19			ns
	VCC=6.0V	16			ns
SCLR low level width (tw) (as in Fig. 4)	VCC=2.0V	95			ns
	VCC=4.5V	19			ns
	VCC=6.0V	16			ns
SCLR to Q'H Transmit Delay (tPHL) (as in Figure 4)	VCC=2.0V			220	ns
	VCC=4.5V			44	ns
	VCC=6.0V			37	ns
SCLR to SCK wait time (trem) (as in Figure 4)	VCC=2.0V	65			ns
	VCC=4.5V	13			ns
	VCC=6.0V	11			ns
SER to SCK Establishment Time (tSU) (as in Figure 3)	VCC=2.0V	65			ns
	VCC=4.5V	13			ns
	VCC=6.0V	11			ns
SCK to RCK Establishment Time (tSU) (as in Figure 2)	VCC=2.0V	95			ns
	VCC=4.5V	19			ns
	VCC=6.0V	16			ns
SER to SCK hold time (tH) (as in Fig. 3) (as in Fig. 3)	VCC=2.0V	3			ns
	VCC=4.5V	3			ns
	VCC=6.0V	3			ns

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AC Parameters 2 Tamb=-40°C ~ 125°C					
SCK/RCK Maximum operating frequency (fMAX)	VCC=2.0V	4			MHz
	VCC=4.5V	20			MHz
	VCC=6.0V	24			MHz
SCK to Q'H Maximum transmission delay (tPHL ,tPLH)(As shown in Fig. 1)	VCC=2.0V			240	ns
	VCC=4.5V			48	ns
	VCC=6.0V			41	ns
RCK to QA-QH Maximum transmission delay (tPHL ,tPLH) (as in Fig. 2)	VCC=2.0V			265	ns
	VCC=4.5V			53	ns
	VCC=6.0V			45	ns
G to QA-QH output enable maximum time (tPZH ,tPZL) (as Fig. 5)	VCC=2.0V			225	ns
	VCC=4.5V			45	ns
	VCC=6.0V			38	ns
G to QA-QH output disable max. Time (tPHZ ,tPLZ)(Figure 5)	VCC=2.0V			225	ns
	VCC=4.5V			45	ns
	VCC=6.0V			38	ns
SCK Pulse width (tw) (Fig. 1)	VCC=2.0V	110			ns
	VCC=4.5V	22			ns
	VCC=6.0V	19			ns
RCK pulse width (tw) (Fig. 2)	VCC=2.0V	110			ns
	VCC=4.5V	22			ns
	VCC=6.0V	19			ns
SCLR low level width (tw) (as in Fig. 4)	VCC=2.0V	110			ns
	VCC=4.5V	22			ns
	VCC=6.0V	19			ns
SCLR to Q'H Transmit Delay (tPHL) (as in Figure 4)	VCC=2.0V			265	ns
	VCC=4.5V			53	ns
	VCC=6.0V			45	ns
SCLR to SCK wait time (trem) (as in Figure 4)	VCC=2.0V	75			ns
	VCC=4.5V	15			ns
	VCC=6.0V	13			ns
SER to SCK Establishment Time (tSU) (as in Figure 3)	VCC=2.0V	75			ns
	VCC=4.5V	15			ns
	VCC=6.0V	13			ns
SCK to RCK Establishment Time (tSU) (as in Figure 2)	VCC=2.0V	110			ns
	VCC=4.5V	22			ns
	VCC=6.0V	19			ns
SER to SCK hold time (tH) (as in Fig. 3) (as in Fig. 3)	VCC=2.0V	3			ns
	VCC=4.5V	3			ns
	VCC=6.0V	3			ns

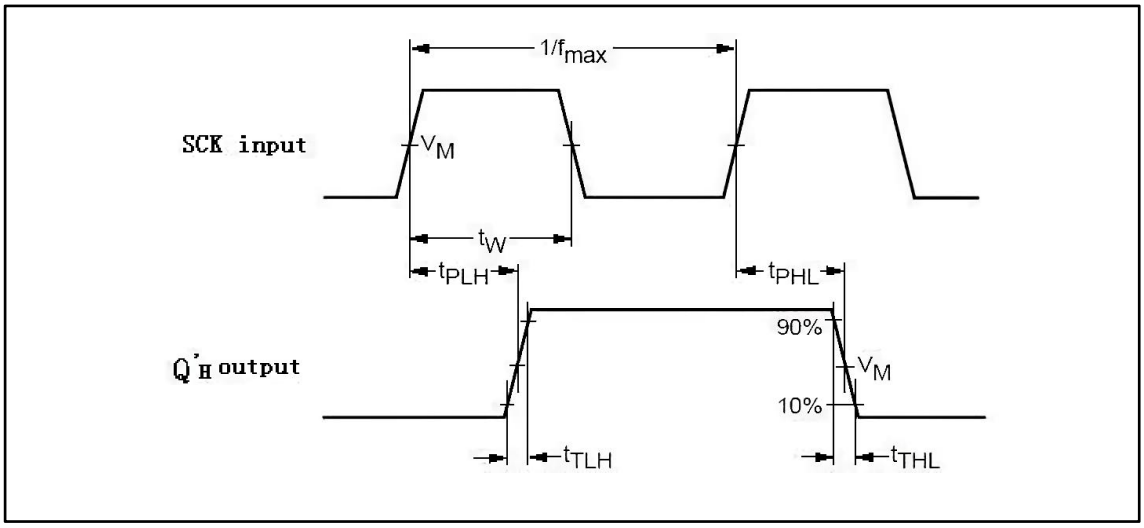


Figure 1: SCK to Q'H transmission delay (t_{PHL} ,t_{PLH}) and SCK pulse width (tw)

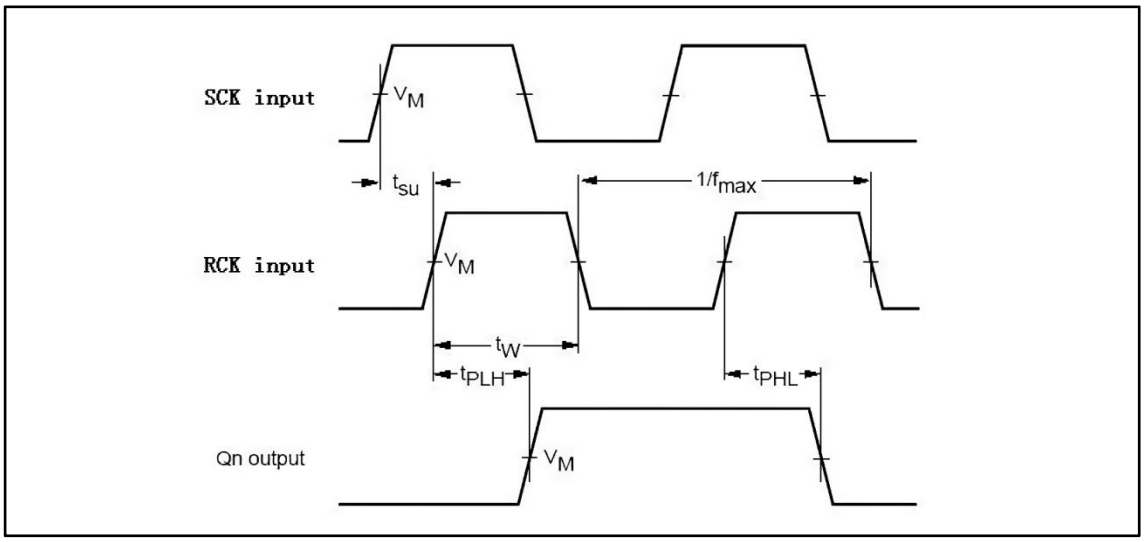


Figure 2: RCK to QA-QH Transmission Delay (t_{PHL} ,t_{PLH}) and RCK Pulse Width (tw) and SCK to RCK Establishment Time (t_{SU})

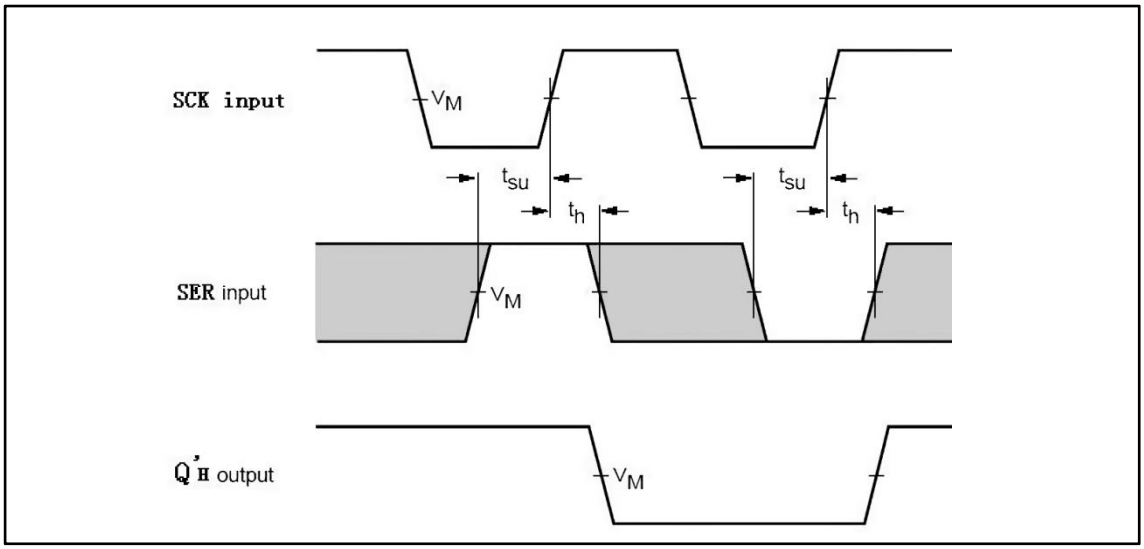


Figure 3: SER to SCK establishment time (t_{SU}) and SER to SCK hold time (t_H)

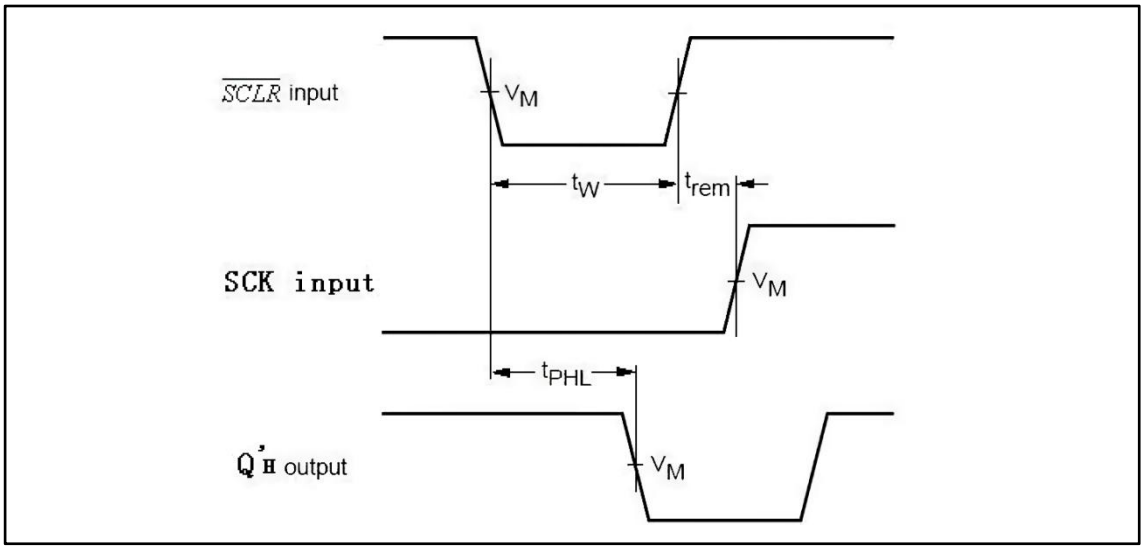


Figure 4: SCLR low level width (tw) and S C L R to Q'H transmission delay (t_{PHL}) and S C L R to SCK wait time (trem)

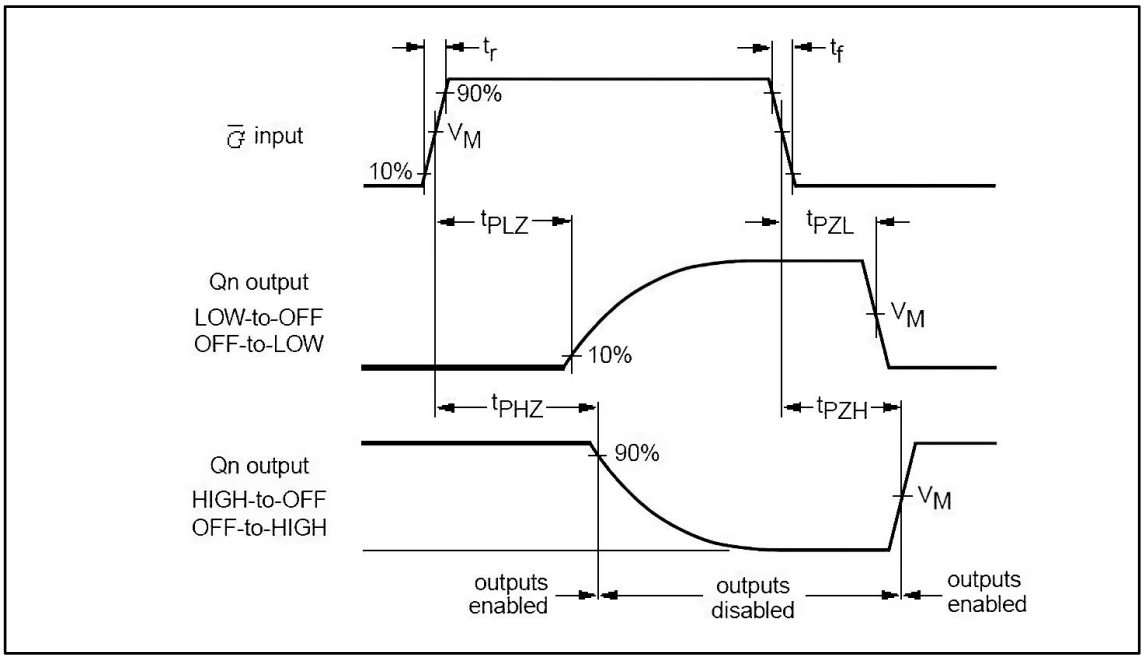
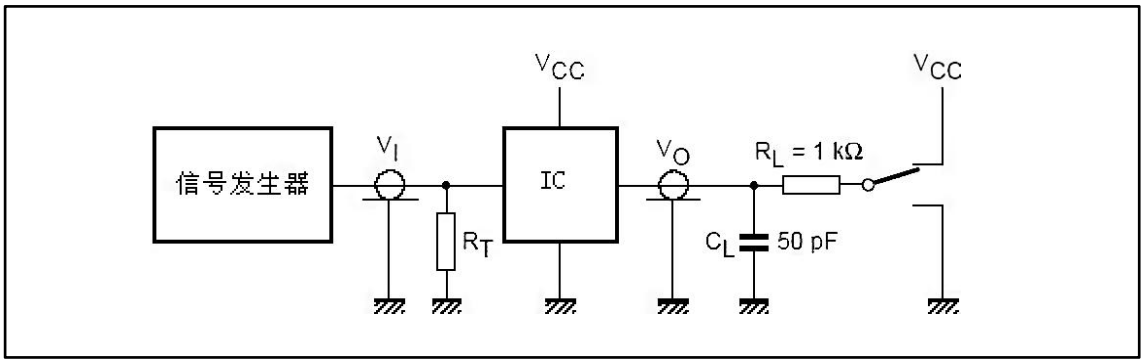


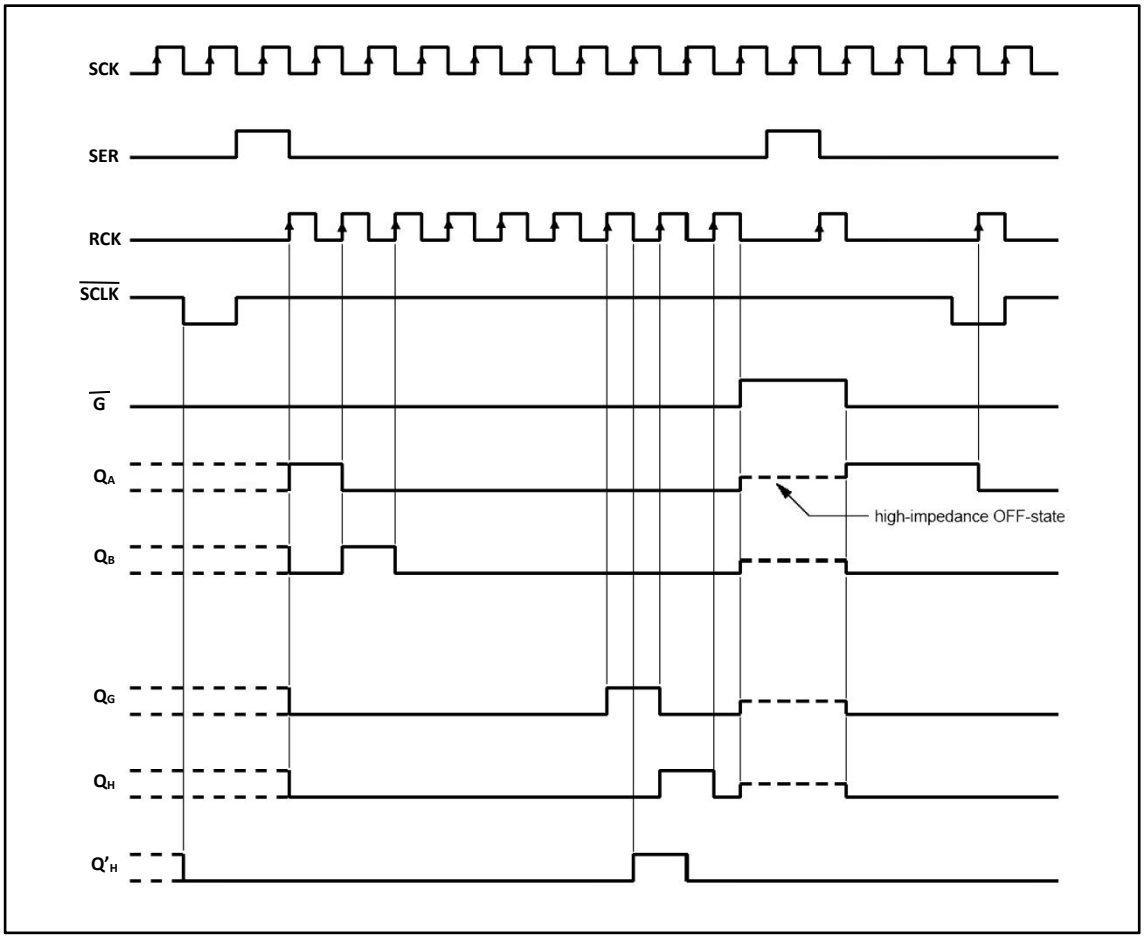
Figure 5: G to QA-QH output enable time (t_{PZH} ,t_{PZL}) and G to QA-QH output disable time (t_{PHZ} ,t_{PLZ})



Test	Switch Selection Status
tPLH/tPHL	open
tPLZ/tPZL	VCC
tPHZ/tPZH	GND

Notes:
1、RL：load resistance
2、CL：Load capacitance
3、RT：port resistance matching with the output impedance of signal generator

5.5. Timing Diagram



6. ORDERING INFORMATION

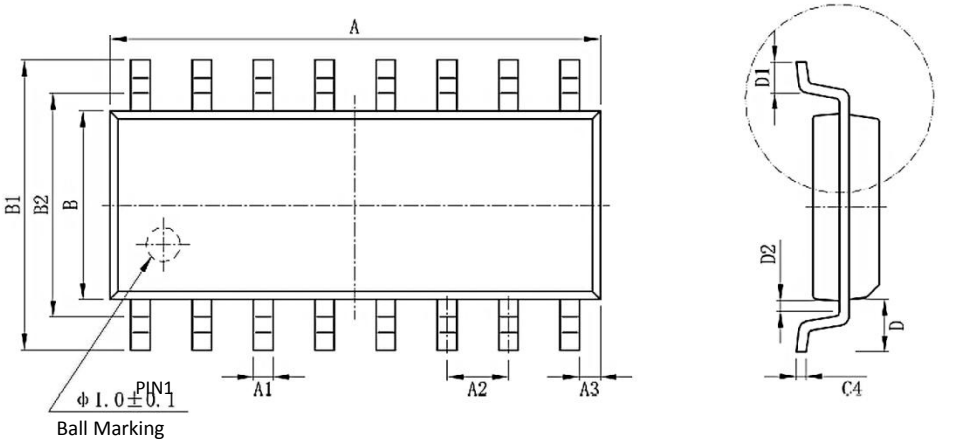
Ordering Information

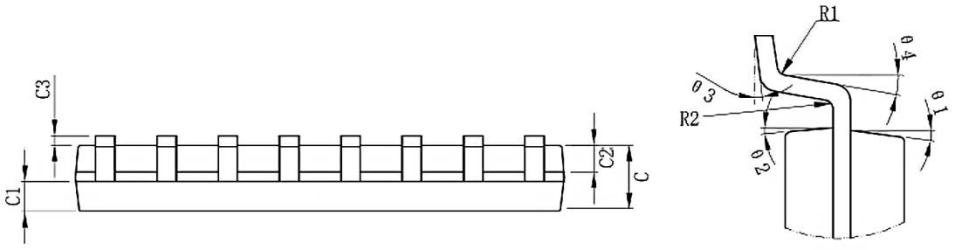
Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL74HC595TS	HC595TS	TSSOP16	5.00 * 3.90	- 40 to +85	MSL3	T&R	2500
XL74HC595	XL74HC595	SOP16	10.00 * 3.95	- 40 to +85	MSL3	T&R	2500

7. DIMENSIONAL DRAWINGS

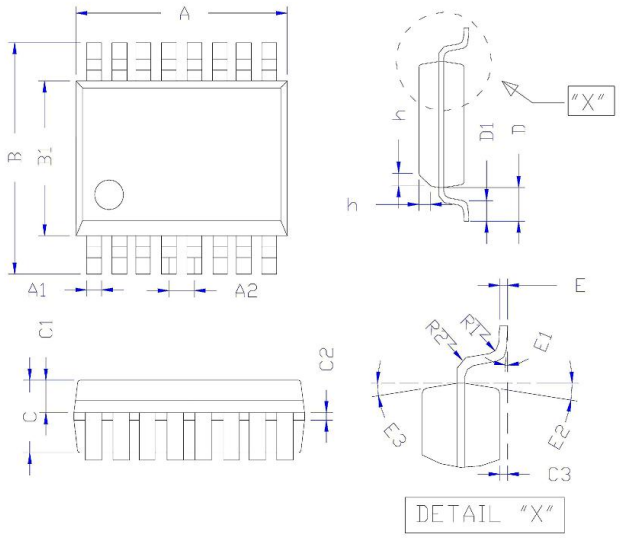
SOP16

Size / Mark	Min（mm）	Max（mm）	Size / Mark	Min（mm）	Max（mm）
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.40	1.60	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.05	0.25			





TSSOP16



SYM	MIN	NOM	MAN
A	4.95	5.00	5.05
A1	0.20	0.22	0.24
A2	0.60	0.65	0.70
B	5.70	6.00	6.30
B1	3.80	3.90	4.00
C	0.95	1.00	1.05
C1	0.40	0.41	0.42
C2	0.05	0.15	0.25
C3	0.02	0.08	0.10
D	0.85	1.05	1.25
D1	0.40	0.65	0.85
E	0.15	0.20	0.25
E1	0℃		8℃
h	0.30	0.40	0.50

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