1. DESCRIPTION

The XD/XL74HC597 is an 8-bit shift register with input flip-flops. It consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface in puts to voltages in excess of V_{CC}.

2. FEATURES

- Input levels:

  For XD/XL74HC597: CMOS level

  8-bit parallel storage register inputs

  Shift register has direct overriding load and clear

- Three kind of available packages:

  SOP16 (XL74HC597)

  TSSOP16 (XL74HC597-TS)

  DIP16 (XD74HC597)

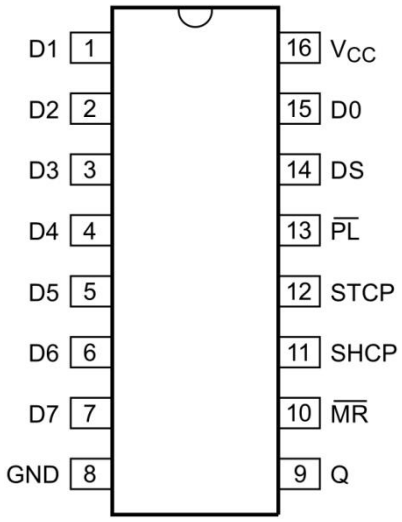
- ESD protection:

  HBM EIA/JESD22-A114F exceeds 2000 V

  MM EIA/JESD22-A115-A exceeds 200 V

3. PIN CONFIGURATIONS AND FUNCTIONS

XL74HC597
XL74HC597-TS
XD74HC597



(TOP VIEW)

Pin description

Symbol	Pin	Description
GND	8	ground (0 V)
Q	9	serial data output
$\overline{MR}$	10	asynchronous master reset input (active LOW)
SHCP	11	shift register clock input (LOW-to-HIGH, edge-triggered)
STCP	12	storage register clock input (LOW-to-HIGH, edge-triggered)
$\overline{PL}$	13	parallel load input (active LOW)
DS	14	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	15, 1, 2, 3, 4, 5, 6, 7	parallel data inputs
V_{CC}	16	supply voltage

4. FUNCTIONAL DIAGRAM

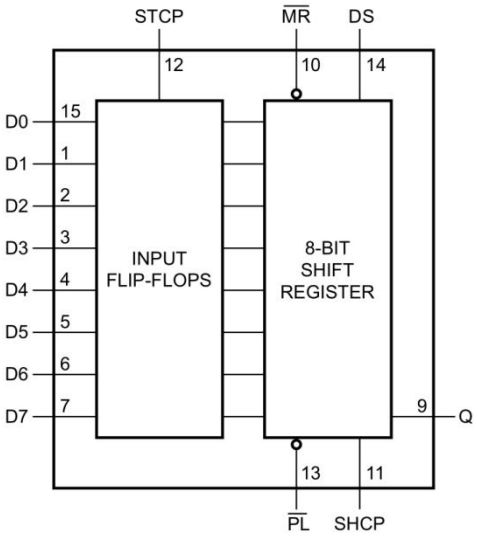


Fig 4-1. Functional diagram

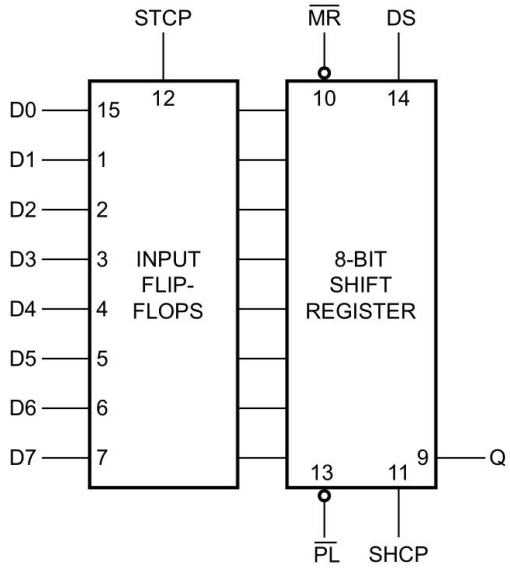


Fig 4-2. Logic symbol

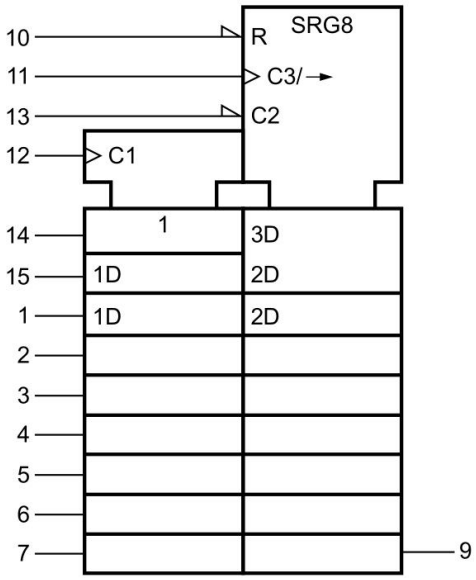


Fig 4-3. IEC Logic symbol

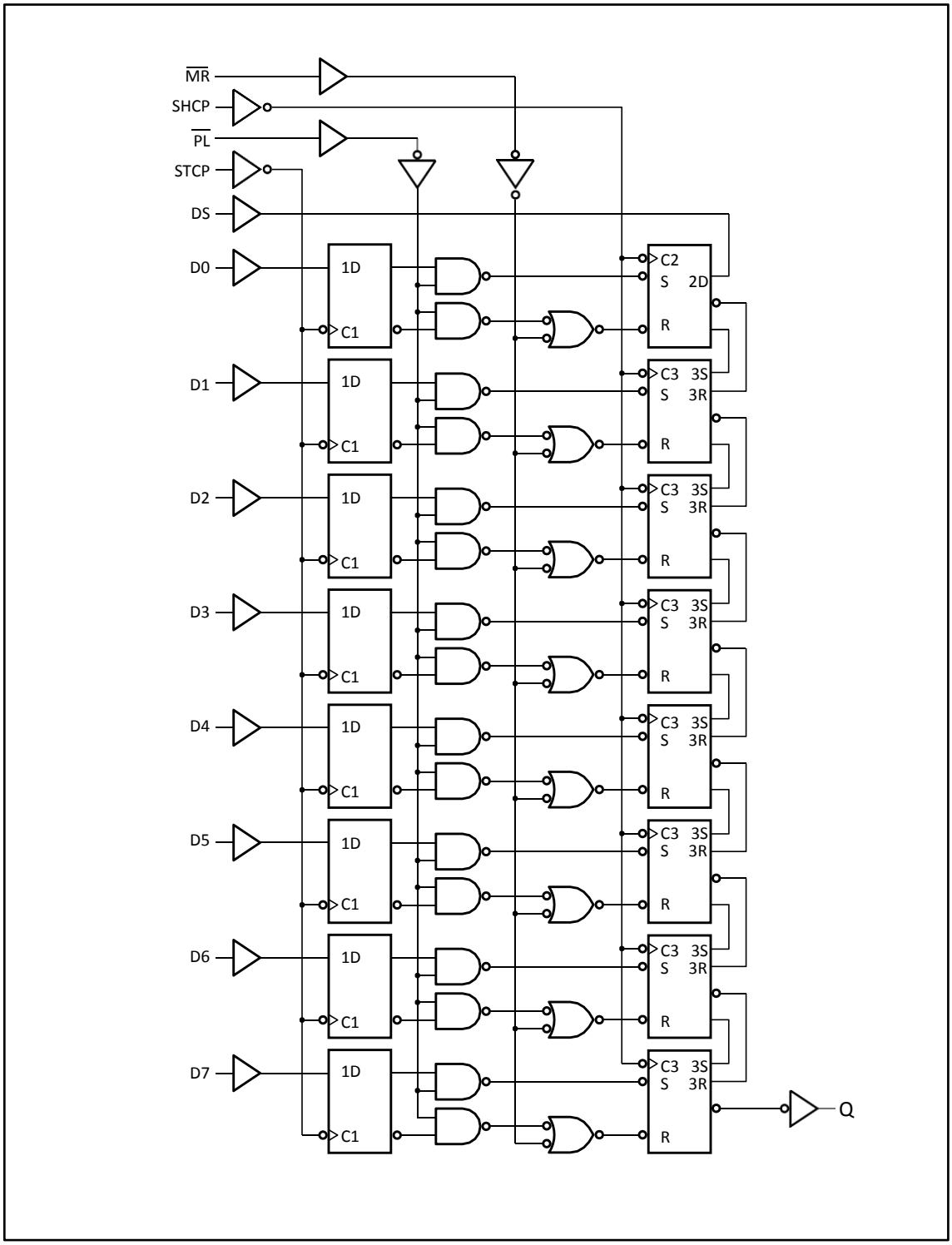


Fig 4-4. Logic diagram

5. FUNCTIONAL DESCRIPTION

Table 5-1. function table

Inputs				Function
STCP	SHCP	PL	MR	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Qn = Qn–1, Q0 = DS

[1] H = HIGH voltage level.

L = LOW voltage level.

X = don't care.

↑ = positive-going transition.

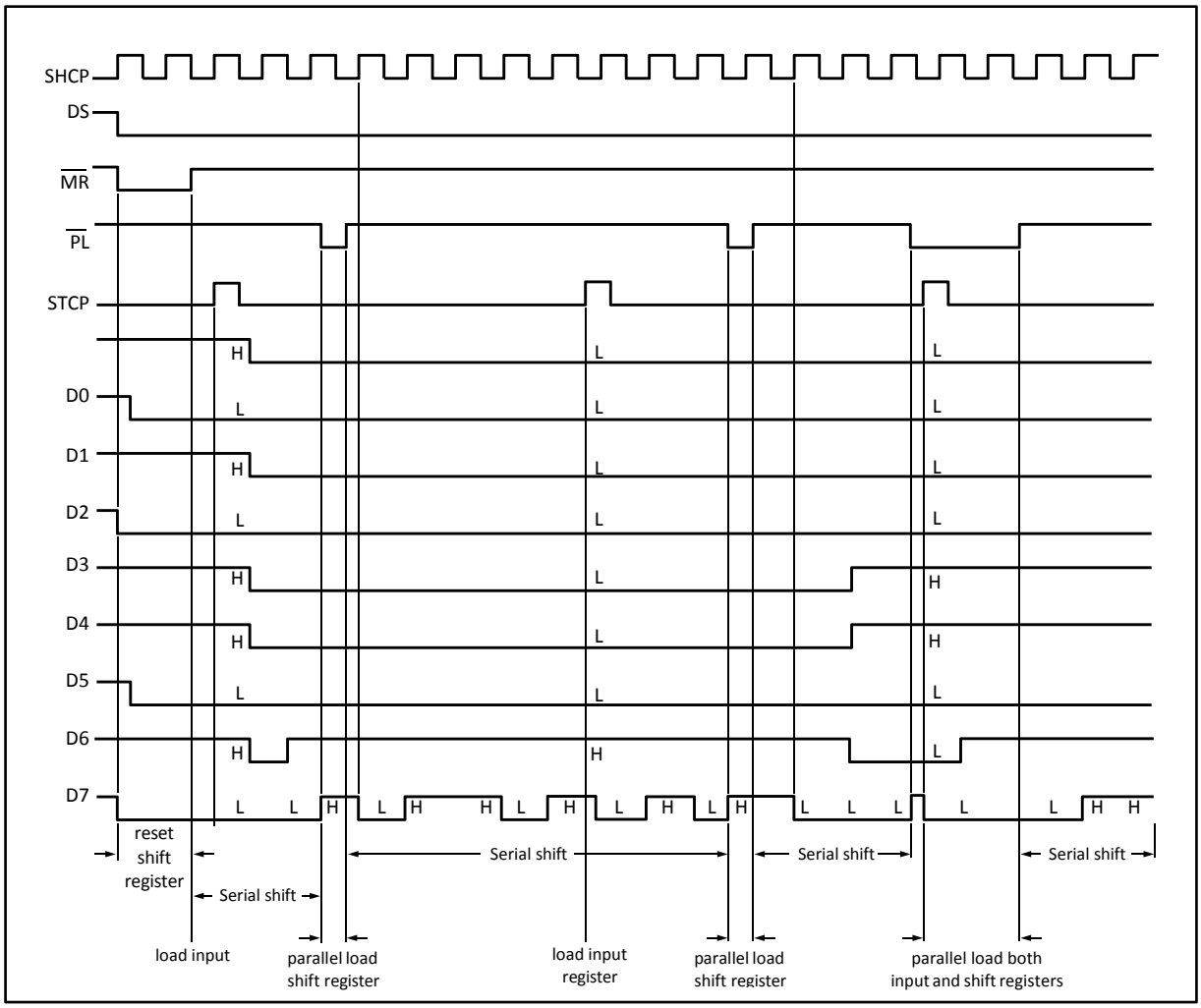


Fig 5-1. Timing diagram

6. SPECIFICATIONS

6.1. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−50	+150	°C
P_{tot}	total power dissipation	DIP16 package	-	750	mW
		SOP16 package	-	500	mW
		TSSOP16 package		450	mW

[1] For DIP16 package: Ptot derates linearly with 12 mW/K above 70 °C.

[2] For SO16: Ptot derates linearly with 8 mW/K above 70 °C.

For TSSOP16 packages: Ptot derates linearly with 5.5 mW/K above 60 °C.

6.2. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	XD/XL74HC597			Unit
			Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	700	ns/V
		V_{CC} = 4.5 V	-	-	200	ns/V
		V_{CC} = 6.0 V	-	-	120	ns/V

6.3. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
XD/XL74HC597								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	12	-	90.0	μA
C_I	input capacitance		-	3.5	-	-	-	pF

6.4. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); CL = 50 pF unless otherwise specified; for test circuit, see Figure 7-7.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
XD/XL74HC597								
t_{pd}	propagation delay	SHCP to Q; see Figure 7-1						
		V_{CC} = 2.0 V	-	55	175	-	220	ns
		V_{CC} = 4.5 V	-	20	35	-	44	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	ns
		V_{CC} = 6.0 V	-	16	30	-	37	ns
		MR to Q; see Figure 7-2						
		V_{CC} = 2.0 V	-	58	175	-	220	ns
		V_{CC} = 4.5 V	-	21	35	-	44	ns
		V_{CC} = 6.0 V	-	17	30	-	37	ns
		STCP to Q; see Figure 7-1						
		V_{CC} = 2.0 V	-	80	250	-	315	ns
		V_{CC} = 4.5 V	-	29	50	-	63	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	25	-	-	-	ns
		V_{CC} = 6.0 V	-	23	43	-	54	ns
		PL to Q; see Figure 7-3						
		V_{CC} = 2.0 V	-	69	215	-	270	ns
		V_{CC} = 4.5 V	-	25	43	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	ns
		V_{CC} = 6.0 V	-	20	37	-	46	ns
t_t	transition time	see Figure 7-3						
		V_{CC} = 2.0 V	-	19	75	-	95	ns
		V_{CC} = 4.5 V	-	7	15	-	19	ns
		V_{CC} = 6.0 V	-	6	13	-	16	ns
t_W	pulse width	STCP HIGH or LOW; see Figure 7-1						
		V_{CC} = 2.0 V	80	11	-	100	-	ns
		V_{CC} = 4.5 V	16	4	-	20	-	ns
		V_{CC} = 6.0 V	14	3	-	17	-	ns
		SHCP HIGH or LOW; see Figure 7-1						
		V_{CC} = 2.0 V	80	14	-	100	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	ns
		MR LOW; see Figure 7-2						
		V_{CC} = 2.0 V	80	22	-	100	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	ns
		PL LOW; see Figure 7-3						
		V_{CC} = 2.0 V	80	22	-	100	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Figure 7-4						
		V_{CC} = 2.0 V	60	-3	-	75	-	ns
		V_{CC} = 4.5 V	12	-1	-	15	-	ns
		V_{CC} = 6.0 V	10	-1	-	13	-	ns
t_{su}	set-up time	Dn to STCP; see Figure 7-5						
		V_{CC} = 2.0 V	60	8	-	75	-	ns
		V_{CC} = 4.5 V	12	3	-	15	-	ns
		V_{CC} = 6.0 V	10	2	-	13	-	ns
		DS to SHCP; see Figure 7-5						
		V_{CC} = 2.0 V	60	11	-	75	-	ns
		V_{CC} = 4.5 V	12	4	-	15	-	ns
		V_{CC} = 6.0 V	10	3	-	13	-	ns
		$\overline{PL}$ to SHCP; see Figure 7-6						
		V_{CC} = 2.0 V	60	11	-	75	-	ns
		V_{CC} = 4.5 V	12	4	-	15	-	ns
		V_{CC} = 6.0 V	10	3	-	13	-	ns
t_h	hold time	Dn to STCP; see Figure 7-6						
		V_{CC} = 2.0 V	5	-3	-	5	-	ns
		V_{CC} = 4.5 V	5	-1	-	5	-	ns
		V_{CC} = 6.0 V	5	-1	-	5	-	ns
		$\overline{PL}$, DS to SHCP; see Figure 7-6						
		V_{CC} = 2.0 V	5	-6	-	5	-	ns
		V_{CC} = 4.5 V	5	-2	-	5	-	ns
		V_{CC} = 6.0 V	5	-2	-	5	-	ns
f_{max}	maximum frequency	SHCP; see Figure 7-1						
		V_{CC} = 2.0 V	6.0	29	-	4.8	-	MHz
		V_{CC} = 4.5 V	30	87	-	24	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	96	-	-	-	MHz
		V_{CC} = 6.0 V	35	104	-	28	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	29	-	-	-	pF

[1] tpd is the same as tPLH and tPHL.

[2] t_t is the same as tTHL and tTLH.

[3] CPD is used to determine the dynamic power dissipation (PD in µW).

$P_D = C_{PD}\ V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

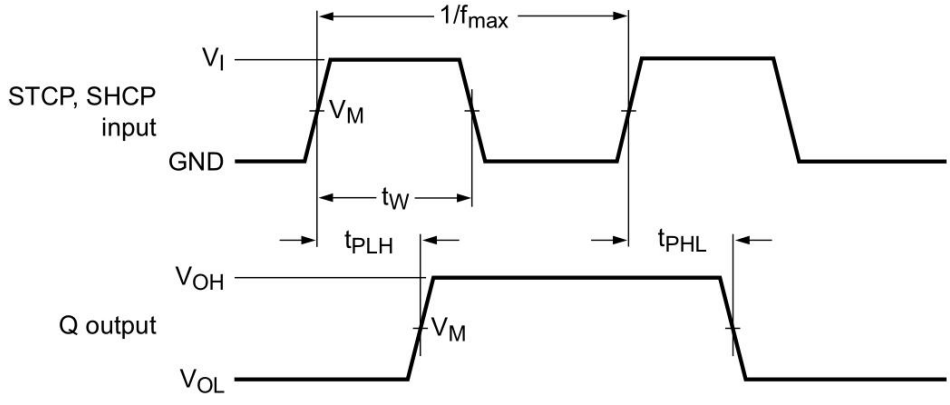
C_L = output load capacitance in pF;

VCC = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

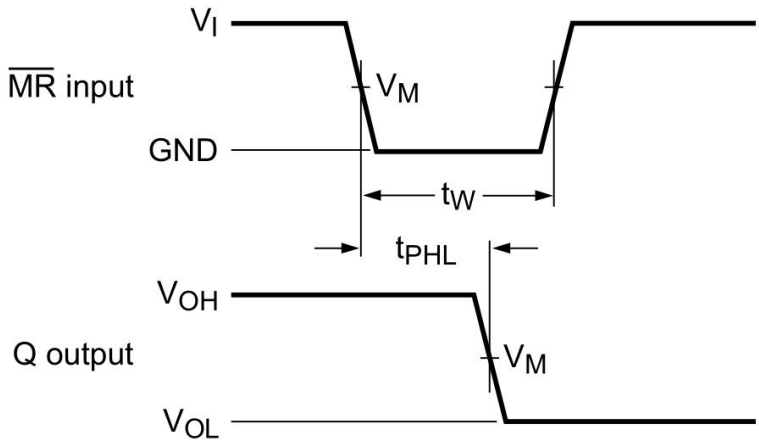
7. Waveforms



Measurement points are given in Table 7-1.

V OL and V OH are typical voltage output levels that occur with the output load.

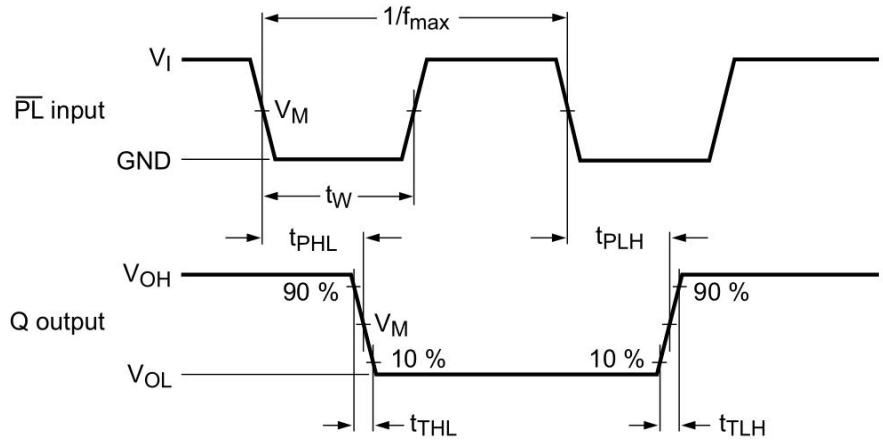
Fig 7-1. Shift clock and storage clock inputs to output, propagation delays, pulse widths and maximum clock frequency



Measurement points are given in Table 7-1.

V OL and V OH are typical voltage output levels that occur with the output load.

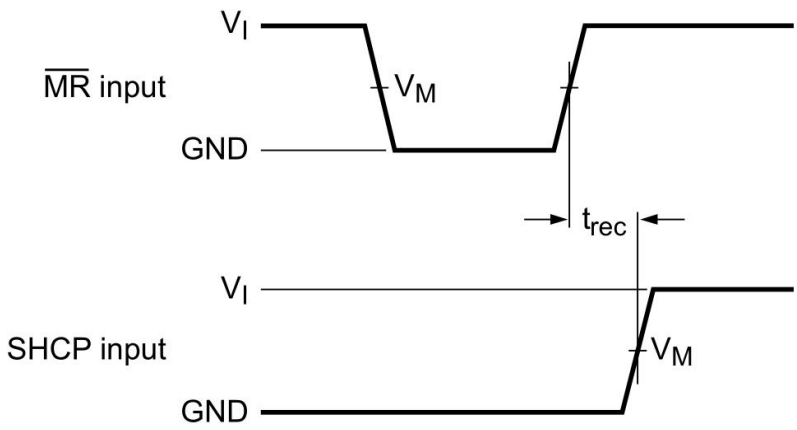
Fig 7-2. input (MR) to (Q), output propagation delays and (MR) pulse width



Measurement points are given in Table 7-1.

V OL and V OH are typical voltage output levels that occur with the output load.

Fig 7-3. Input (PL) to (Q), output propagation delays, PL pulse width and output transition times



Measurement points are given in Table 7-1.

Fig 7-4. Input (MR) to shift clock (SHCP) and storage clock (STCP) recovery times

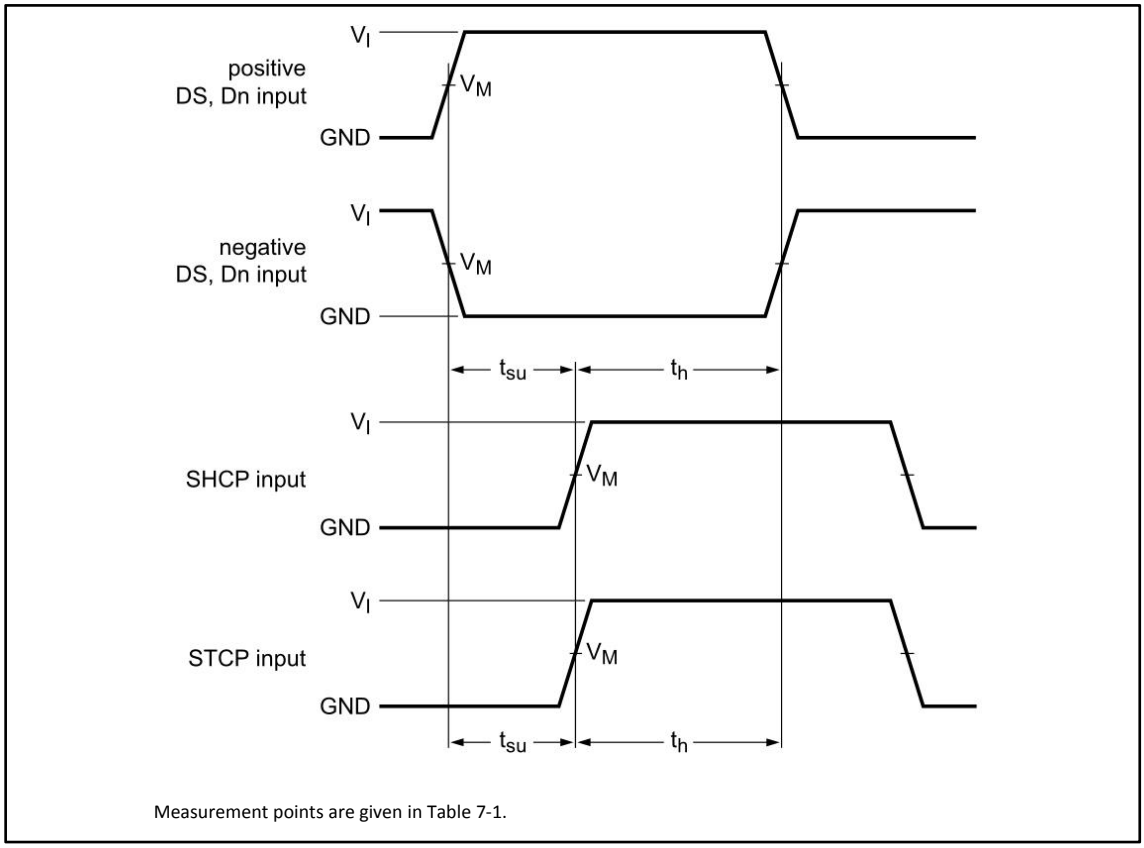


Fig 7-5. Hold and set-up times for (DS), (Dn) inputs to (SHCP), (STCP) inputs

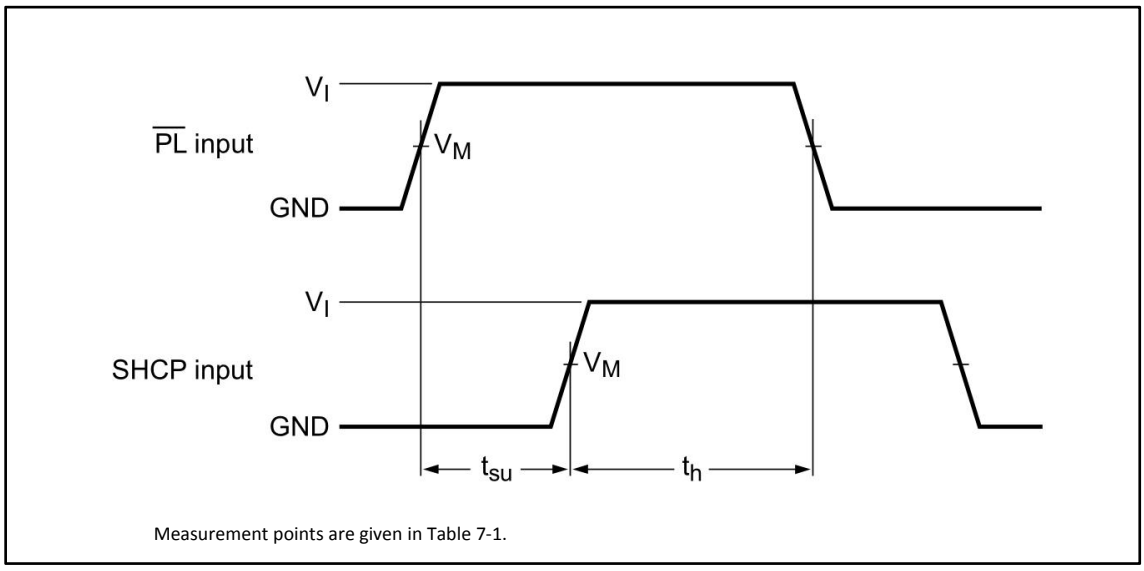
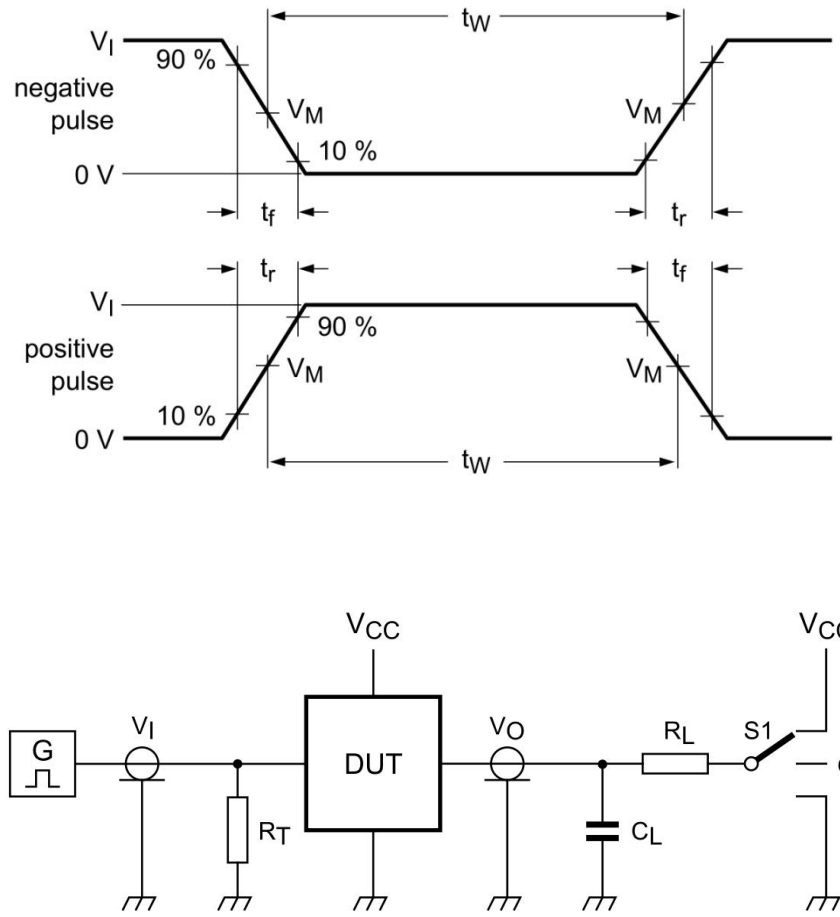


Fig 7-6. Set-up times for (PL) input to (SHCP) input

Table 7-1. Measurement points

Type	Input		Output
	V_M	V_I	V_M
XL74HC597 XL74HC597-TS XD74HC597	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$



Test data is given in Table 7-2.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S_1 = Test selection switch.

Fig 7-7. Test circuit for measuring switching times

Table 7-2. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
XL74HC597 XL74HC597-TS XD74HC597	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

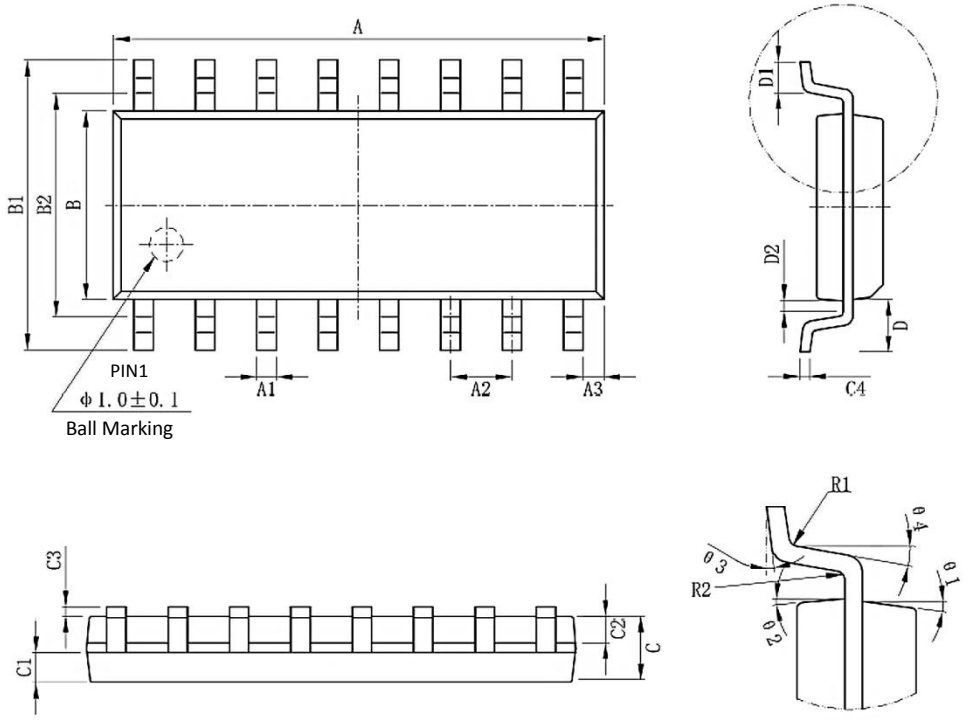
8. ORDERING INFORMATION

Ordering Information							
Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL74HC597	XL74HC597	SOP16	10.00 * 3.95	- 40 to 85	MSL3	T&R	2500
XL74HC597-TS	XL74HC597-TS	TSSOP16	5.00 * 3.90	- 40 to 85	MSL3	T&R	2500
XD74HC597	XD74HC597	DIP16	19.05 * 6.35	- 40 to 85	MSL3	Tube 25	1000

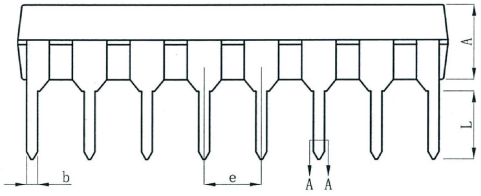
9. DIMENSIONAL DRAWINGS

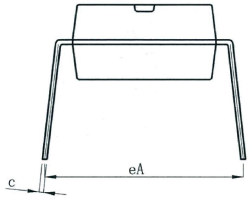
SOP16

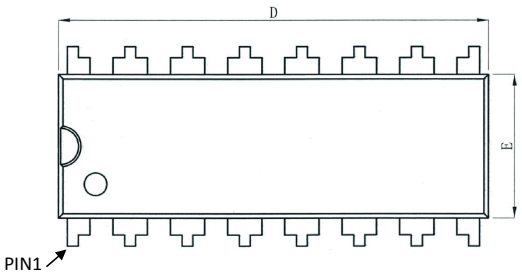
Size / Mark	Min (mm)	Max (mm)	Size / Mark	Min (mm)	Max (mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.40	1.60	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.05	0.25			

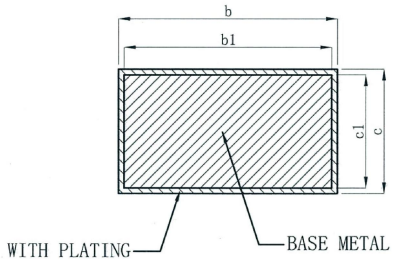


DIP16



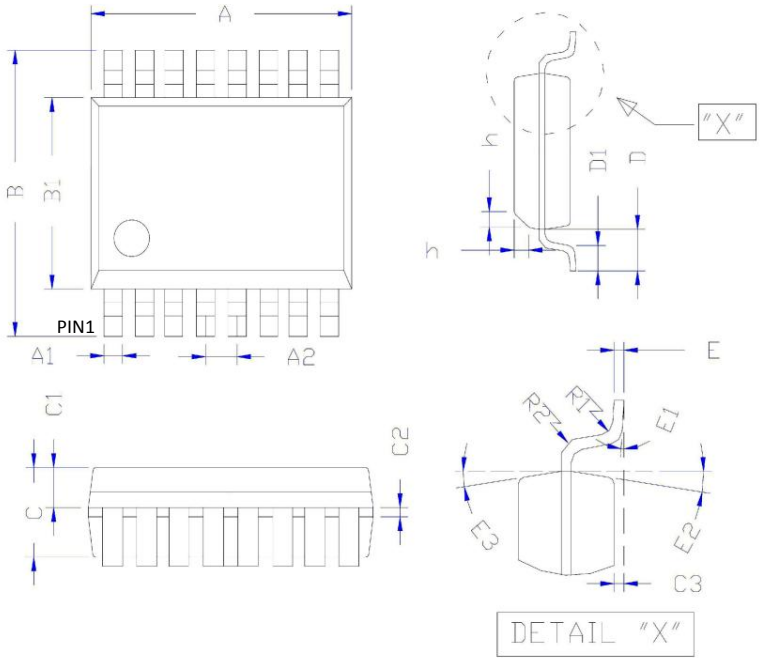






symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

TSSOP16



Symbol	Indicate	MIN	NOM	MAX
A	Overall length	4.95	5.00	5.05
A1	Foot width	0.20	0.22	0.24
A2	Foot spacing	0.60	0.65	0.70
B	Span	5.70	6.00	6.30
B1	Colloid width	3.80	3.90	4.00
C	Colloid thickness	0.95	1.00	1.05
C1	Thickness of upper colloid	0.40	0.41	0.42
C2		0.05	0.15	0.25
C3	Stand height	0.02	0.08	0.10
D	Fingle-sided Factory	0.85	1.05	1.25
D1	Foot length	0.40	0.65	0.85
E	Foot Thickness	0.15	0.20	0.25
E2	Foot Angle	0°		8°
h		0.30	0.40	0.50

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