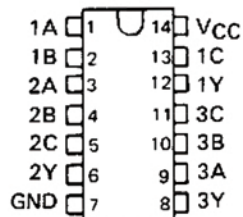


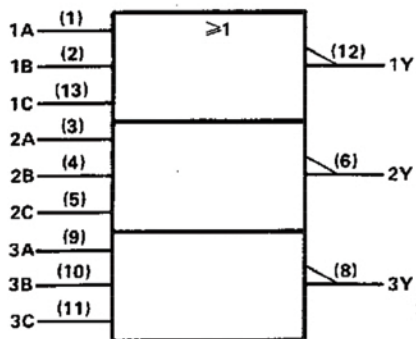
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

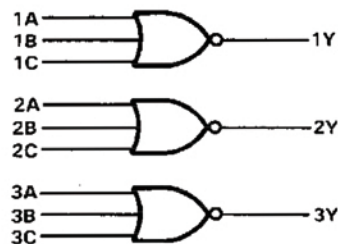
XD74LS27  
 (TOP VIEW)



logic symbol†



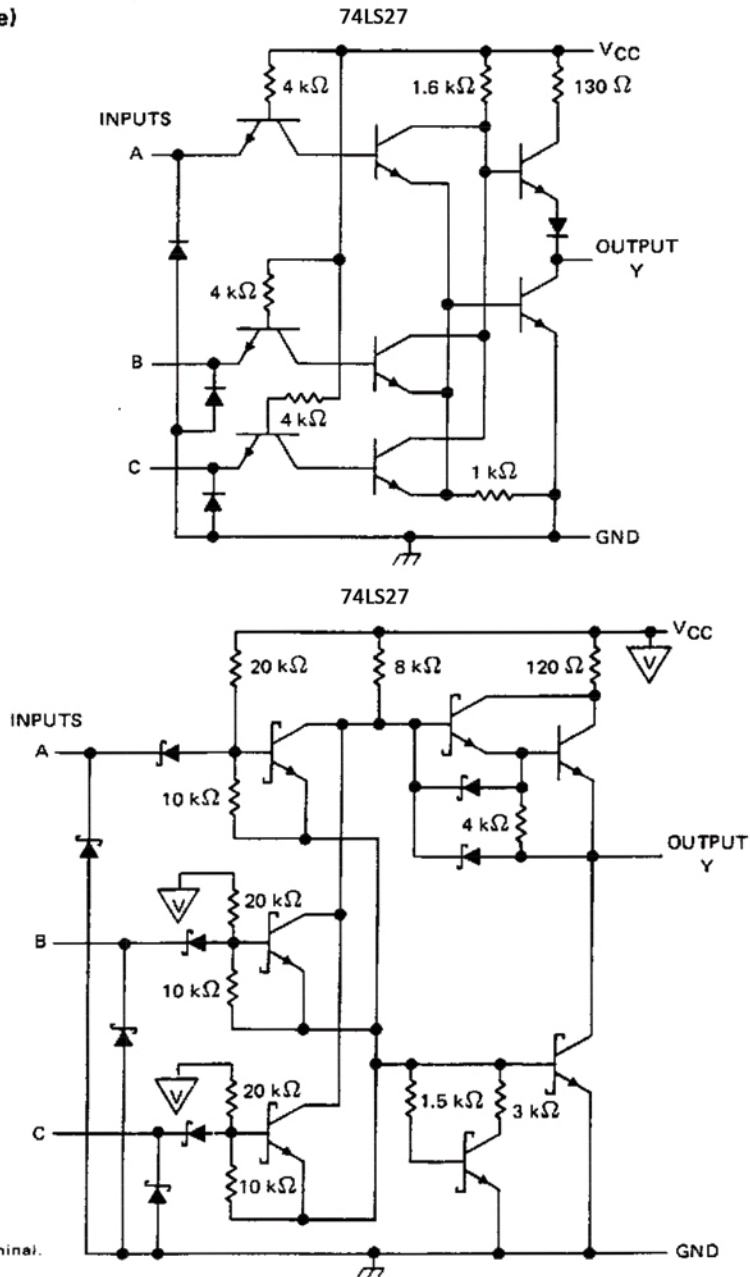
logic diagram



positive logic

$$Y = A + B + C \text{ or } Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

schematics (each gate)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: 74LS27	5.5 V
74LS27	7 V
Operating free-air temperature: 74LS27	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

**recommended operating conditions**

	74LS27			UNIT
	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			V
V <sub>IL</sub> Low-level input voltage			0.8	V
I <sub>OH</sub> High-level output current			-0.4	mA
I <sub>OL</sub> Low-level output current			8	mA
T <sub>A</sub> Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	74LS27			UNIT
		MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, V <sub>OH</sub> = 18 mA			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4mA	2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, I <sub>OL</sub> = 4mA		0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, I <sub>OL</sub> = 8mA		0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MIN, V <sub>I</sub> = 7V			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MIN, V <sub>I</sub> = 2.7V			20	µA
I <sub>IL</sub>	V <sub>CC</sub> = MIN, V <sub>I</sub> = 0.4V			-0.4	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MIN,	-20		-100	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MIN, V <sub>I</sub> = 0V		2	4	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MIN, See Note 2		3.4	6.8	mA

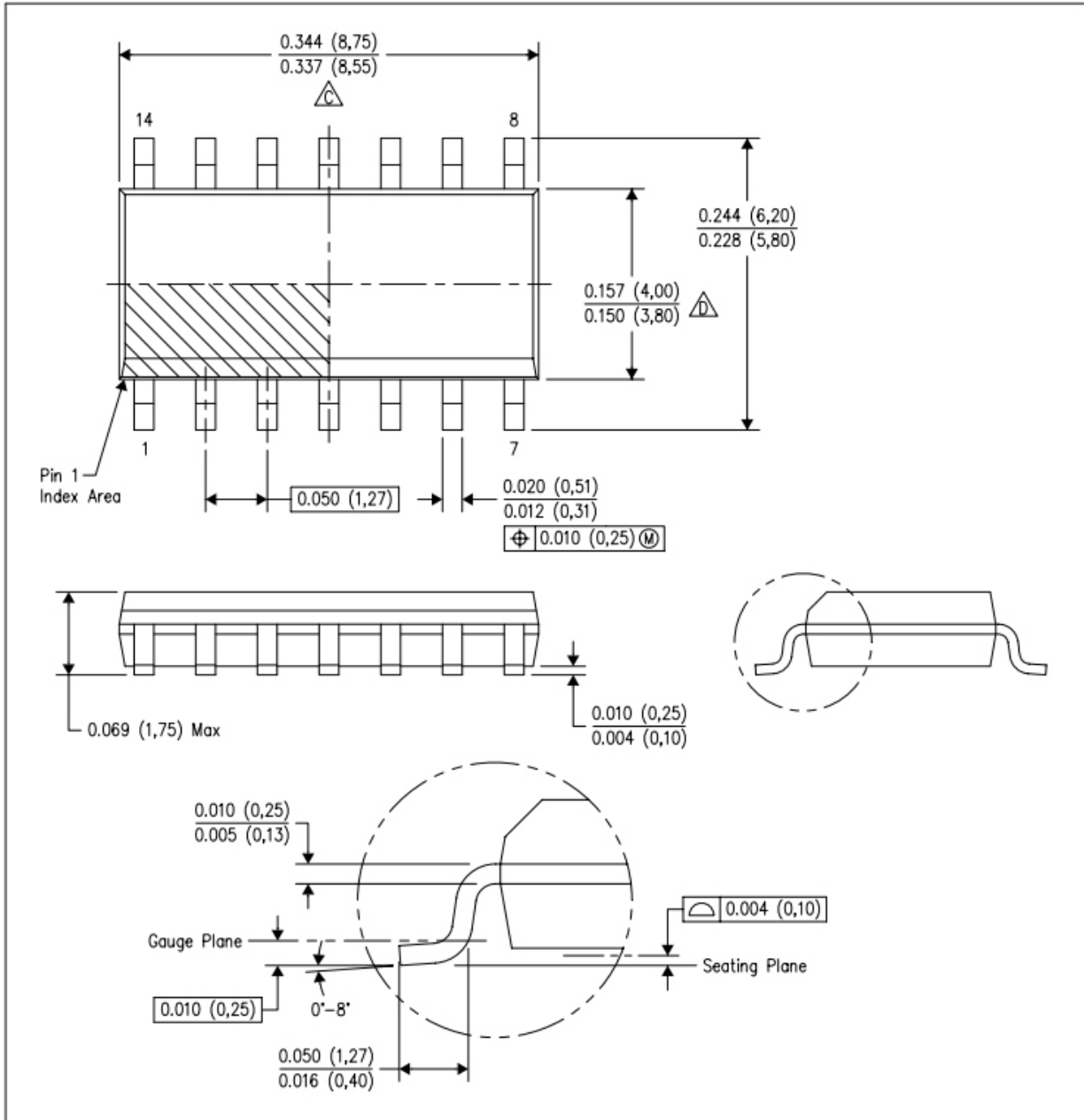
**switching characteristics, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A, B or C	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15pF		10	15	ns
t <sub>PLH</sub>					10	15	ns

**NOTE 3: Load circuits and voltage waveforms are shown in Section 1.**

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

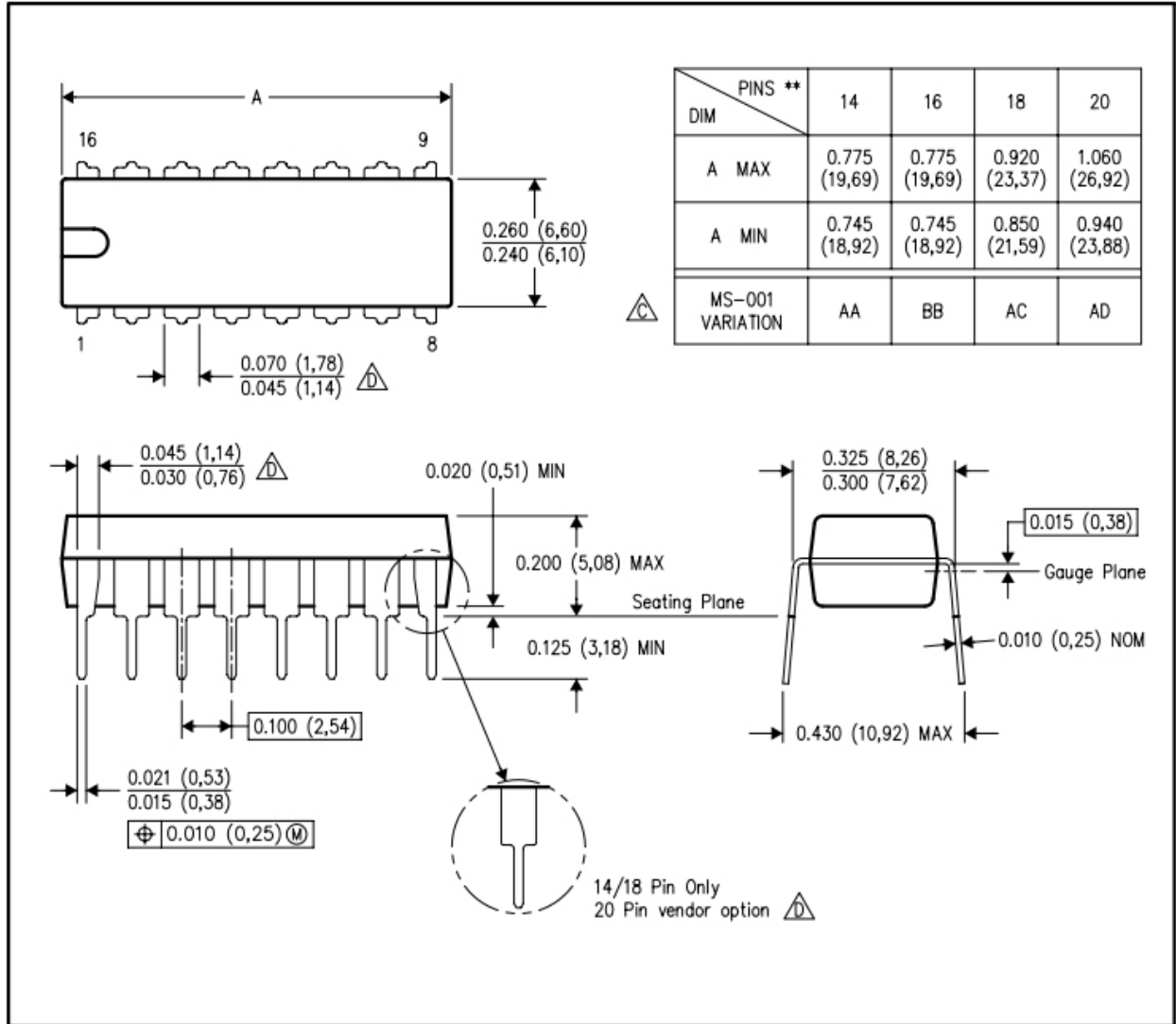


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

以上信息仅供参考. 如需帮助联系客服人员. 谢谢 XINLUDA

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